EEPROM MEMORY PRODUCTS

DATABOOK

1st EDITION

JUNE 1995

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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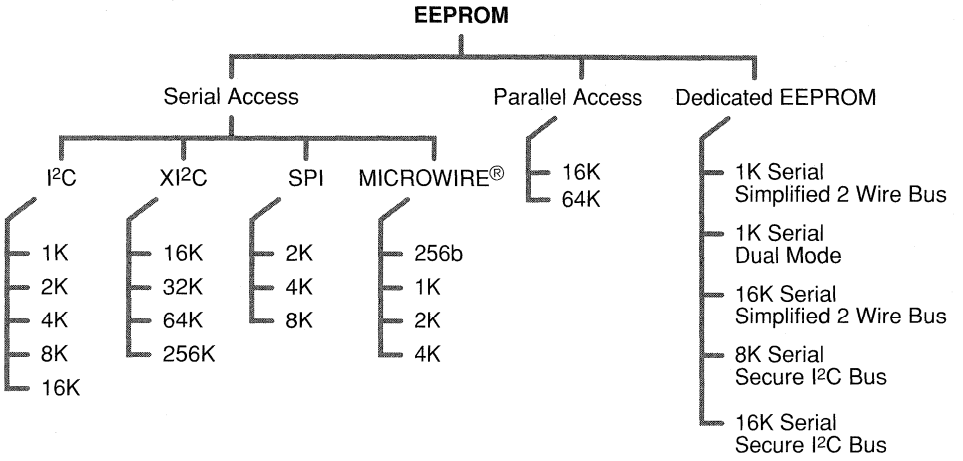
INTRODUCTION

SGS-THOMSON Microelectronics is a broad range semiconductor company. The product range includes memory products which satisfy the needs of a wide range of applications. They include:

- Non-Volatile Memories: OTP Memories, UV EPROMs, FLASH Memories, Serial and Parallel EEPROMs and NVRAMs (battery backed SRAMs)
- Synchronous and Asynchronous Fast SRAMs

This databook provides comprehensive technical information on the Serial and Parallel Access EEPROM products.



EEPROMs (Electrically Eraseable Programable Memories).

The EEPROM may be erased and programmed byte-by-byte, giving it an added flexibility compared to FLASH Memory which must be erased in bulk or sector conditions. Two distinct families of EEPROM are Serial or Parallel Access types. The Serial Access EEPROMs feature low pin counts (typically they are packaged in 8 pin packages) and a lower range of densities from 256 bit up to 64K bit. The Parallel Access EEPROMs, needing external access to both parallel Address and Data lines, are packaged in multi-pin packages, typically 28 or 32 pin for 64K density, and focus only on the higher memory densities from 16K bit upwards.

EEPROMs are widely used for storing equipment set-up parameters or data tables. The special CMOS process and cell designs used by SGS-THOMSON allows us to offer products with a very high endurance against wear-out that occurs after many erase/write cycles in this type of memory. Typically our EEPROMs are able to withstand 5 to 10 million cycles together with over 10 years data retention.

SGS-THOMSON has an extensive program of both process research and development and product design which results in many new product updates and introductions every year. Please contact your nearest Sales Office to learn about new products that have been introduced since this databook was published.

GENERAL INDEX

SERIAL ACCESS
I^2C BUS EEPROM

ST24C01, ST25C01
ST24W01, ST25W01

SERIAL ACCESS 1K (128 x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES with 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24 versions
  - 2.5V to 5.5V for ST25 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W01 and ST25W01
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

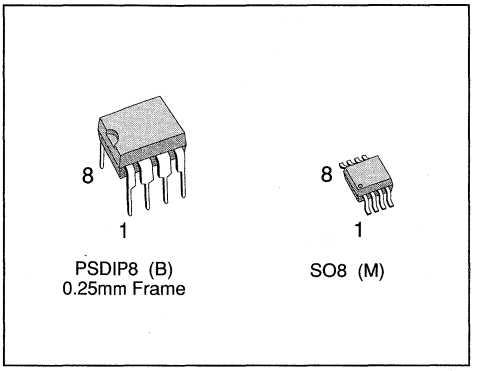
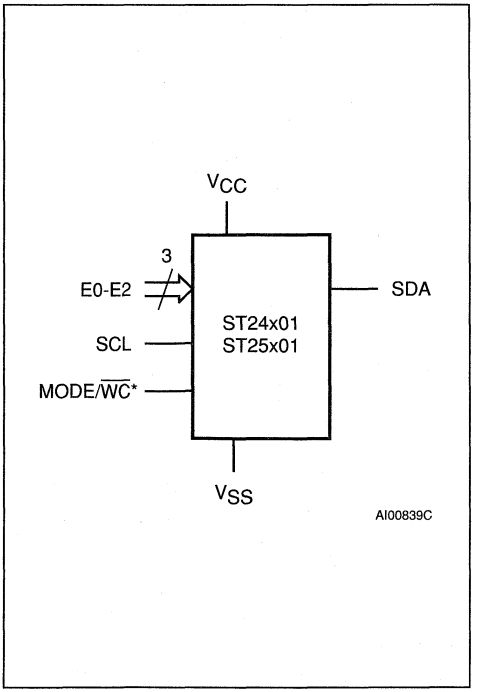


Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W01 products.

DESCRIPTION

This specification covers a range of 1K bits I^2C bus EEPROM products, the ST24/25C01, and the ST24/25W01. In the text, products are referred to as ST24/25x01, where "x" is: "C" for Standard version and "W" for hardware Write Control version.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

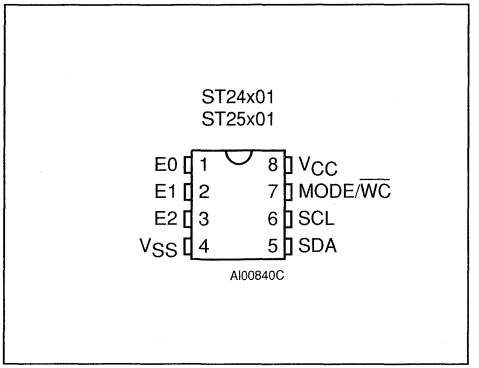


Figure 2B. SO Pin Connections

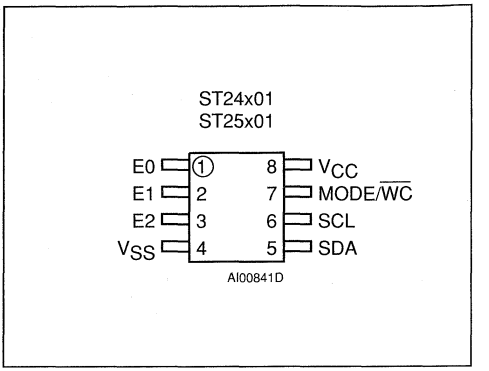


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x01 are 1K bit electrically erasable programmable memories (EEPROM), organized as 128 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to 8 x 1K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	$\overline{RW}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, $\overline{RW}$ = '0', Address,
	'1'			reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 128	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, $\overline{RW}$ = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $\overline{RW}$ = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W01 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W01 and ST25W01 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}.

SIGNAL DESCRIPTION (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x01 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x01 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x01 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x01 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x01 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x01, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

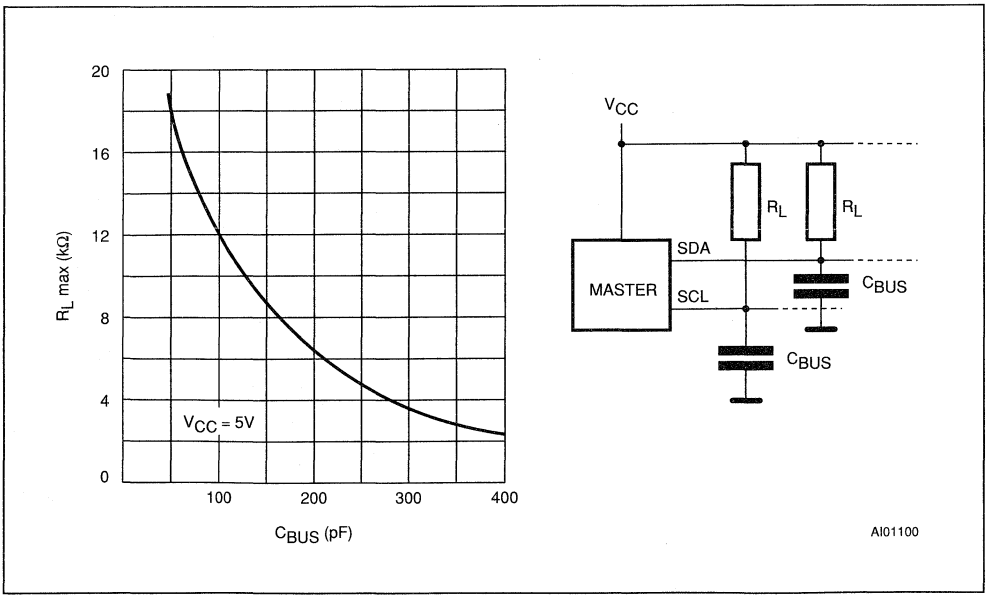


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W01)	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W01)	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

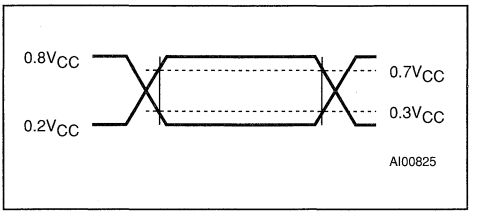
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to 8 x 1K memories can be connected on the same bus giving a memory capacity total of 8K bits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms

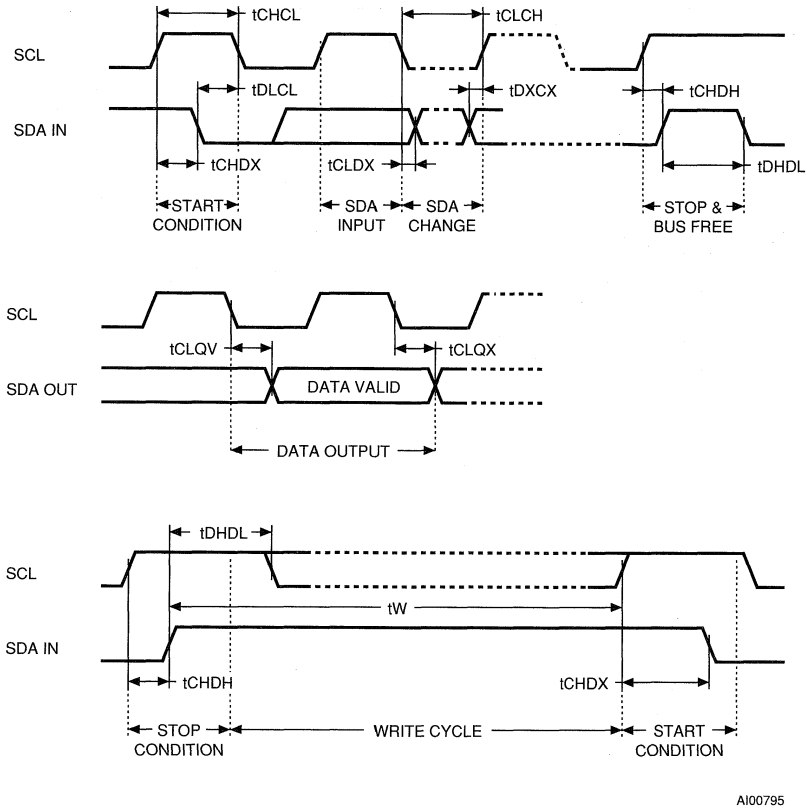
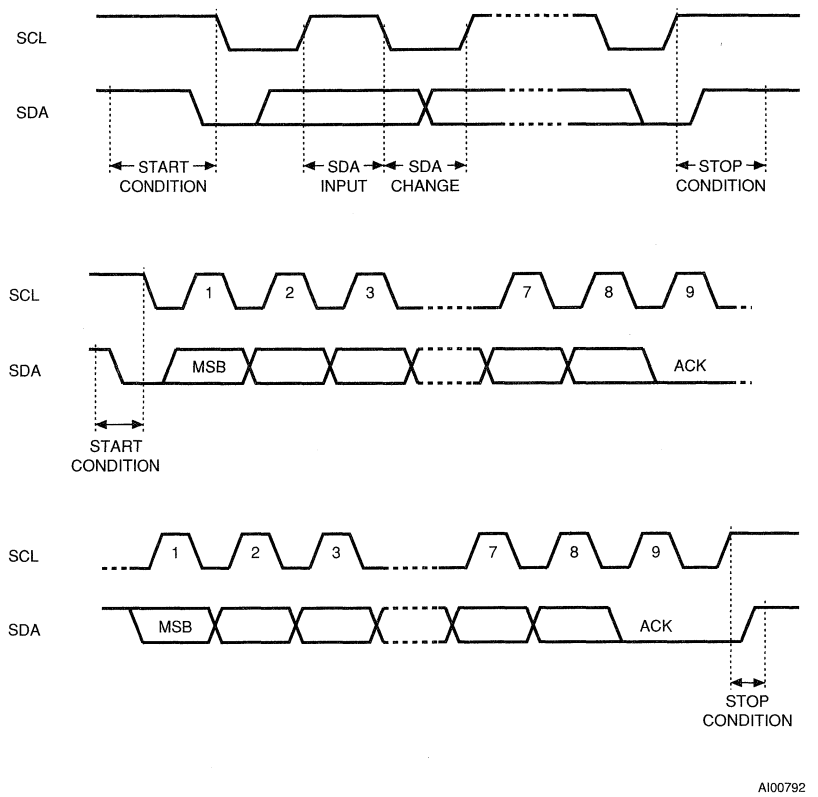


Figure 6. I²C Bus Protocol



Write Operations

The Multibyte Write mode (only available on the ST24/25C01 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 7 bits (the Most Significant Bit is ignored) provides access to any of the 128 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W01 versions, any write command with $\overline{WC}$ = 1 (during a period of time from the START condition untill the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 5 most significant address bits A6-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Figure 7. Write Cycle Polling using ACK

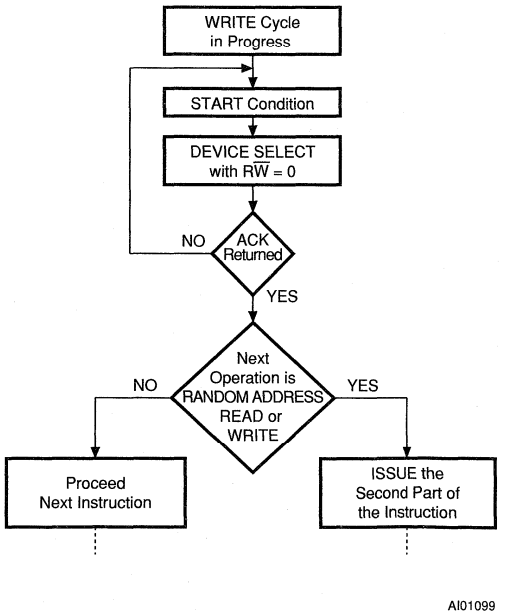
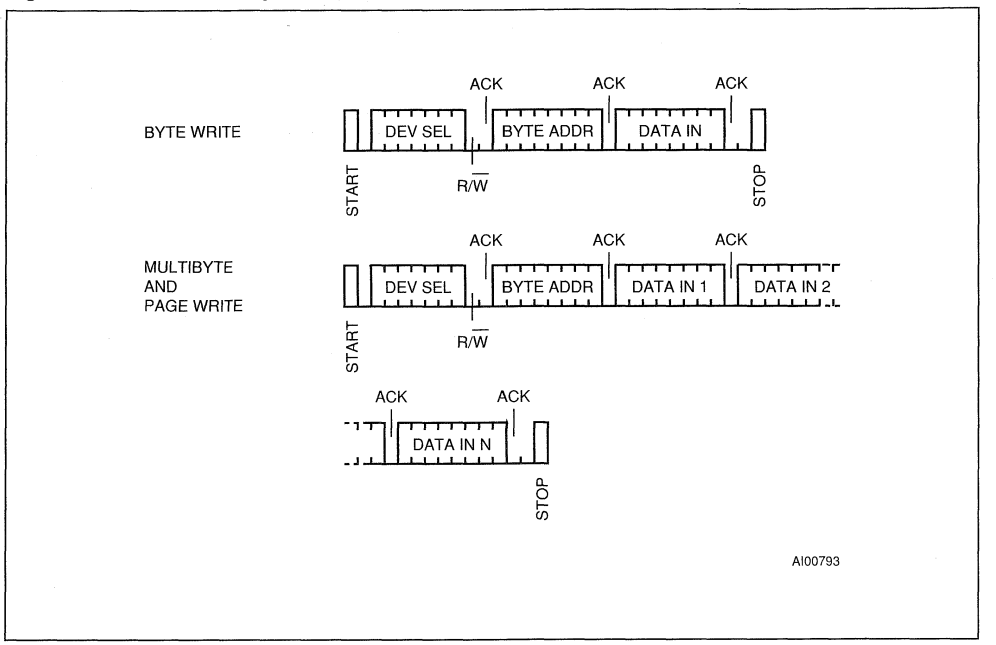


Figure 8. Write Modes Sequence (ST24/25C01)



Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (tW) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

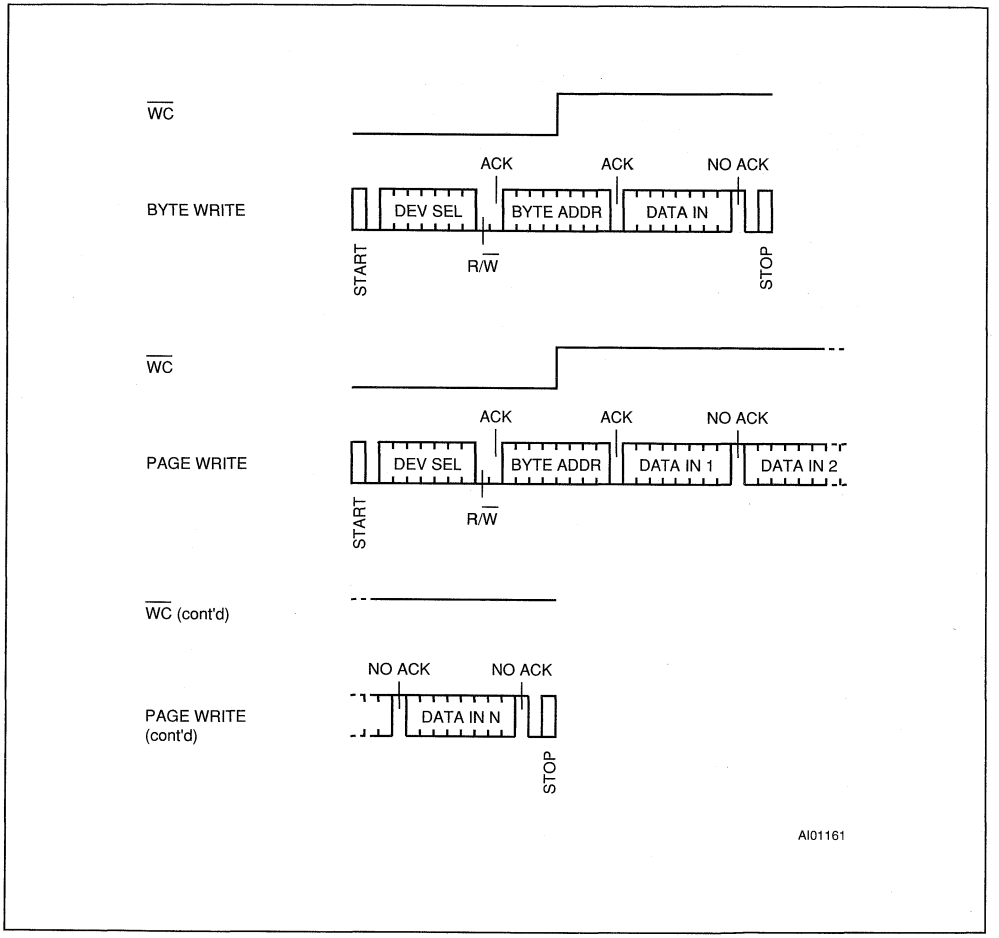
Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

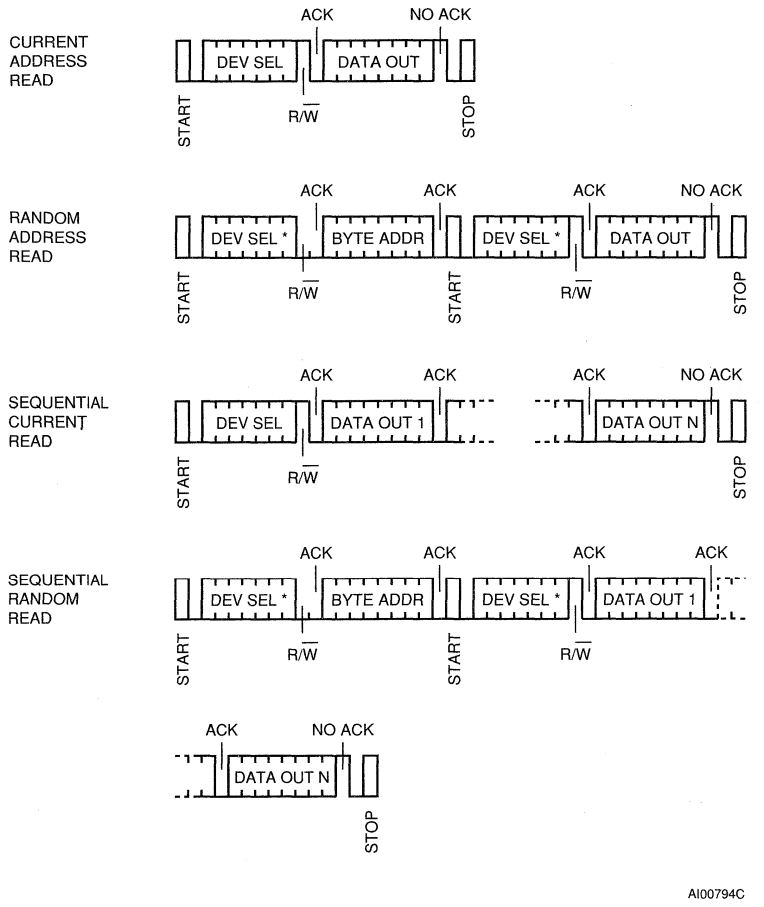
Figure 9. Write Modes Sequence with Write Control = 1 (ST24/25W01)



Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

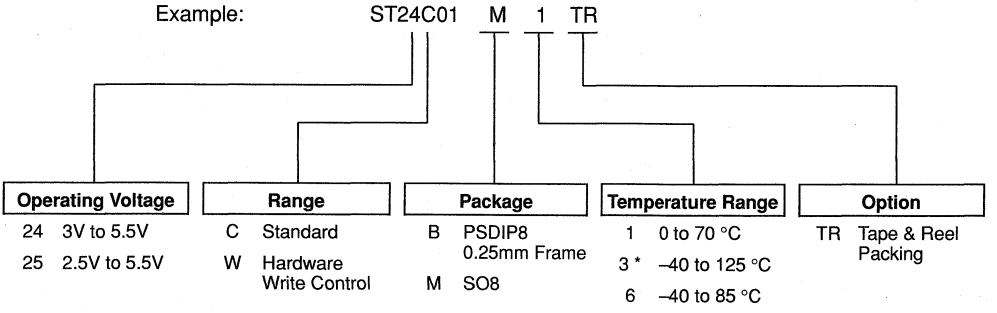
Acknowledge in Read Mode. In all read modes the ST24/25x01 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the St24/25x01 terminate the data transfer and switches to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

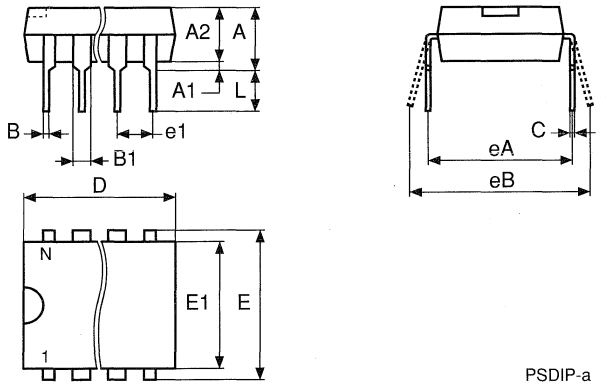
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	

PSDIP8



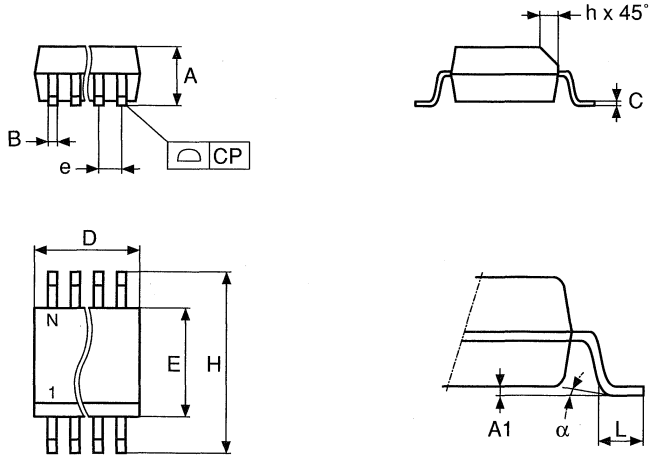
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



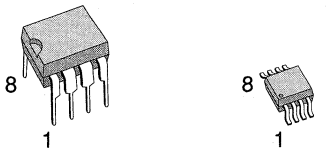
SO-a

Drawing is out of scale

ST24C02, ST25C02 ST24W02, ST25W02

SERIAL ACCESS 2K (256 x 8) EEPROM

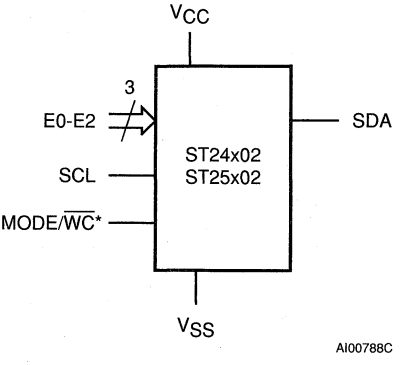
- 1 MILLION ERASE/WRITE CYCLES with 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x02 versions
  - 2.5V to 5.5V for ST25x02 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W02 and ST25W02
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W02 products.

DESCRIPTION

This specification covers a range of 2K bits I^2C bus EEPROM products, the ST24/25C02 and ST24/25W02. In the text, products are referred to as ST24/25x02, where "x" is: "C" for Standard version and "W" for hardware Write Control version.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

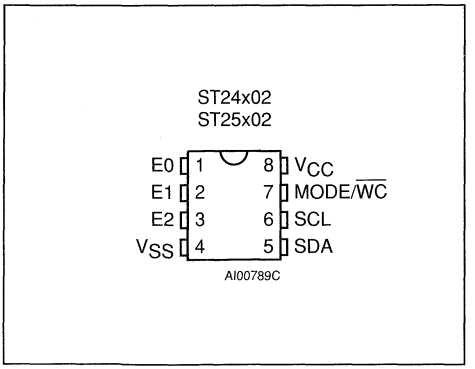


Figure 2B. SO Pin Connections

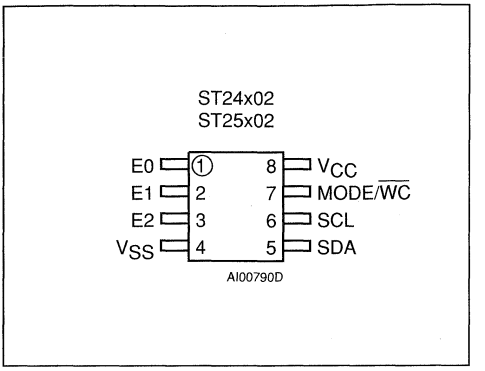


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x02 are 2K bit electrically erasable programmable memories (EEPROM), organized as 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to 8 x 2K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 256	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W02 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W02 and ST25W02 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x02 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x02 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x02 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x02 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x02 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x02, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

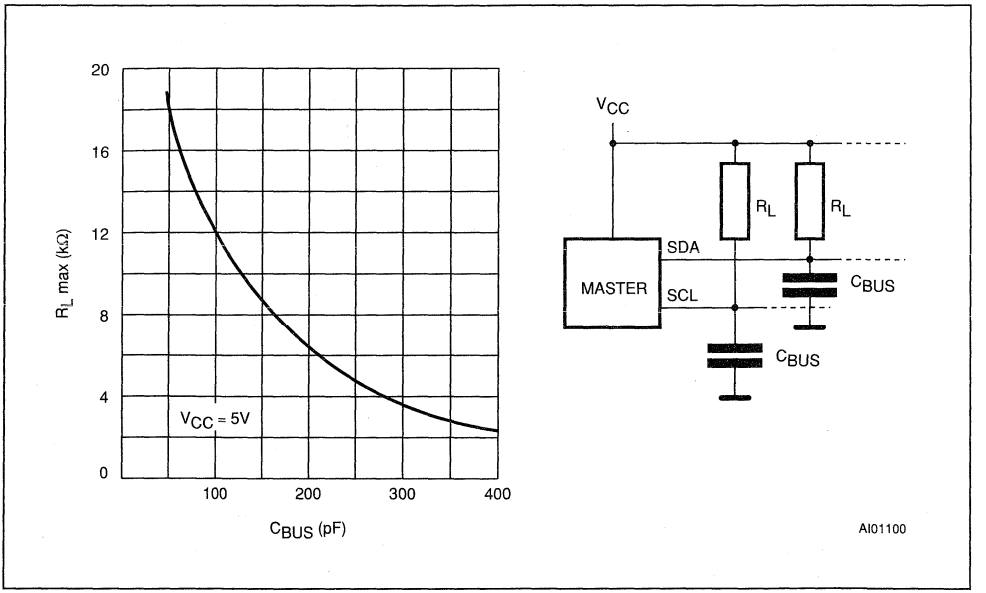


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W02)	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W02)	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

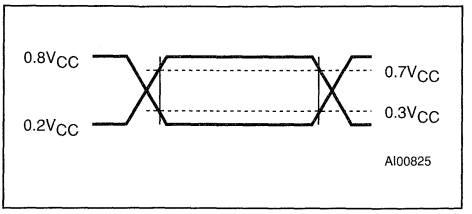
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to 8 x 2K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms

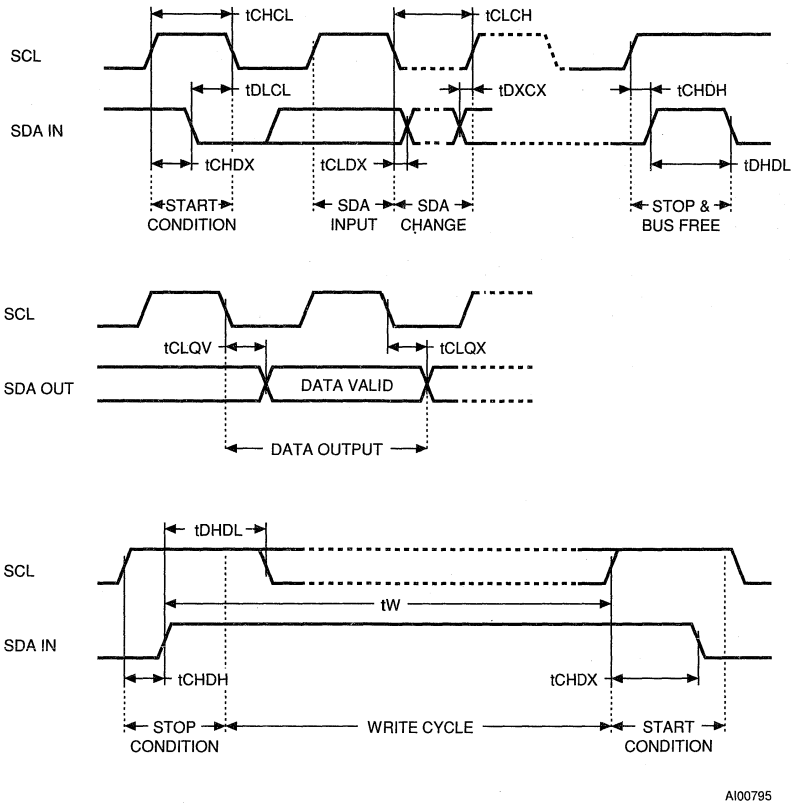
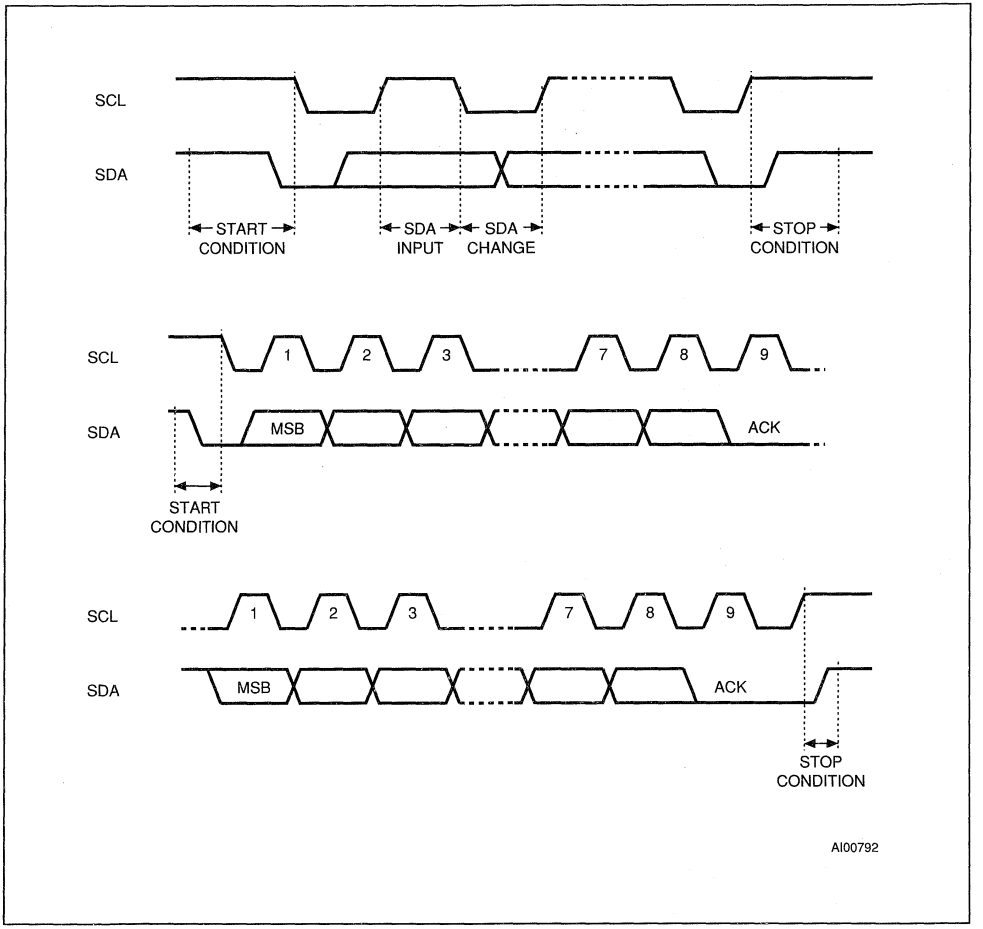


Figure 6. I^2C Bus Protocol



Write Operations

The Multibyte Write mode (only available on the ST24/25C02 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W02 versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Figure 7. Write Cycle Polling using ACK

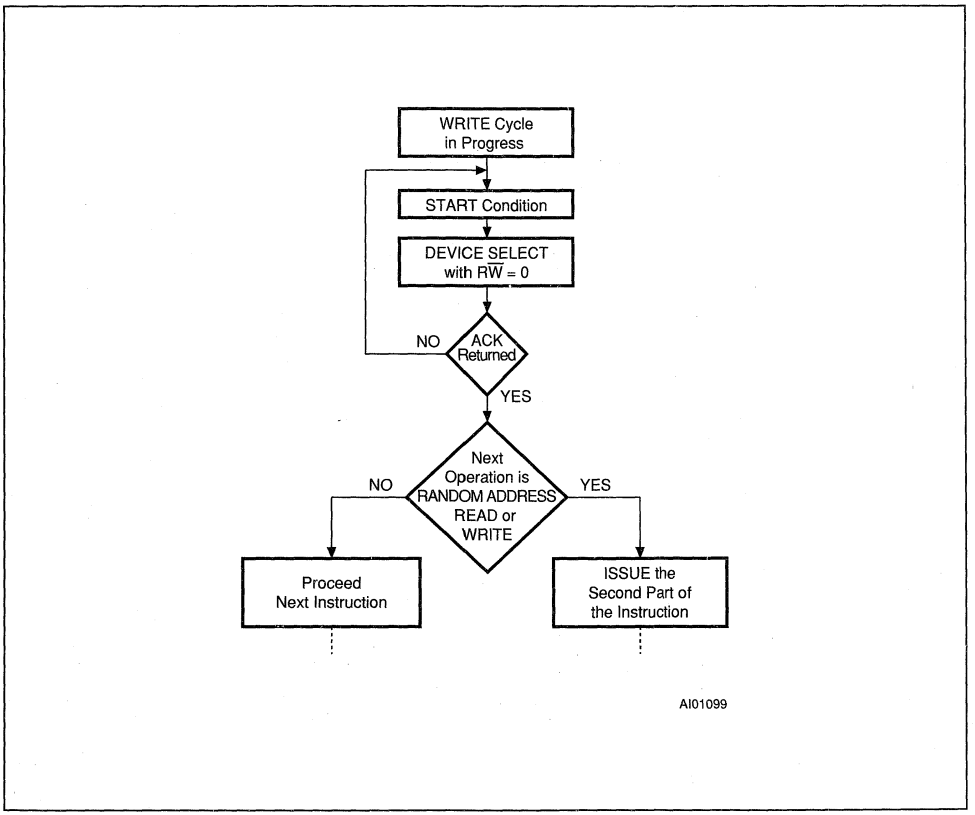
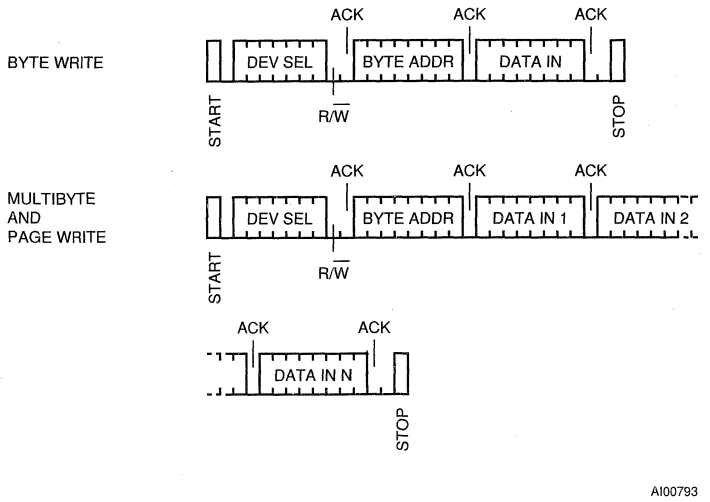


Figure 8. Write Modes Sequence (ST24/25C02)



Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (tw) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

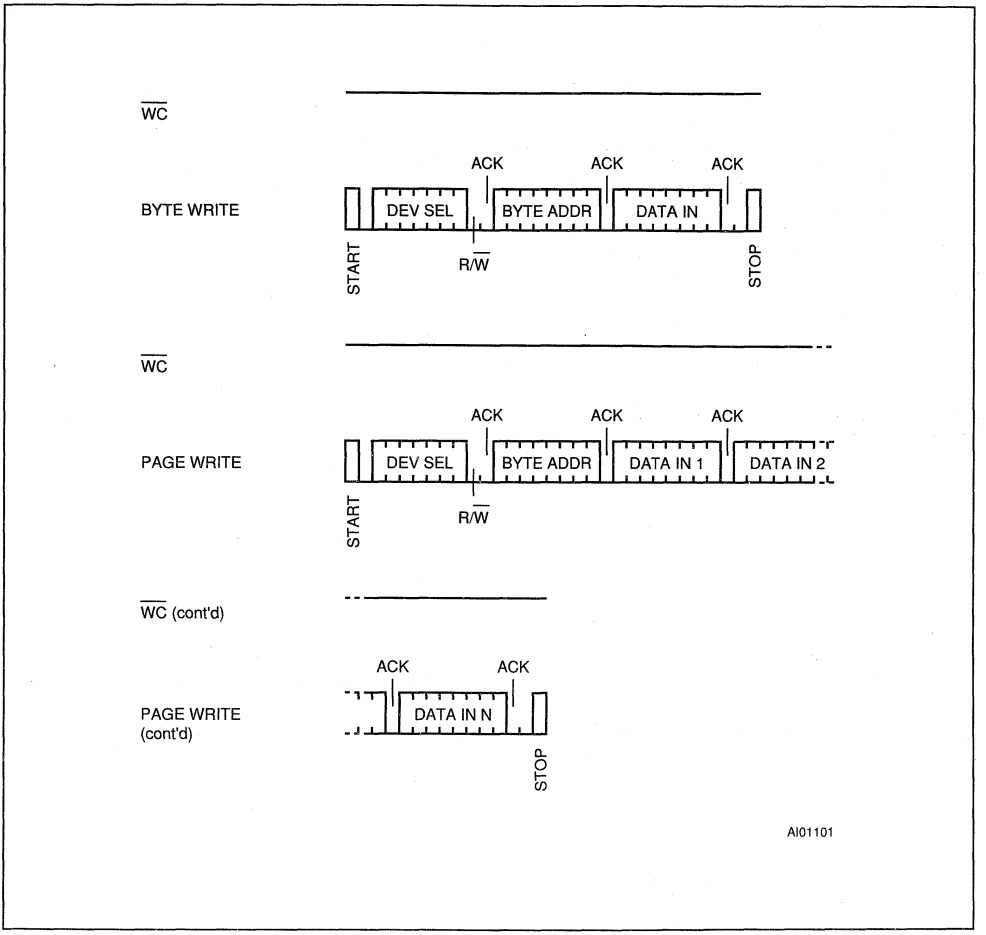
Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

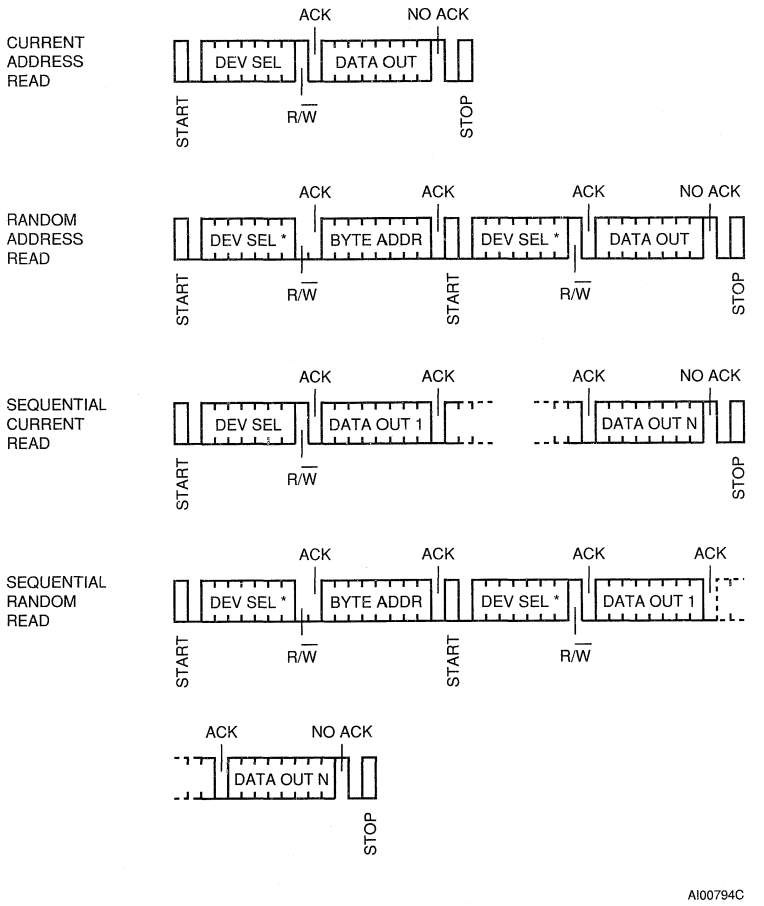
Figure 9. Write Modes Sequence with Write Control = 1 (ST24/25W02)



Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

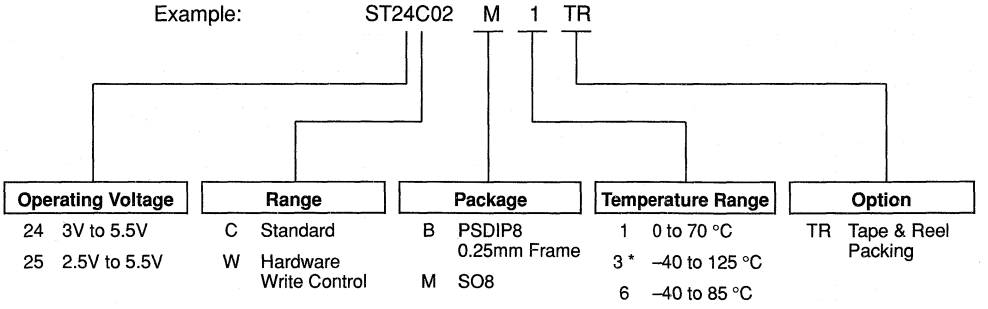
Acknowledge in Read Mode. In all read modes the ST24/25x02 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x02 terminate the data transfer and switches to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

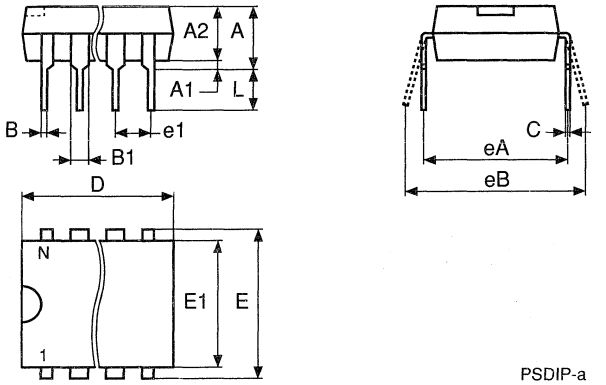
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



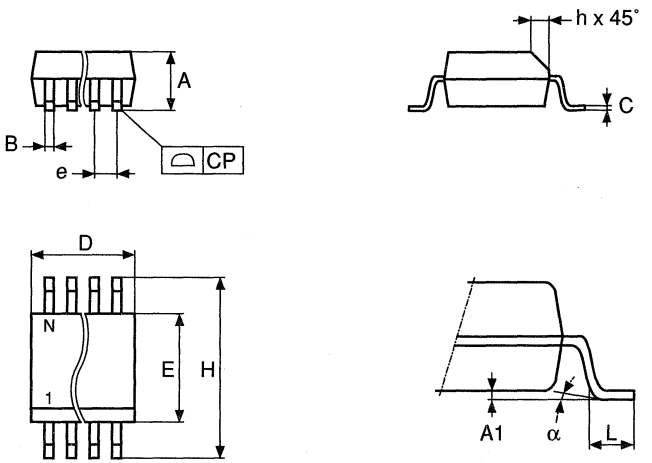
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is out of scale

ST24C04, ST25C04
ST24W04, ST25W04

SERIAL ACCESS 4K (512 x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES with 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x04 versions
  - 2.5V to 5.5V for ST25x04 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W04 and ST25W04
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

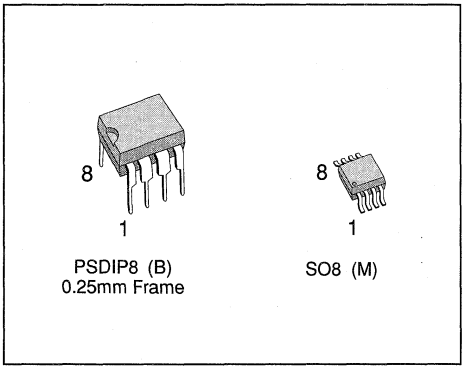
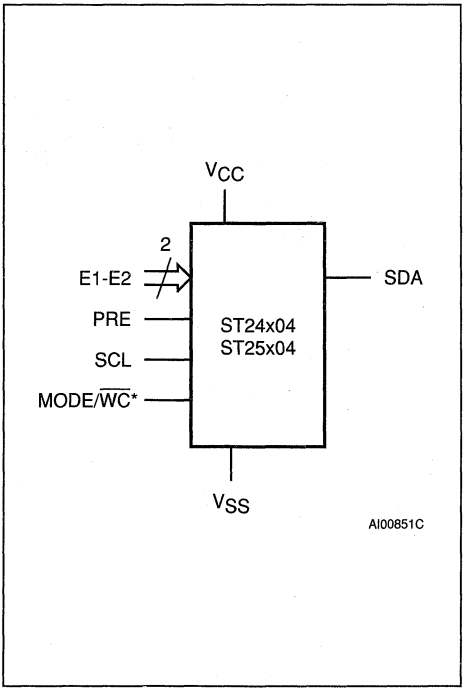


Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W04 products.

DESCRIPTION

This specification covers a range of 4K bits I^2C bus EEPROM products, the ST24/25C04 and the ST24/25W04. In the text, products are referred to as ST24/25x04, where "x" is: "C" for Standard version and "W" for hardware Write Control version.

Table 1. Signal Names

PRE	Write Protect Enable
E1-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

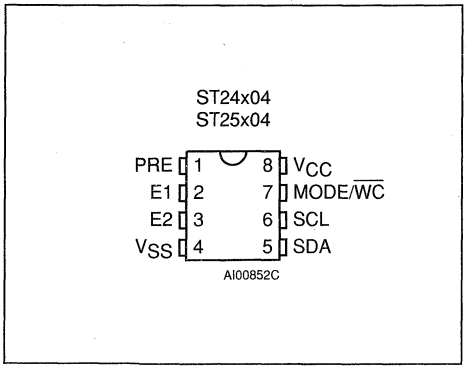


Figure 2B. SO Pin Connections

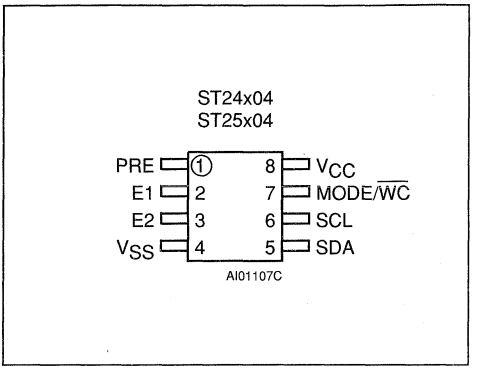


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x04 are 4K bit electrically erasable programmable memories (EEPROM), organized as 2 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 2 chip enable inputs (E2, E1) so that up to 4 x 4K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	A8	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 512	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W04 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E1 - E2). These chip enable inputs are used to set the 2 least significant bits (b2, b3) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Protect Enable (PRE). The PRE input pin, in addition to the status of the Block Address Pointer bit (b2, location 1FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W04 and ST25W04 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x04 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x04 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x04 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x04 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x04 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x04, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

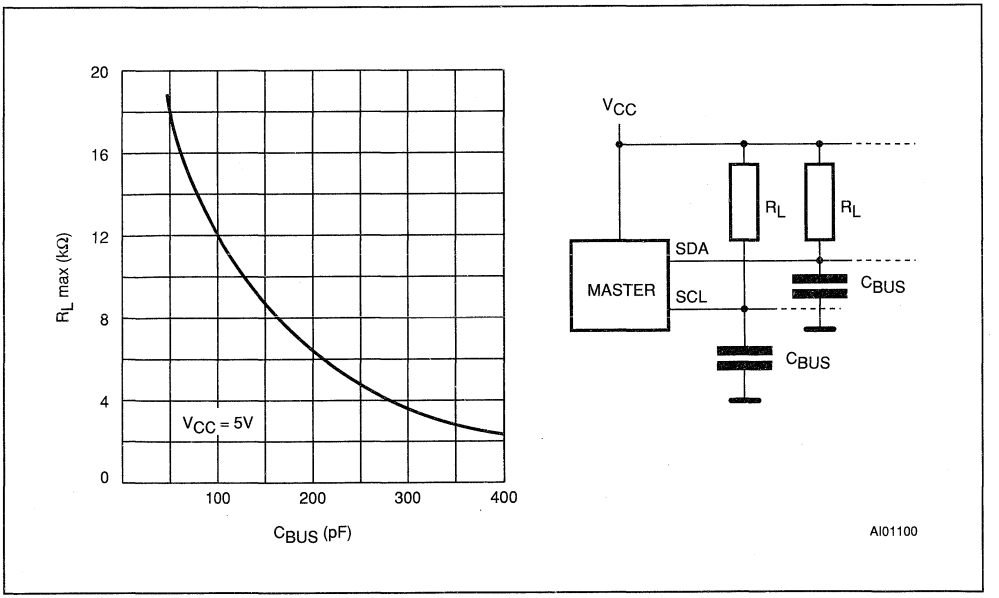


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W04)	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W04)	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E1-E2, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E1-E2, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

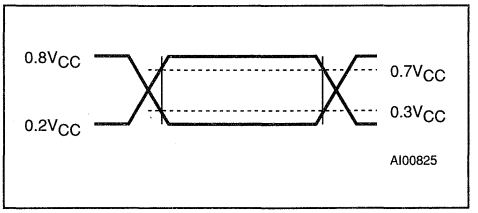
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms

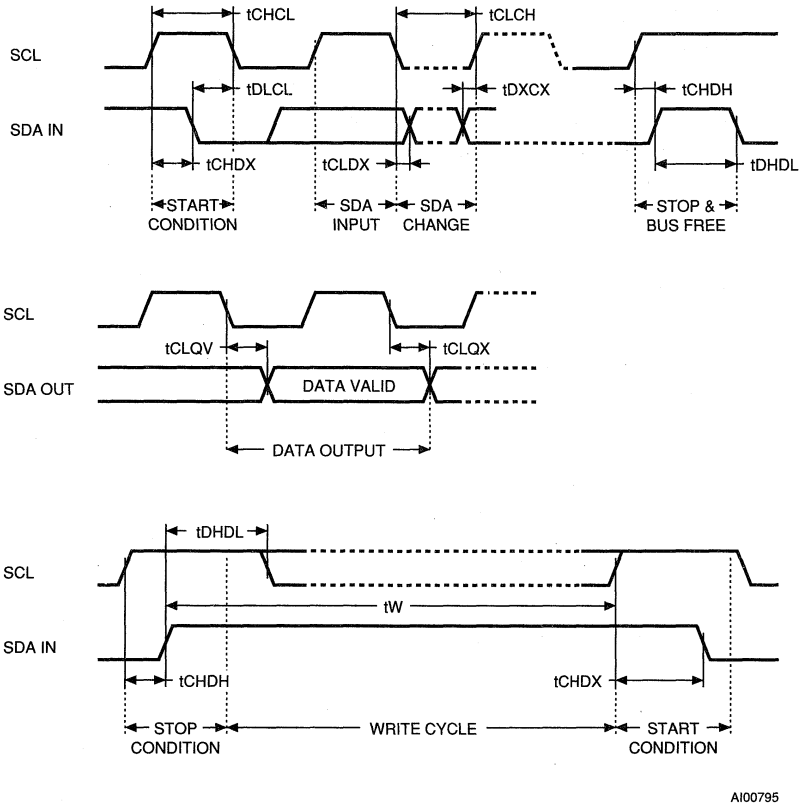


DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 2 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1. Thus up to 4 x 4K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following 2 bits to its chip enable inputs E2, E1.

The 7th bit sent is the block number (one block = 256 bytes). The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms



Write Operations

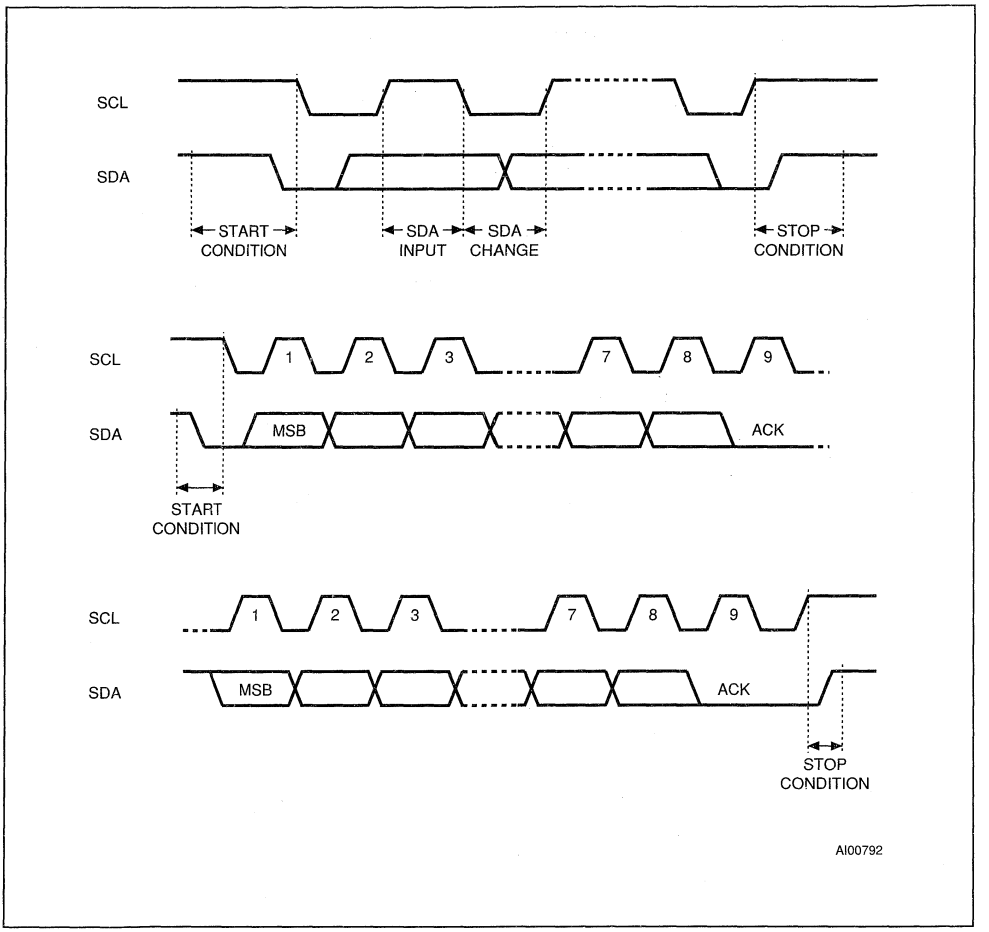
The Multibyte Write mode (only available on the ST24/25C04 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to one block of 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W04 versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Figure 6. I²C Bus Protocol



Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes as soon as the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant mem-

ory address bits (A7-A3) are the same inside one block. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

Figure 7. Memory Protection

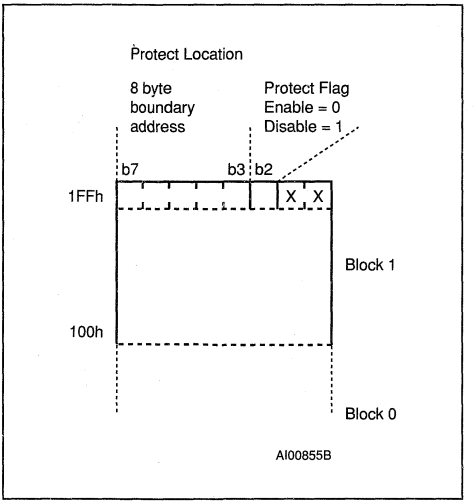


Figure 8. Write Cycle Polling using ACK

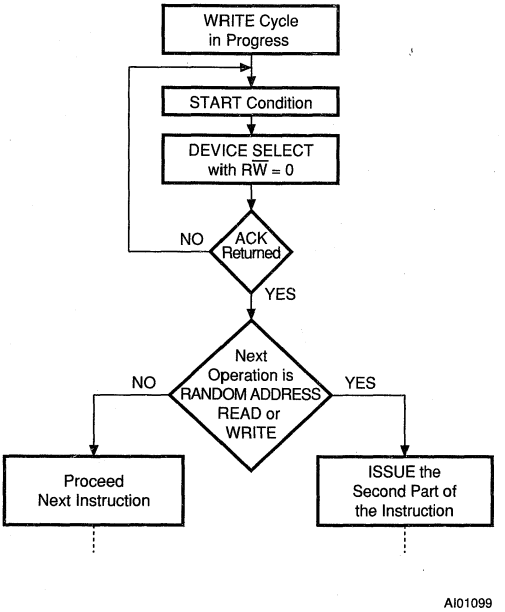
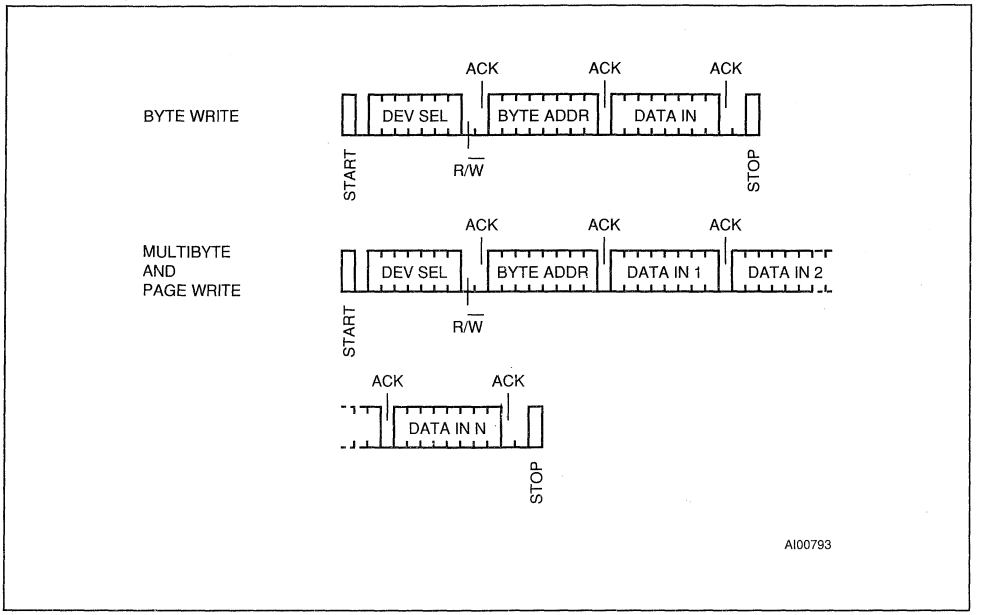


Figure 9. Write Modes Sequence (ST24/25C04)



DEVICE OPERATION (cont'd)

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Write Protection. Data in the upper block of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 1FFh) when the PRE input pin is taken high and when the Protect Flag (bit b2 in location 1FFh) is set to '0'. The boundary address is user defined by writing a value in the Block Address Pointer (location 1FFh).

This Block Address Pointer defines an 8 bit address composed of the 5 MSBs of location 1FFh and 3 LSBs which are read as '0'. This address pointer can therefore address a boundary in steps of 8 bytes.

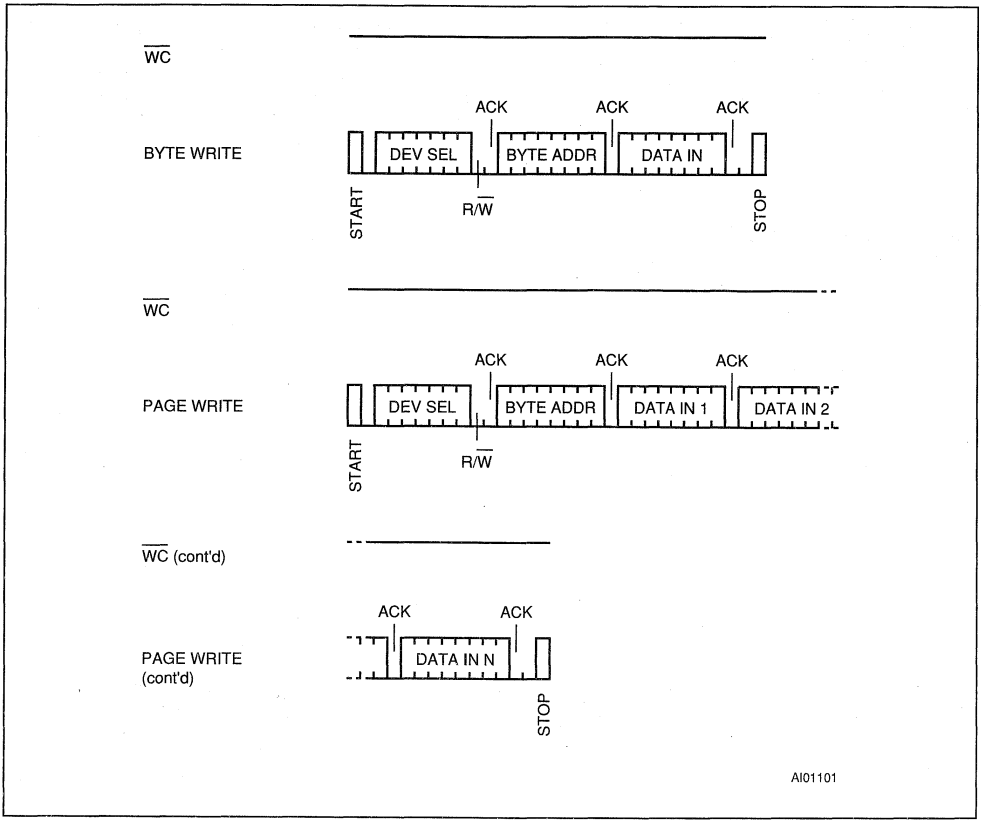
The sequence to follow to use the Write Protected feature is:

- write the data to be protected into the top of the memory, up to, but not including, location 1FFh;
- set the protection by writing the correct bottom boundary address, into location 1FFh, with bit b2 (Protect flag) set to '0'.

The area will now be protected when the PRE input is taken High.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 3 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 1FFh, by 3 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 8 bytes lower boundary of the protected area.

Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W04)



Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 11. This is followed by another START condition from the master and the byte address is repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

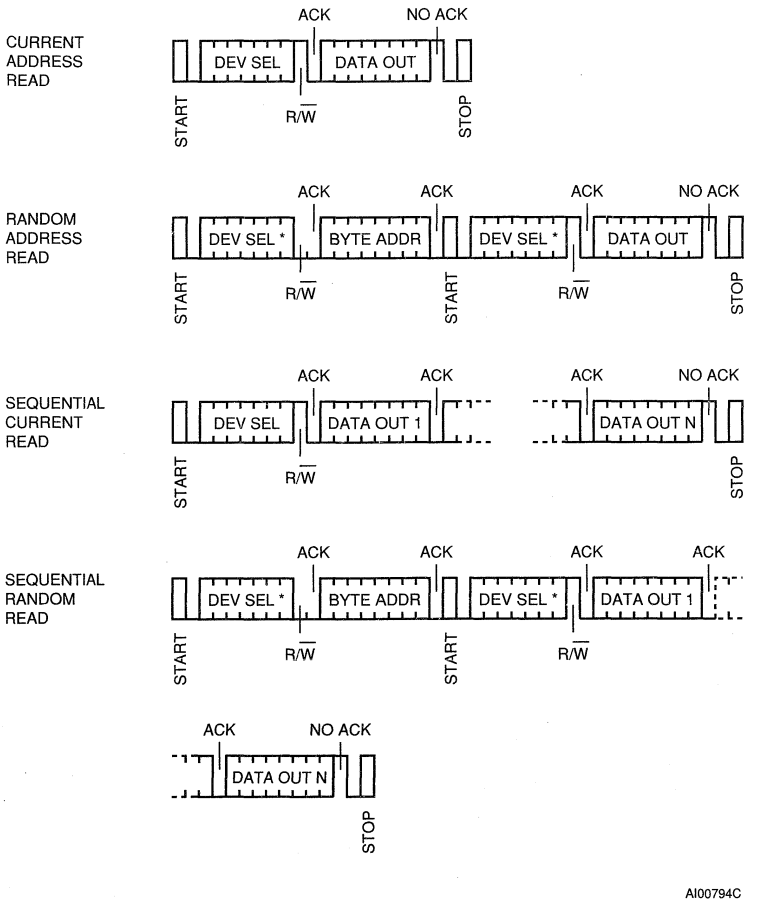
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte out-

DEVICE OPERATION (cont'd)

put, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

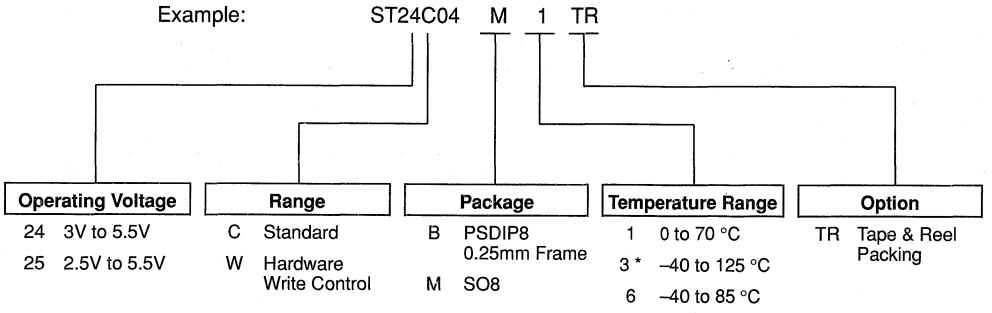
Acknowledge in Read Mode. In all read modes the ST24/25x04 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x04 terminate the data transfer and switches to a standby state.

Figure 11. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's".(FFh).

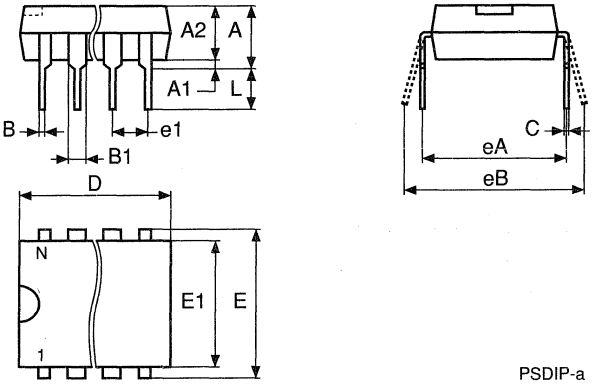
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	

PSDIP8



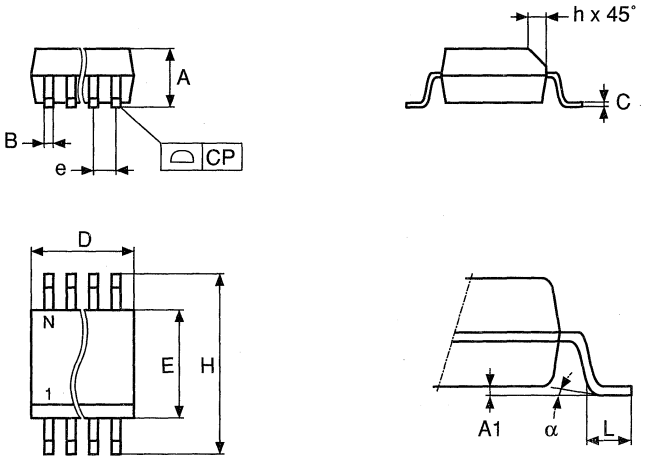
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



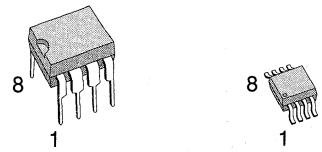
SO-a

Drawing is out of scale

ST24C08, ST25C08 ST24W08, ST25W08

SERIAL ACCESS 8K (1K x 8) EEPROM

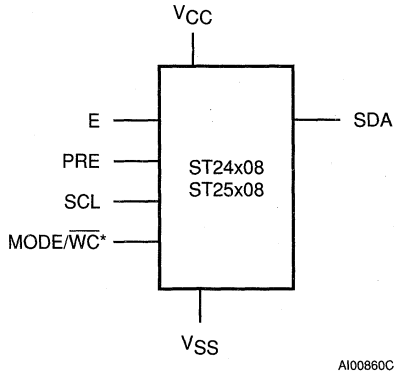
- 1 MILLION ERASE/WRITE CYCLES with 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x08 versions
  - 2.5V to 5.5V for ST25x08 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W08 and ST25W08
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W08 products.

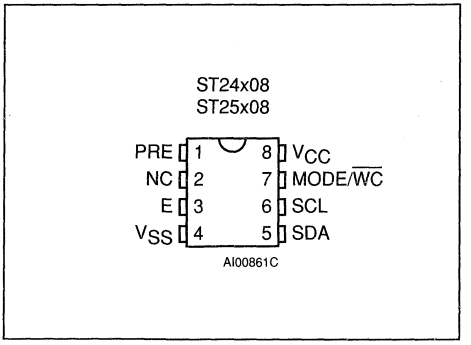
DESCRIPTION

This specification covers a range of 8K bits I^2C bus EEPROM products, the ST24/25C08 and the ST24/25W08. In the text, products are referred to as ST24/25x08, where "x" is: "C" for Standard version and "W" for Hardware Write Control version.

Table 1. Signal Names

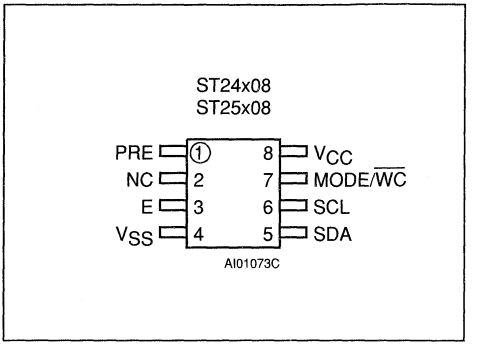
PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x08 are 8K bit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 1 chip enable input (E) so that up to 2 x 8K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable	Block Select		RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E	A9	A8	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 1024	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	8	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W08 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E). This chip enable input is used to set one least significant bit (b3) of the device select byte code. This input may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Protect Enable (PRE). The PRE input pin, in addition to the status of the Block Address Pointer bit (b2, location 3FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also WC feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control (WC). An hardware Write Control (WC) feature is offered only for ST24W08 and ST25W08 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC = V_{IH}) or disable (WC = V_{IL}) the internal write protection. When unconnected the WC input is internally read as V_{IL}.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x08 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x08 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x08 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x08 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x08 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x08, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

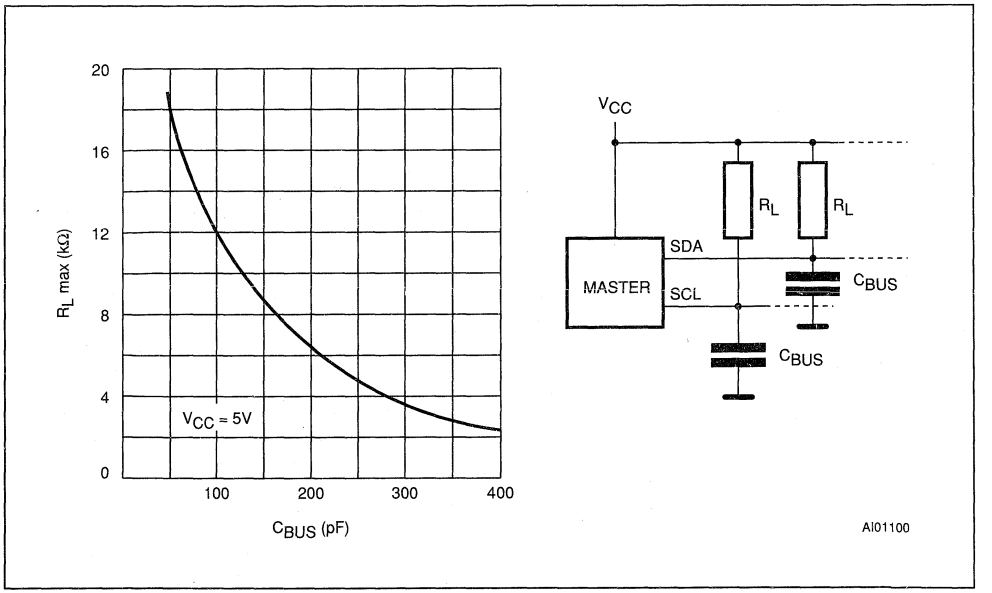


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W08)	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W08)	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

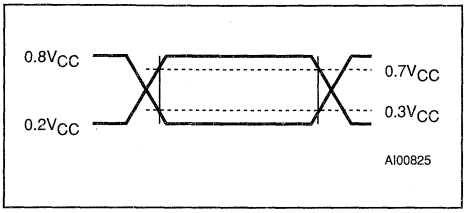
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms

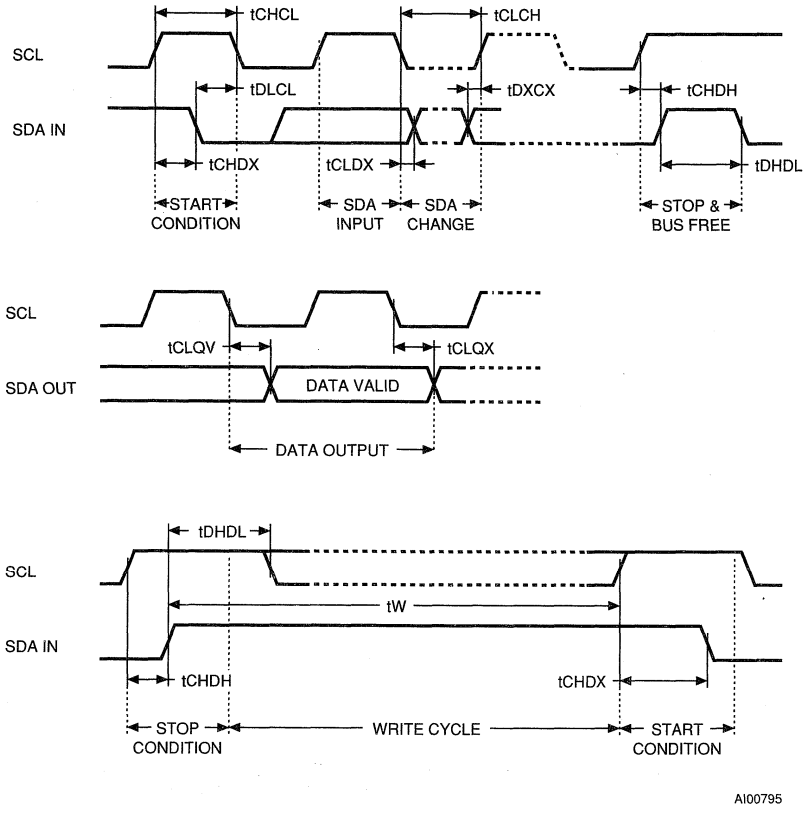


DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following bit identifies the specific memory on the bus. It is matched to the chip enable signal E. Thus up to 2 x 8K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following bit to its chip enable input E.

The 6th and 7th bits sent, select the block number (one block = 256 bytes). The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms



Write Operations

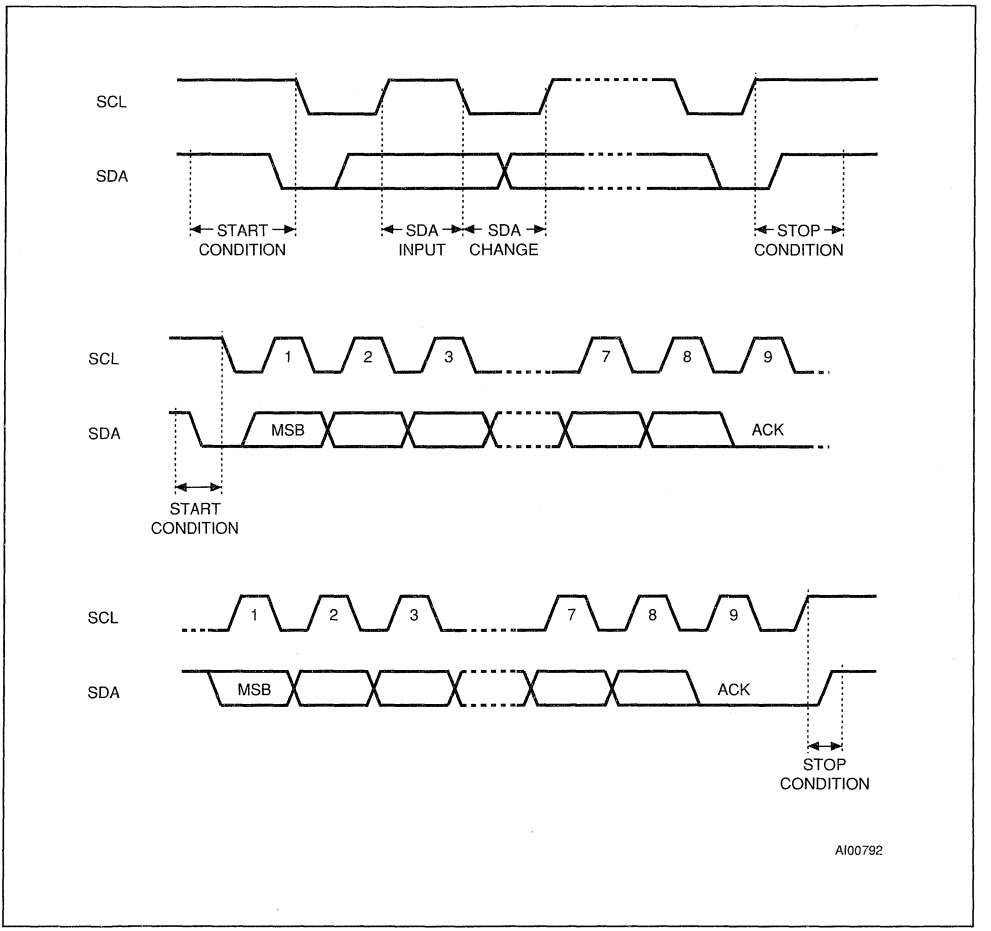
The Multibyte Write mode (only available on the ST24/25C08 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to one block of 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W08 versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the standby current.

Figure 6. I^2C Bus Protocol



Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 5 most significant address bits A7-A3), the programming time is then doubled to a maximum of 20ms. Writing more than 8 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 16 bytes long). However, the Multibyte Write can properly write up to 16 consecutive bytes only if the first address of these 16 bytes is the first address of the row, the 15 following bytes being written in the 15 following bytes of this same row.

Page Write. For the Page Write mode the MODE pin must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant memory address bits (A7-A4) are the same inside one block. The master sends from one up to 16 bytes

of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

Figure 7. Memory Protection

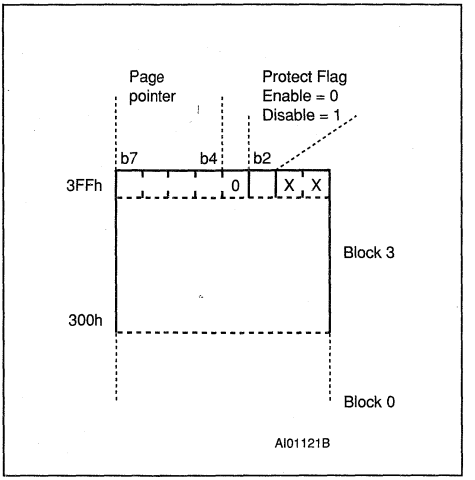


Figure 8. Write Cycle Polling using ACK

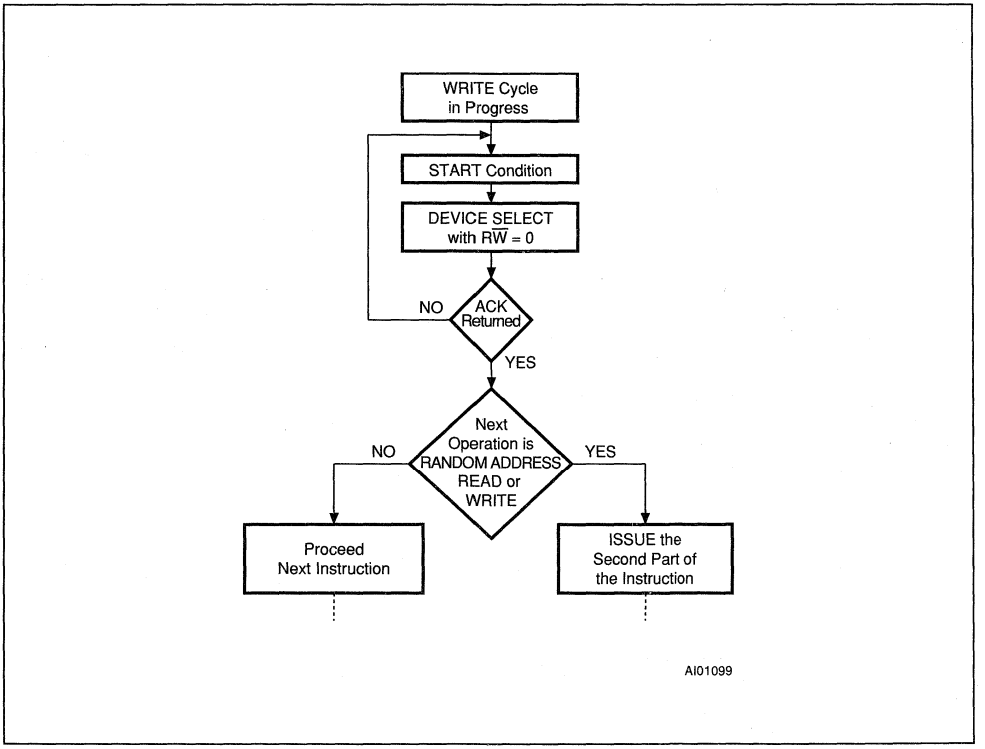
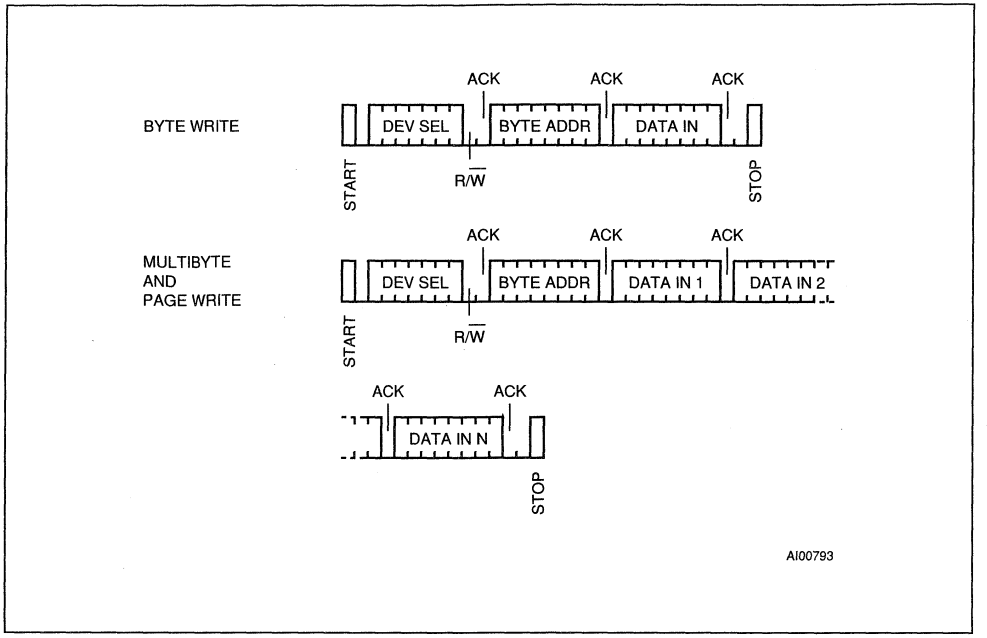


Figure 9. Write Modes Sequence (ST24/25C08)



DEVICE OPERATION (cont'd)

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Write Protection. Data in the upper block of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 3FFh) when the PRE input pin is taken high and when the Protect Flag (bit b2 in location 3FFh) is set to '0'. The boundary address is user defined by writing a value in the Block Address Pointer (location 3FFh).

This Block Address Pointer defines an 8 bit address composed of the 4 MSBs of location 3FFh and 4 LSBs which are read as '0'. This address pointer can therefore address a boundary in steps of 16 bytes.

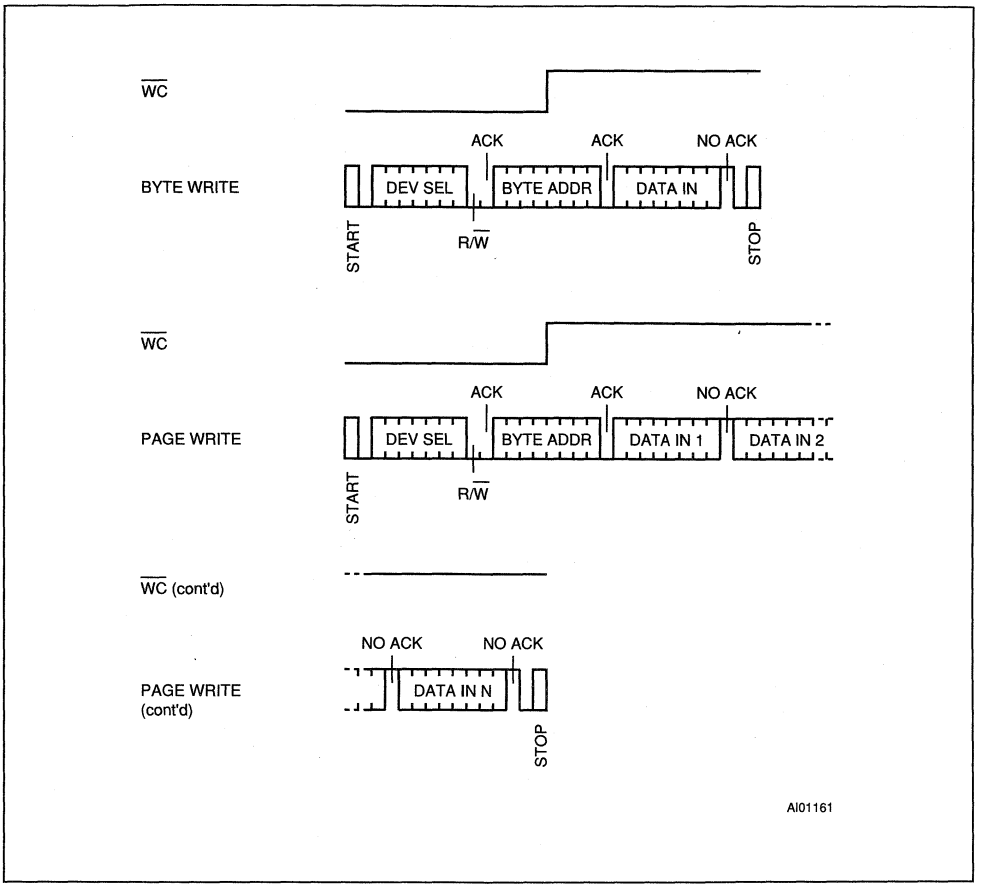
The sequence to follow to use the Write Protected feature is:

- write the data to be protected into the top of the memory, up to, but not including, location 3FFh;
- set the protection by writing the correct bottom boundary address, into location 3FFh, with bit b2 (Protect flag) set to '0'.

The area will now be protected when the PRE input is taken High.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 7 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 3FFh, by 7 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 16 bytes lower boundary of the protected area.

Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W08)



Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address is repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

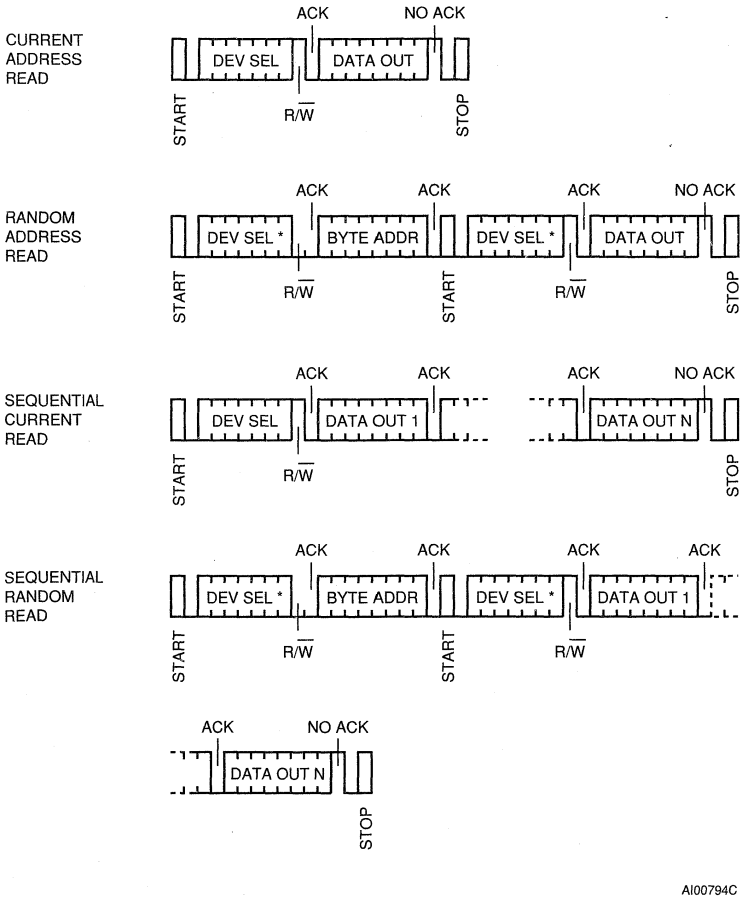
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the

DEVICE OPERATION (cont'd)

master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

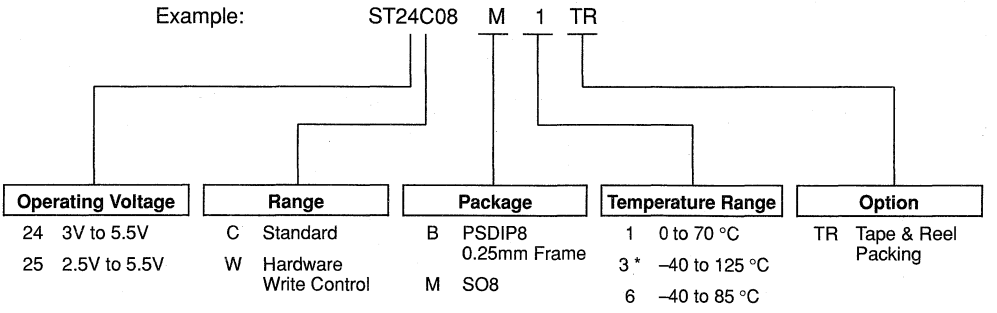
Acknowledge in Read Mode. In all read modes the ST24/25x08 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x08 terminate the data transfer and switches to a standby state.

Figure 11. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

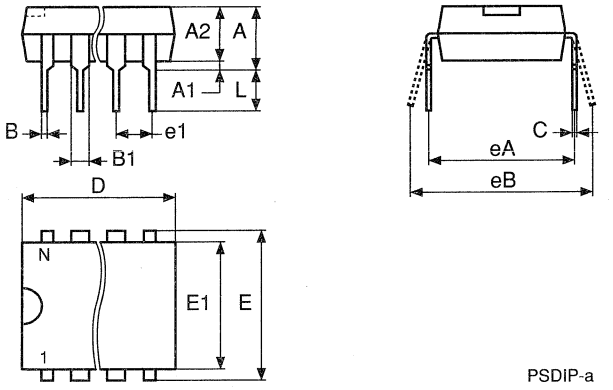
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



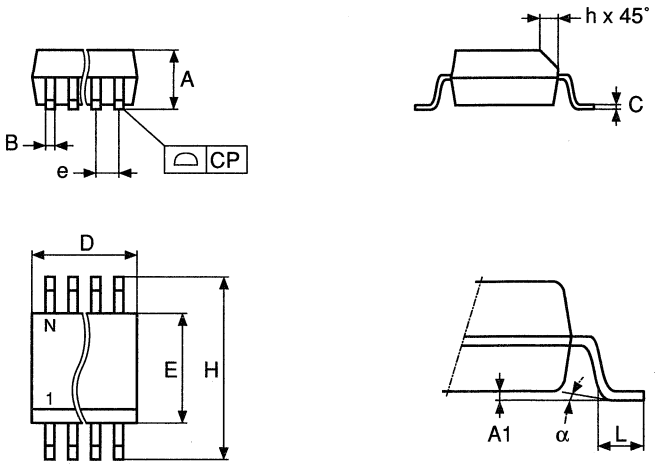
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



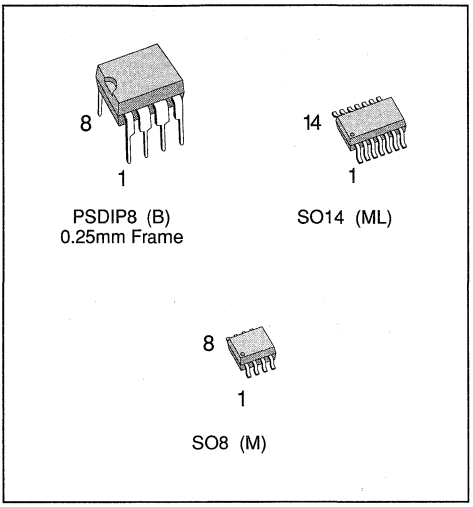
SO-a

Drawing is out of scale

ST24C16, ST25C16
ST24W16, ST25W16

SERIAL ACCESS 16K (2K x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES) for the ST24C16
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



DESCRIPTION

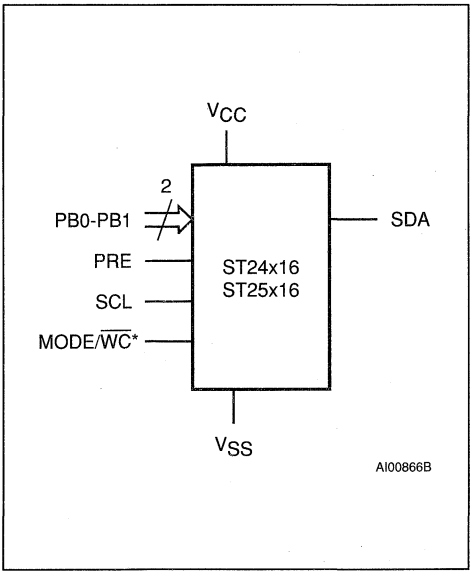
This specification covers a range of 16K bits I^2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured in SGS-THOMSON's Hi-Endurance Advanced

Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W16 products.

Figure 2A. DIP Pin Connections

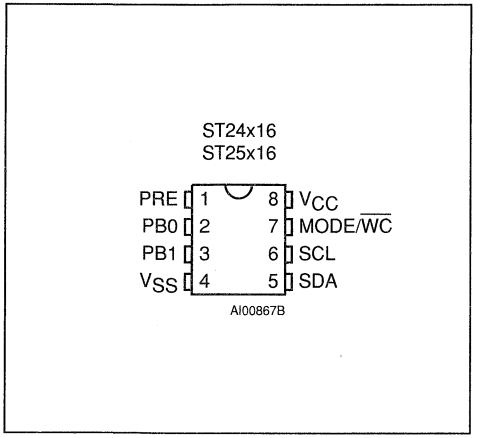
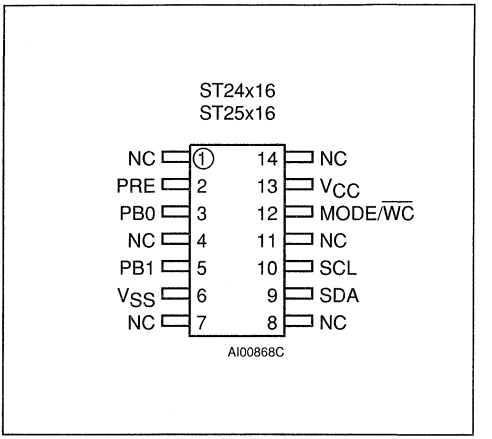
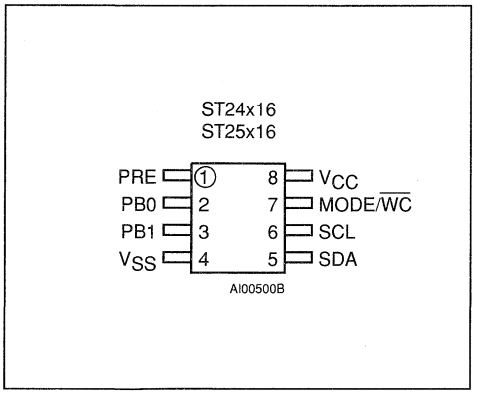


Figure 2B. SO14 Pin Connections



Warning: NC = No Connection

Figure 2C. SO8 Pin Connections



DESCRIPTION (cont'd)

CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 10 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memories behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the 4 upper blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PB1. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 and SO14) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

Table 3. Device Select Code

	Device Code				Memory MSB Addresses			$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	A10	A9	A8	$\overline{RW}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$\overline{RW}$ bit	MODE pin	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, $\overline{RW}$ = '0', Address,
	'1'			reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	X	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	X	1	START, Device Select, $\overline{RW}$ = '0'
Multibyte Write	'0'	V_{IH}	8	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, $\overline{RW}$ = '0'

Note: X = V_{IH} or V_{IL}.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input signal is used to synchronise all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA signal is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Protected Block Select (PB0, PB1). PB0 and PB1 input signals select the block in the upper part of the memory where write protection starts. These inputs have a CMOS compatible input level.

Protect Enable (PRE). The PRE input signal, in addition to the status of the Block Address Pointer bit (b2, location 7FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature is offered only for ST24W16 and ST25W16 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}. The devices with this Write Control feature no longer supports the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

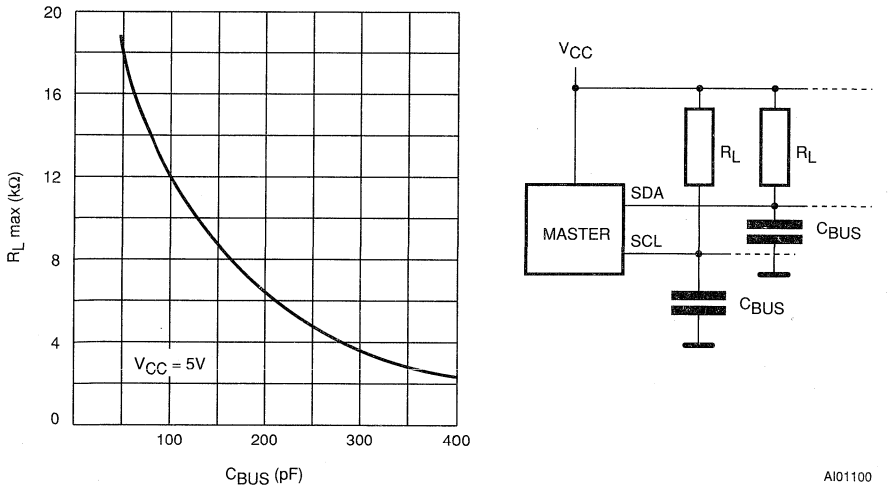


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W16)	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W16)	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

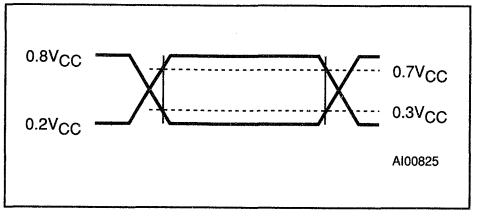
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (2)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (5 address MSB are not constant) the maximum programming time is doubled to 20ms.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION

I²C Bus Background

The ST24/25x16 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x16 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x16 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 5. AC Waveforms

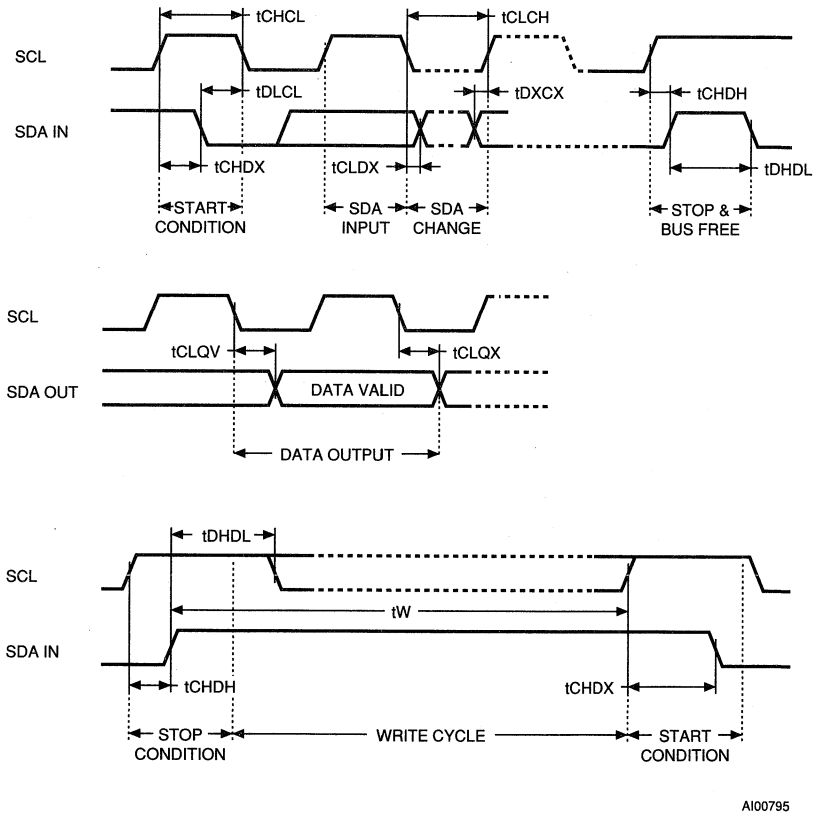
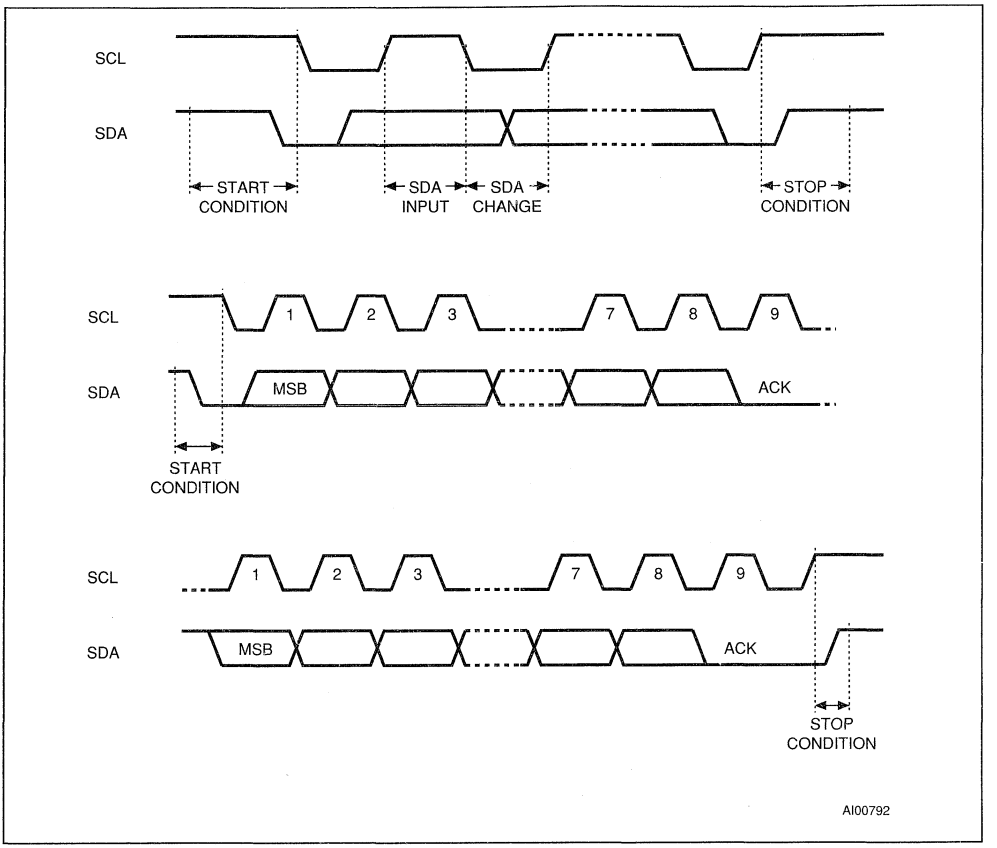


Figure 6. I²C Bus Protocol



Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x16 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

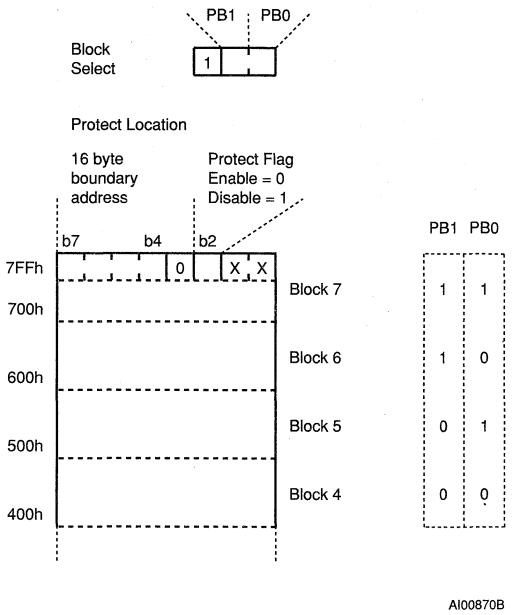
Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x16 samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x16, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifie the device type (1010), 3 Block select bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Figure 7. Memory Protection



Write Operations

The Multibyte Write mode (only available on the ST24/25C16 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes of one memory block. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W16 versions, any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 10.

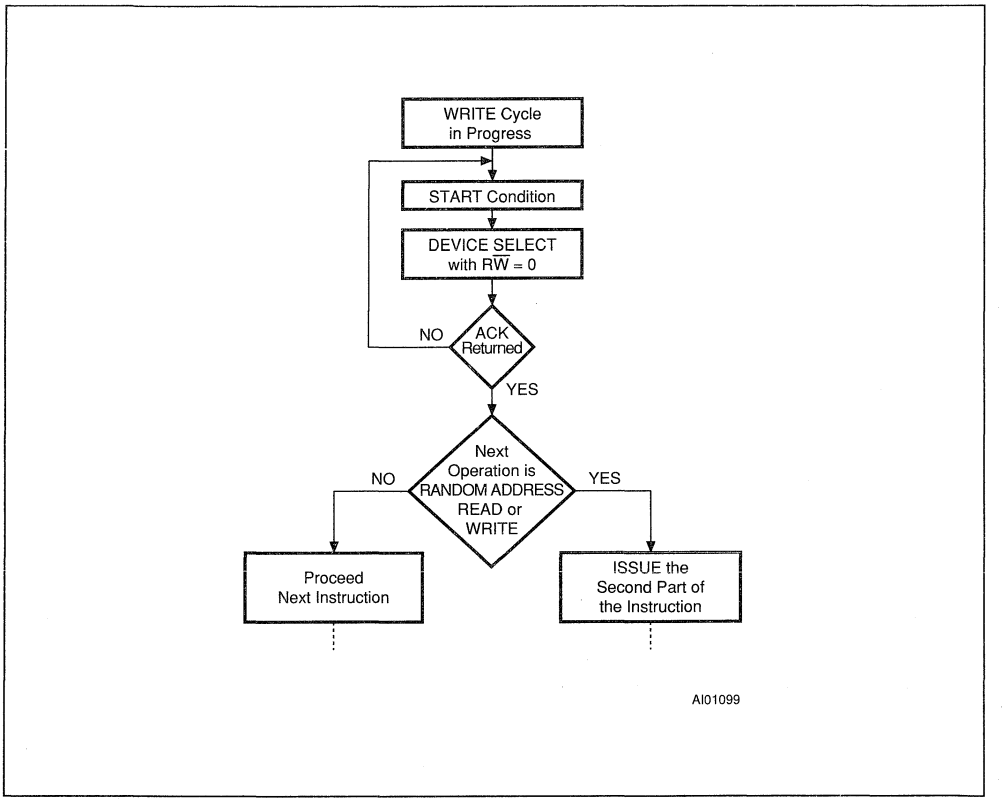
Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write (ST24/25C16 only). For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 contiguous rows (one row is 16 bytes), the programming time is then doubled to a maximum of 20ms. Writing more than 8 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 16 bytes long). However, the Multibyte Write can properly write up to 16 consecutive bytes only if the first address of these 16 bytes is the first address of the row, the 15 following bytes being written in the 15 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the same Block Address bits (b3, b2, b1 of Device Select code in Table 3) and the same 4 MSBs in the Byte Address. The master sends one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

Figure 8. Write Cycle Polling using ACK



The sequence is:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is internally writing, no ACK will be returned. The Master goes back to Step1. If the memory has terminated the internal writing, it will issue an ACK indicating that the memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Write Protection. Data in the upper four blocks of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 7FFh). The boundary address is user defined by writing a value in the Block Address Pointer (location 7FFh).

This Block Address Pointer defines an 8 bit address composed of the 4 MSBs of location 7FFh and 4 LSBs which are forced to '0'. This address pointer can therefore address a boundary in steps of 16 bytes.

The block in which the Block Address Pointer defines the boundary of the write protected memory is defined by the logic level on the PB1 and PBO inputs:

- PB1 = '0' and PB0 = '0' select block 4
- PB1 = '0' and PB0 = '1' select block 5
- PB1 = '1' and PB0 = '0' select block 6
- PB1 = '1' and PB0 = '1' select block 7

To use the Write Protected feature follow this sequence:

- write the data to be protected into the top of the memory, up to, but not including, location 7FFh;
- select the block by hardwiring the signals PB0 & PB1;
- and set the protection by writing the correct bottom boundary address into location 7FFh.

The area will now be protected when the PRE input is taken High.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 7 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 7FFh, by 7 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 16 bytes lower boundary of the protected area.

Figure 9. Write Modes Sequence (ST24/25C16)

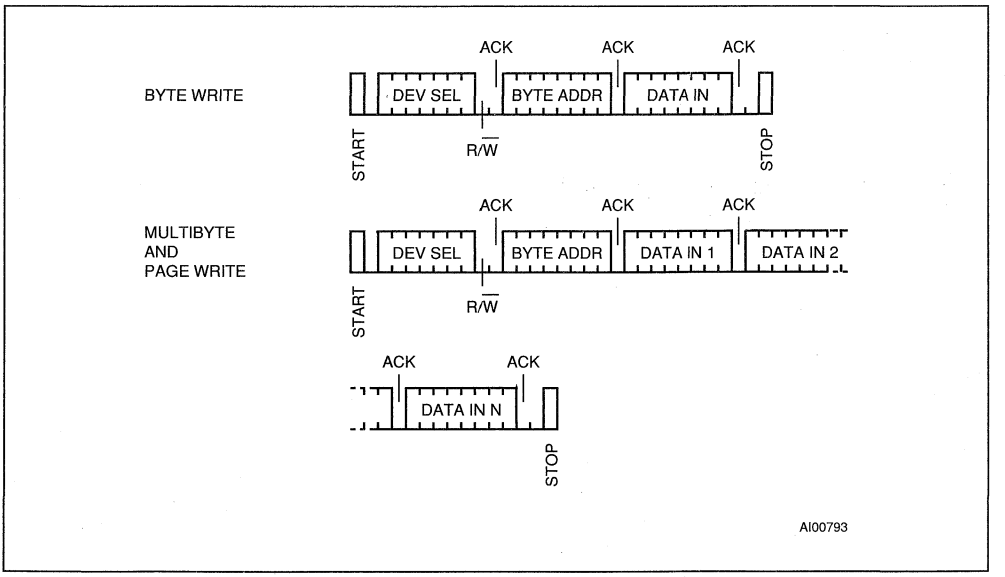
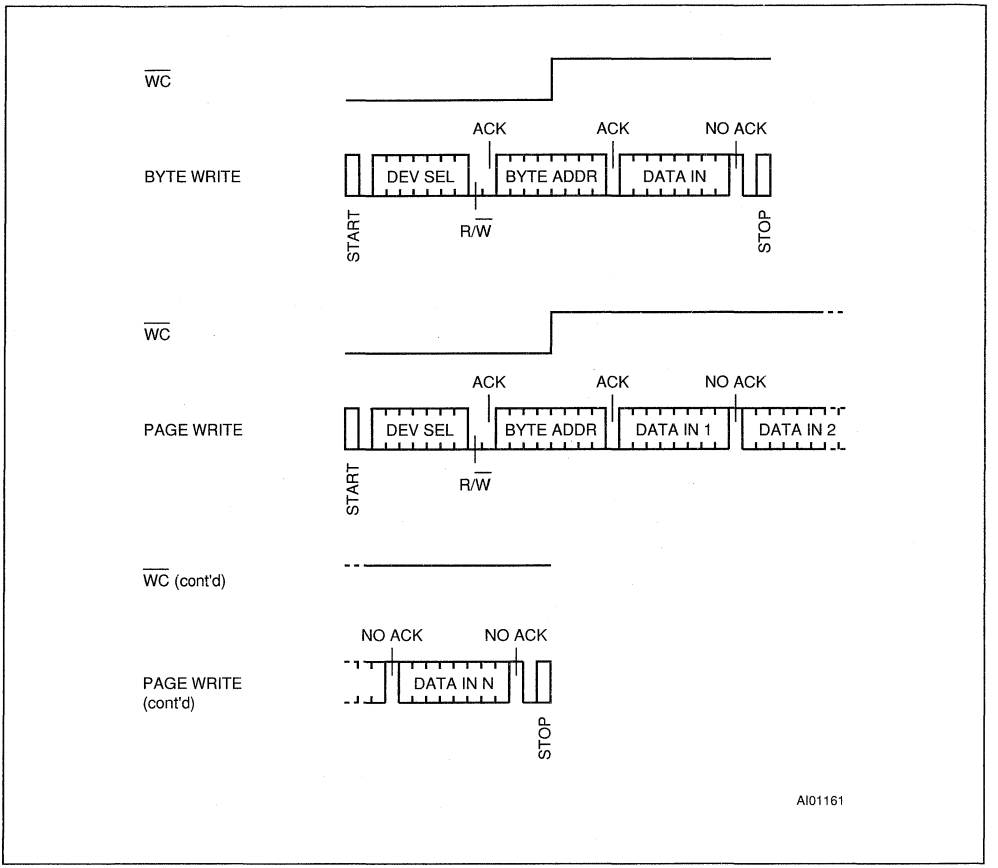


Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W16)



Read Operation

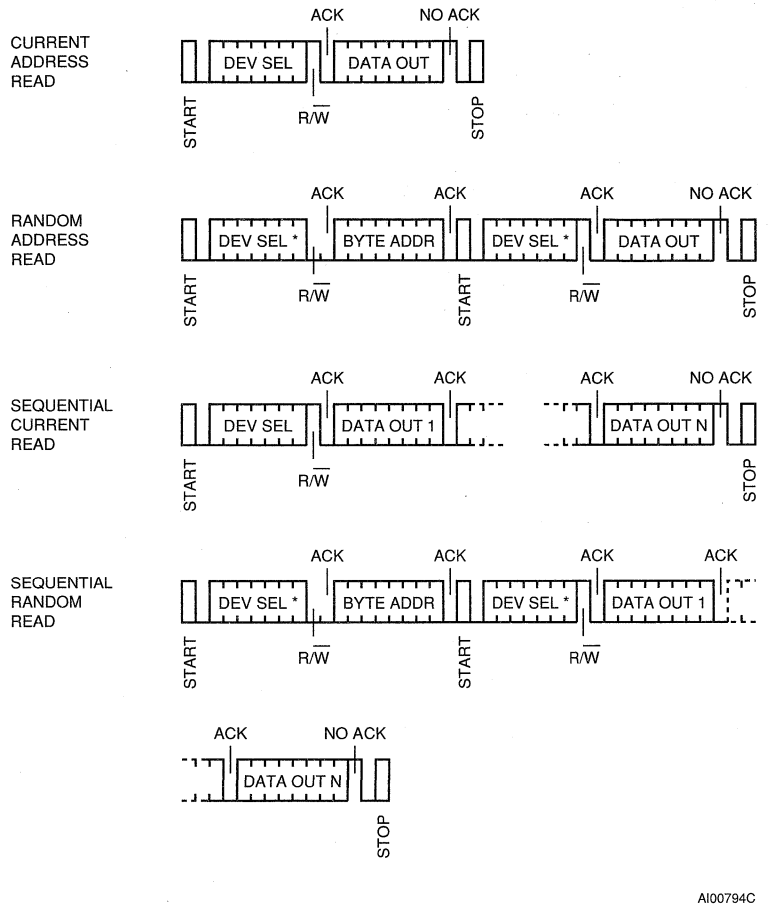
Read operations are independent of the state of the MODE signal. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte out-

Figure 11. Read Modes Sequence

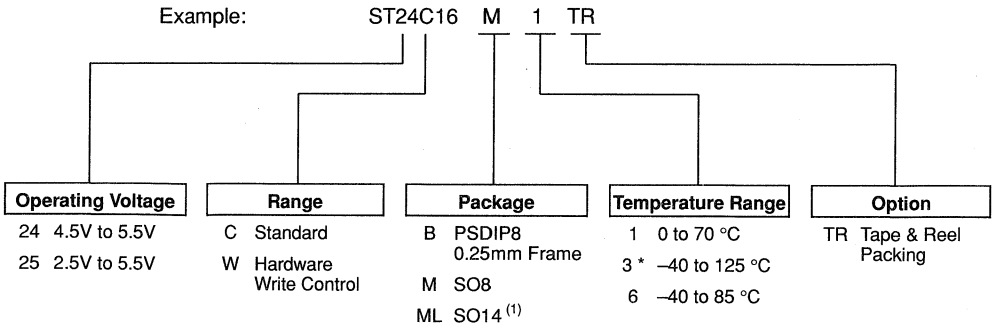


Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

put, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x16 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x16 terminate the data transfer and switches to a standby state.

ORDERING INFORMATION SCHEME



Notes: 1. Not for new designs.
3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

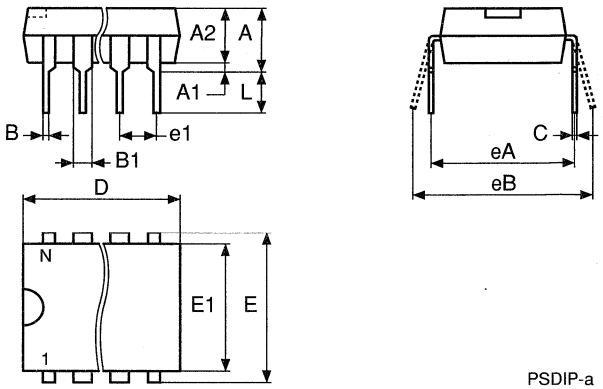
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



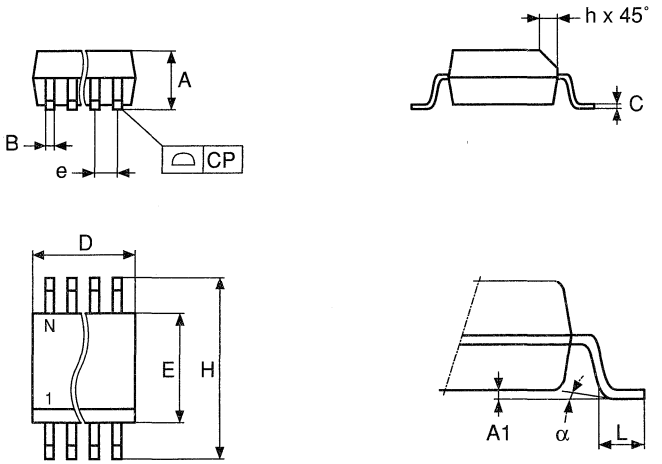
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



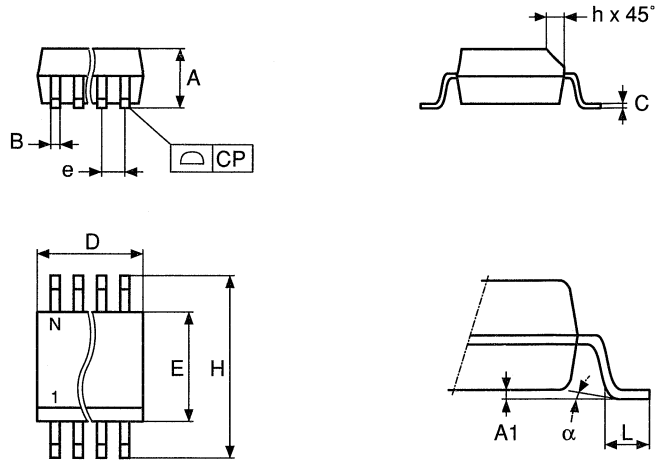
SO-a

Drawing is out of scale

SO14 - 14 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		8.55	8.75		0.337	0.344
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.80		0.016	0.031
α		0°	8°		0°	8°
N	14			14		
CP			0.10			0.004

SO14



SO-a

Drawing is out of scale

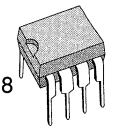
SERIAL ACCESS
XI^{2}C BUS EEPROM

SGS-THOMSON MICROELECTRONICS

ST24E16
ST25E16

SERIAL ACCESS EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS 16K (2K x 8) EEPROM

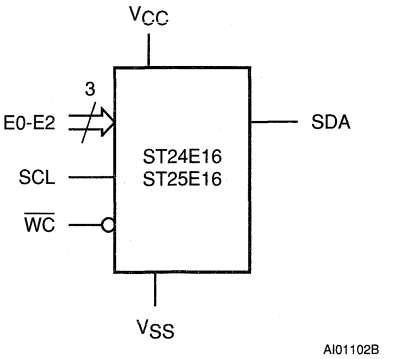
- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for ST24E16 version
  - 2.5V to 5.5V for ST25E16 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of over 10 years. The ST25E16 operates with a power supply value as low as 2.5V.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

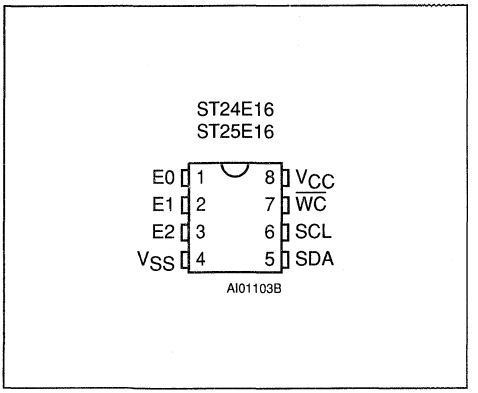


Figure 2B. SO Pin Connections

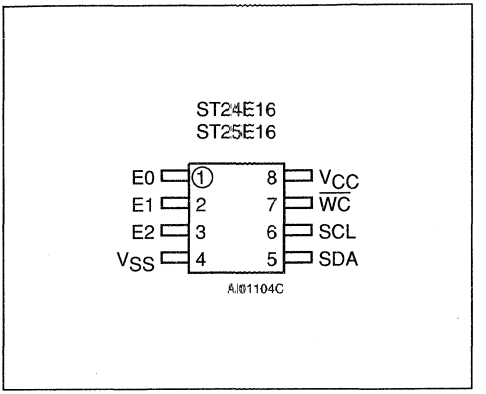


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages		–0.3 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E16 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E16 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	$\overline{RW}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	$\overline{RW}$ bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	1	START, Device Select, $\overline{RW}$ = '0', Address,
	'1'		reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	16	START, Device Select, $\overline{RW}$ = '0'

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E16 may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 128 Kbit.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

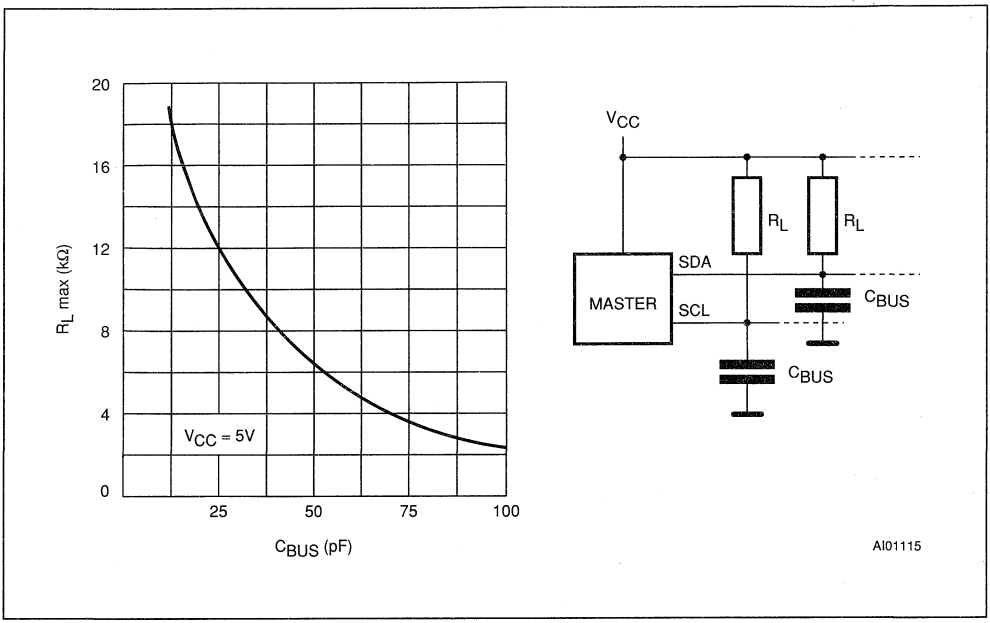
Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. The devices with this Write Control feature no longer supports the multibyte mode of operation. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} (see Table 5).

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acnowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus, f_C = 400kHz



DEVICE OPERATION

I^2C Bus Background

The ST24/25E16 support the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver.The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E16 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E16 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E16 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E16 sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E16, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 ° or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (ST25 series)			1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

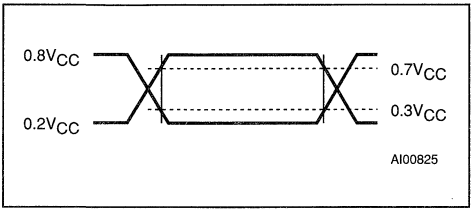
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL1} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b10,b9,b8 of the Most Significant Byte select one block among 8 blocks (one block is 256 bytes).

Most Significant Byte

X	X	X	X	X	b10	b9	b8

X = Don't Care.

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

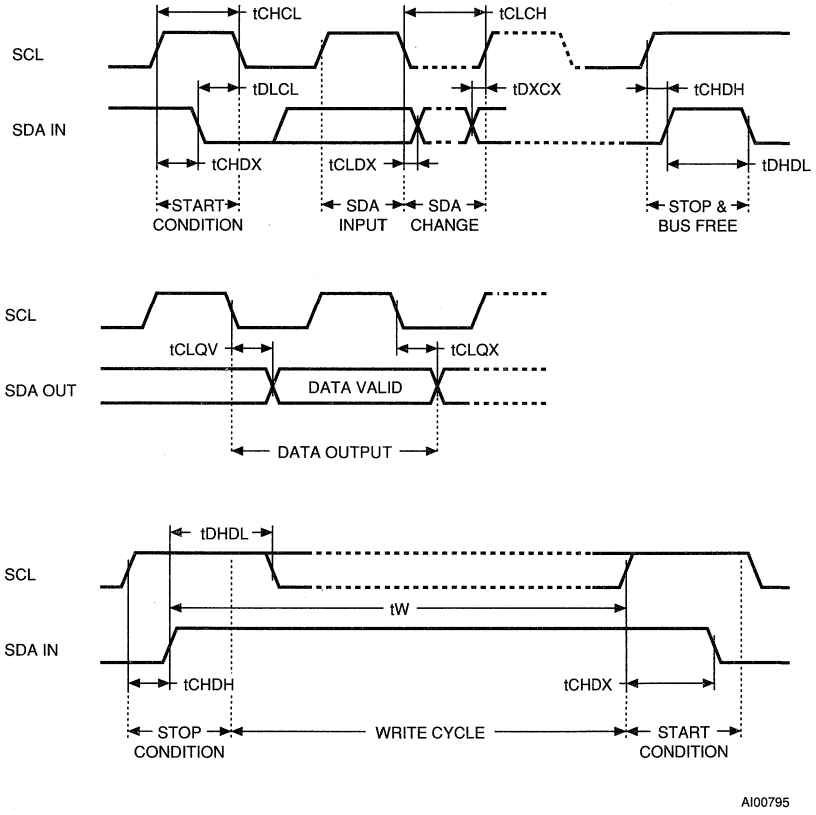
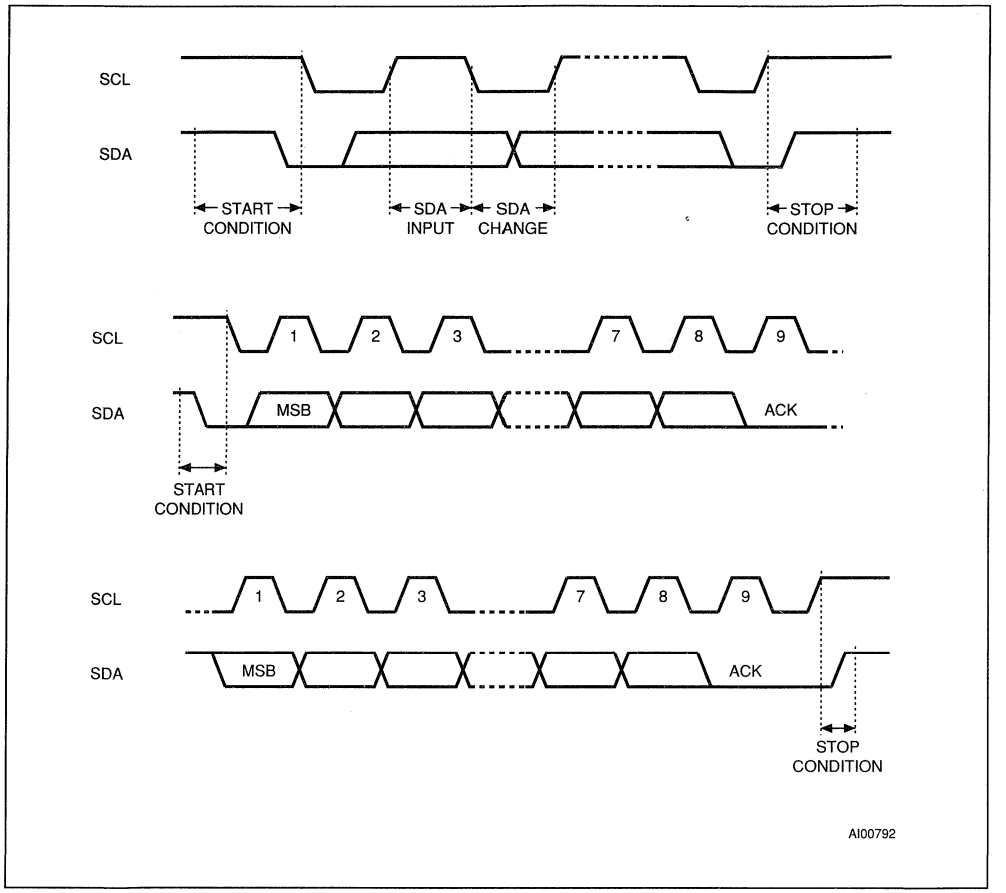


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the RW bit reset to '0'. The ST24/25E16 acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 8 blocks of 256 bytes each. Writing in the ST24/25E16 may be inhibited if input pin WC is taken high.

For the ST24/25E16 versions, any write command with WC = '1' (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E16. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same row of 16 bytes in the memory, that is the same Address bits (b10-b4). The master sends one up to 16 bytes of data, which are each acknowledged by the ST24/25E16. After each byte is transfered, the internal byte address counter (4 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which

could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24/25E16 will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E16 disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E16 are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E16 have terminated the internal writing, it will issue an ACK. The ST24/25E16 are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK

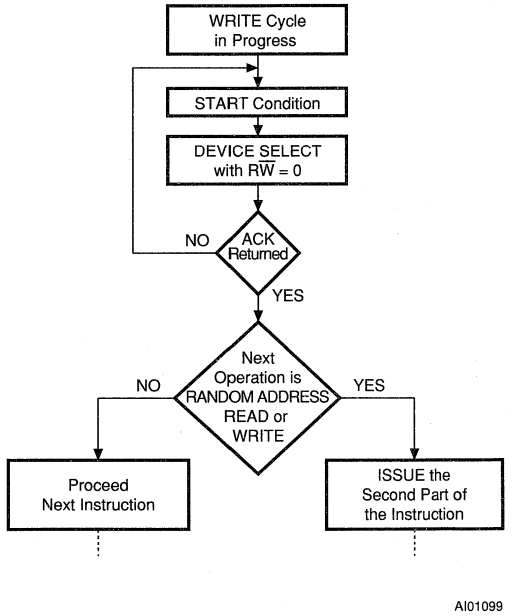
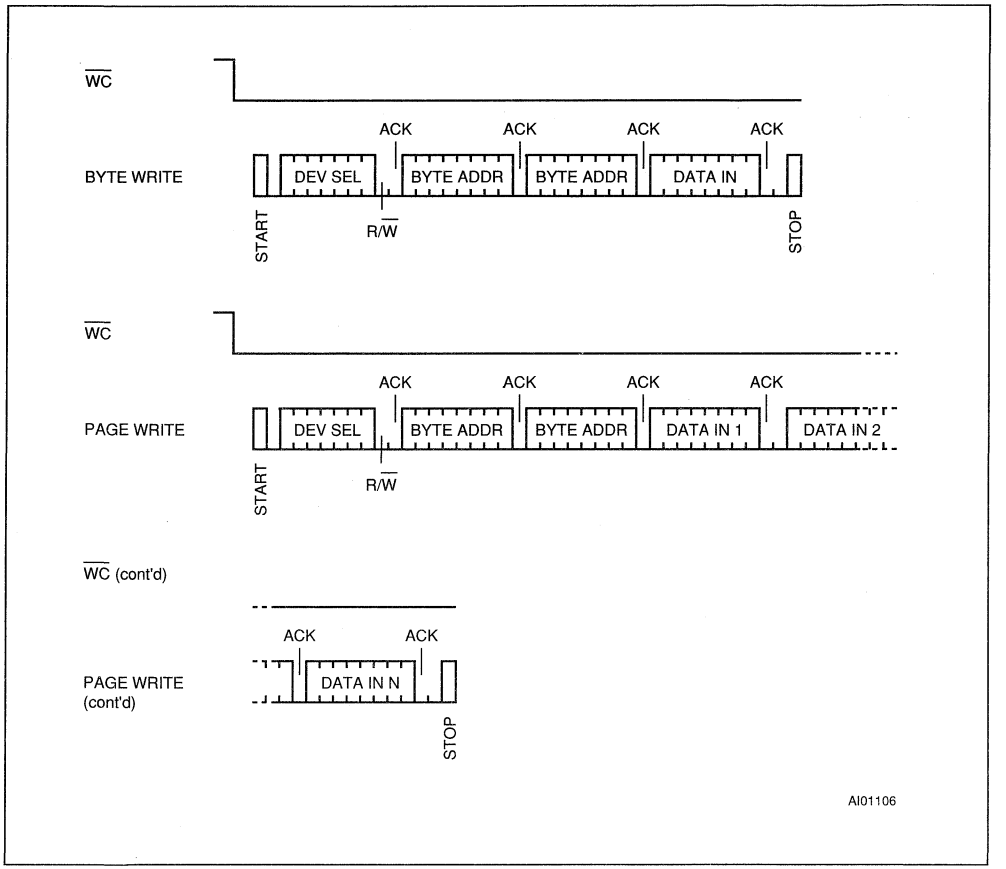


Figure 8. Write Modes Sequence with Write Control = 0



Read Operations

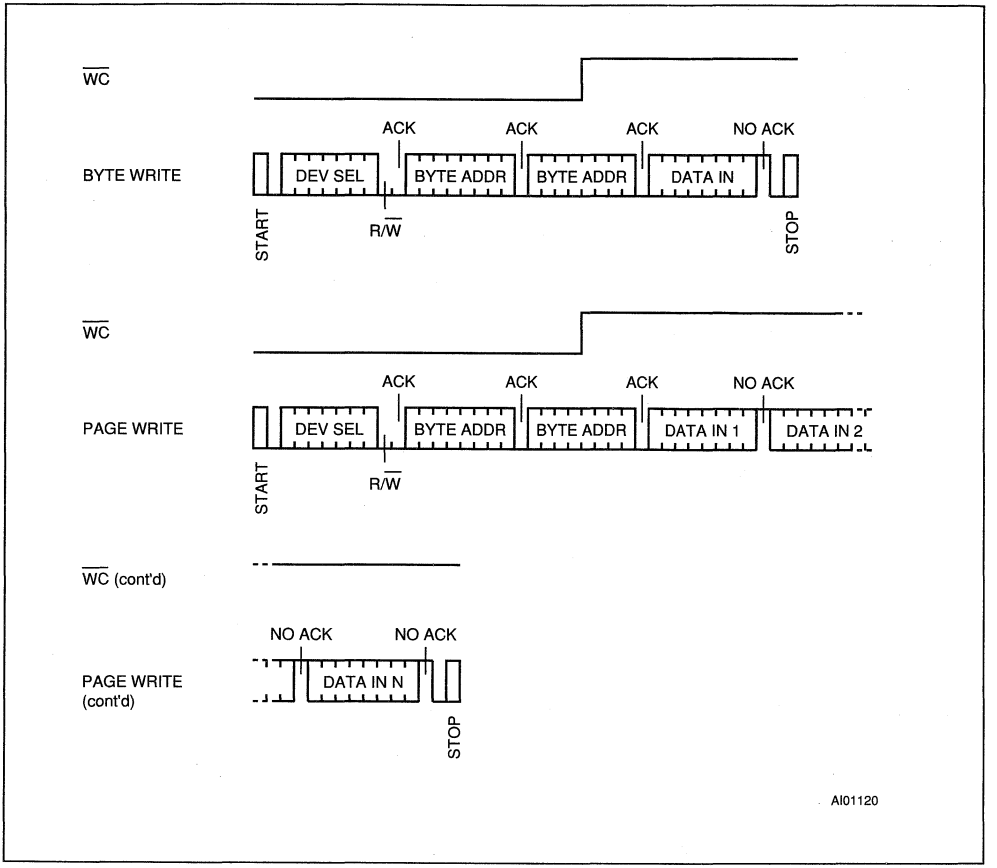
On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E16 have an internal 11 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the R/W bit set to '1'. The ST24/25E16 acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The ST24/25E16 acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E16 continue to output the next byte in

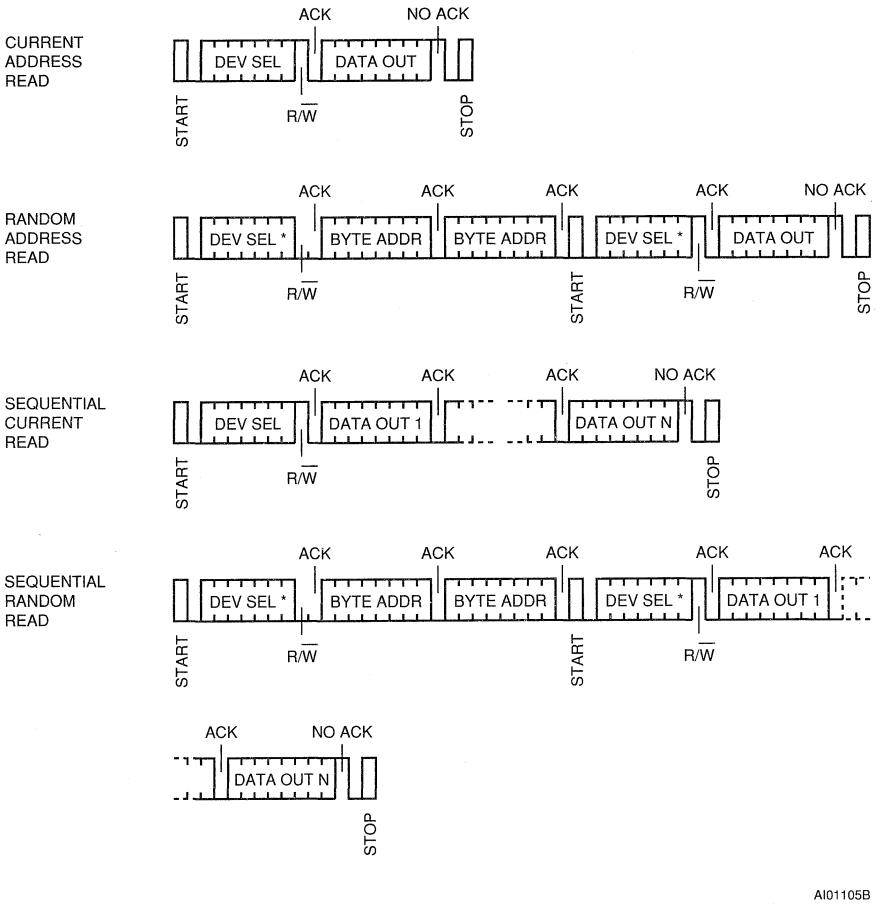
Figure 9. Write Modes Sequence with Write Control = 1



sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

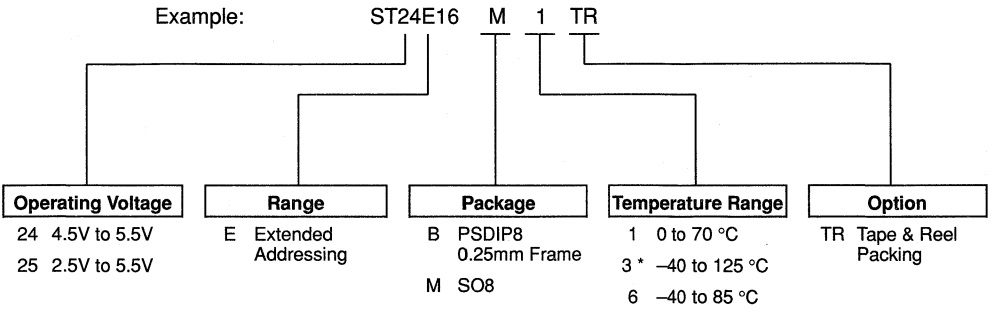
Acknowledge in Read Mode. In all read modes the ST24/25E16 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E16 terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

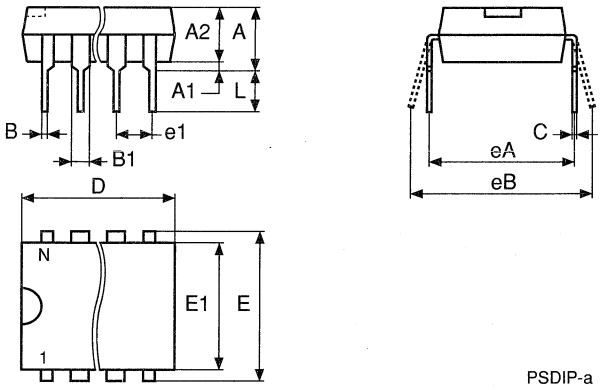
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



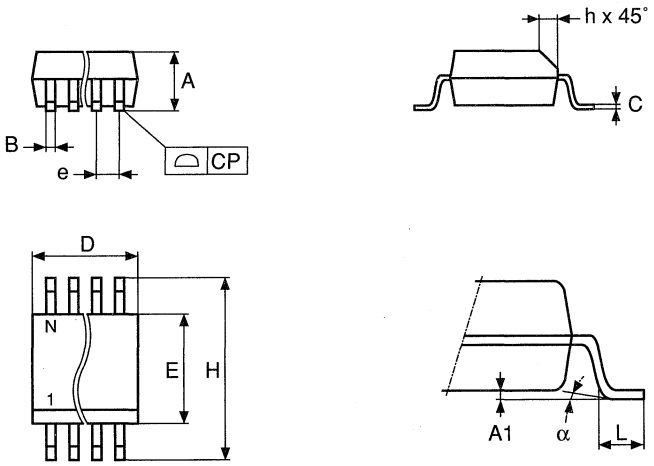
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		9.42	9.79		0.371	0.385
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8

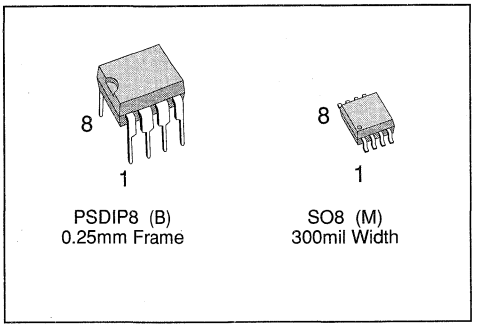


SO-a

Drawing is out of scale

SERIAL ACCESS EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS 32K (4K x 8) EEPROM

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 100,000 ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for ST24E32 version
  - 2.5V to 5.5V for ST25E32 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



DESCRIPTION

The ST24/25E32 are 32K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 512 x 8 bits. The ST25E32 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

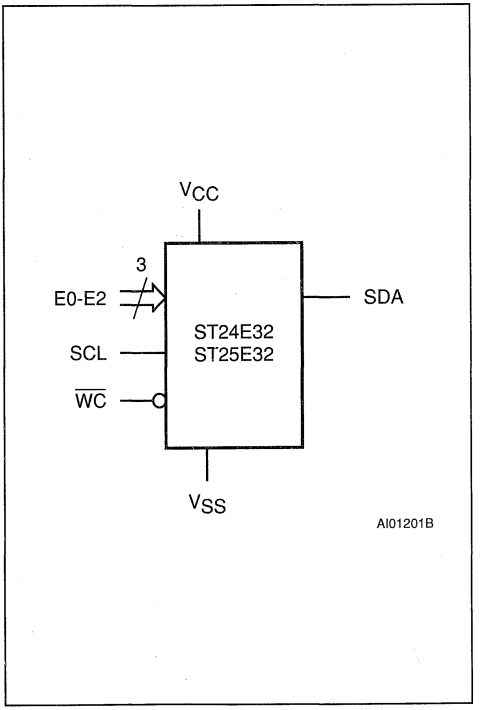


Figure 2A. DIP Pin Connections

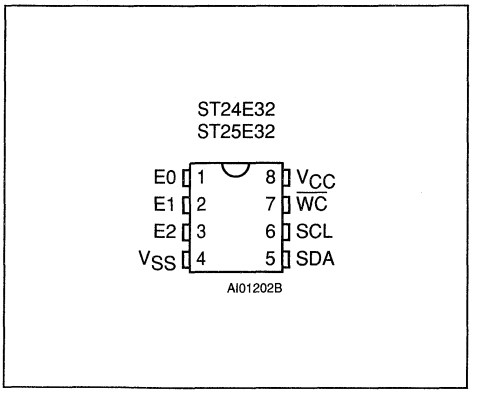


Figure 2B. SO Pin Connections

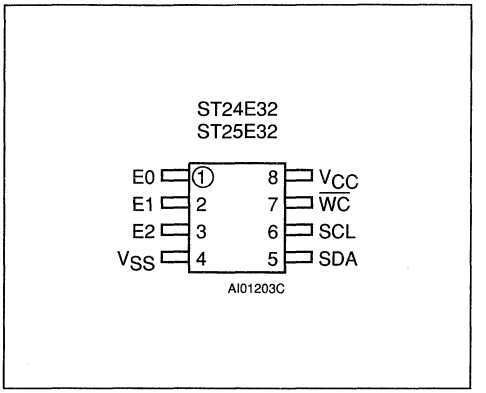


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E32 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E32 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, RW = '1'
Random Address Read	'0'	1	START, Device Select, RW = '0', Address,
	'1'		reSTART, Device Select, RW = '1'
Sequential Read	'1'	1 to 4096	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, RW = '0'
Page Write	'0'	32	START, Device Select, RW = '0'

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E32 may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 256 Kbit.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

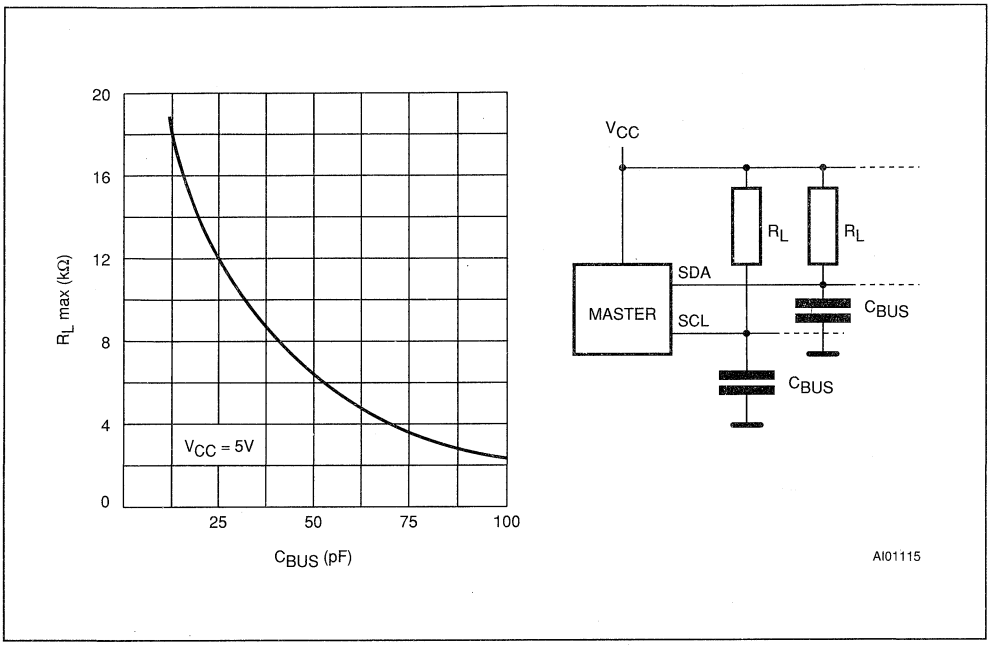
Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as V_{IL} (see Table 5).

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus, f_C = 400kHz



DEVICE OPERATION

I^2C Bus Background

The ST24/25E32 support the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E32 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E32 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E32 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E32 sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E32, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (ST25 series)			1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

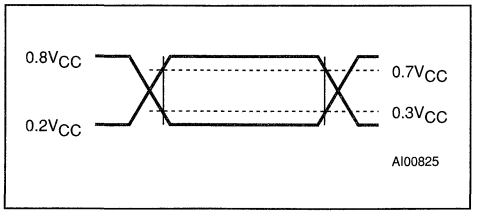
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL1} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b11,b10,b9,b8 of the Most Significant Byte select one block among 16 blocks (one block is 256 bytes).

Most Significant Byte

X	X	X	X	b11	b10	b9	b8

X = Don't Care

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

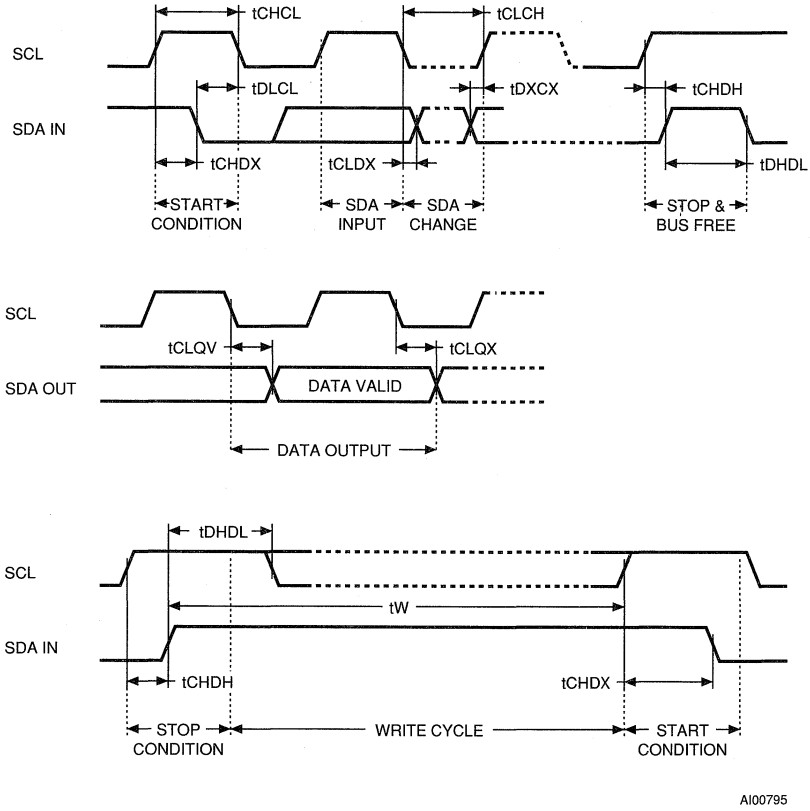
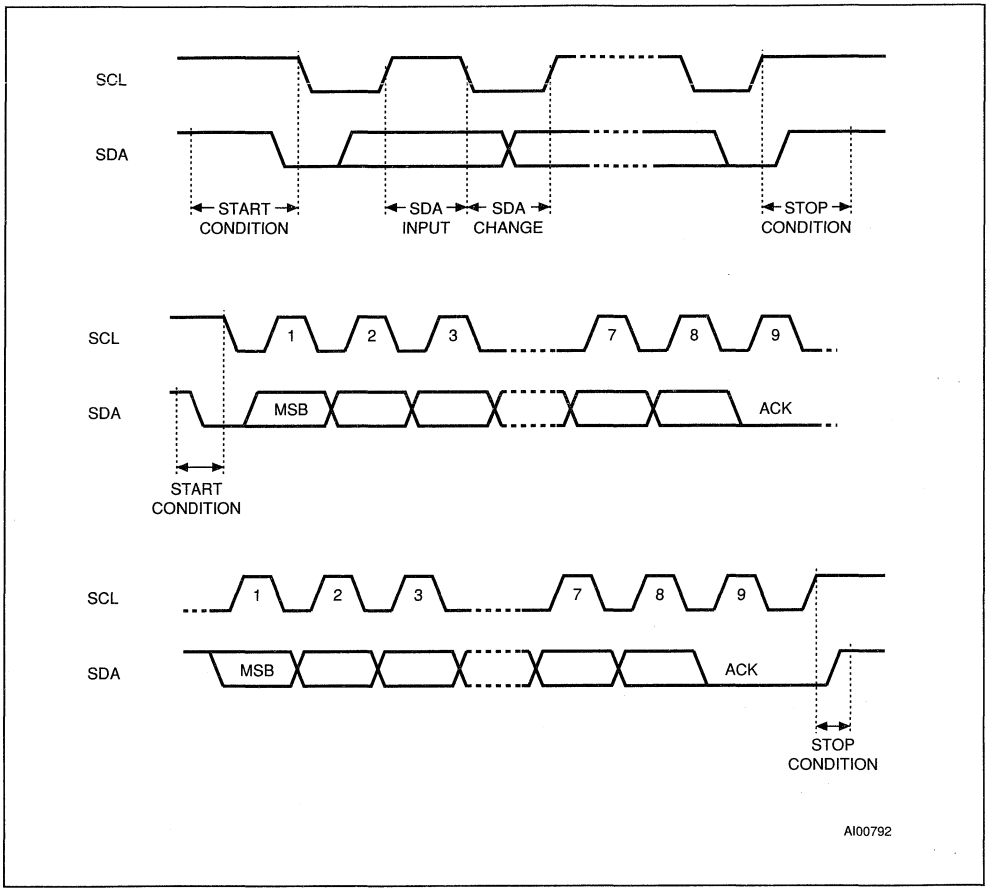


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the RW bit reset to '0'. The ST24/25E32 acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 16 blocks of 256 bytes each. Writing in the ST24/25E32 may be inhibited if input pin $\overline{WC}$ is taken high.

For the ST24/25E32 versions, any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E32. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same row of 32 bytes in the memory, that is the same Address bits (b11 to b5). The master sends one up to 32 bytes of data, which are each acknowledged by the ST24/25E32. After each byte is transfered, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory pro-

gram cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the ST24/25E32 will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E32 disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E32 are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E32 have terminated the internal writing, it will issue an ACK. The ST24/25E32 are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK

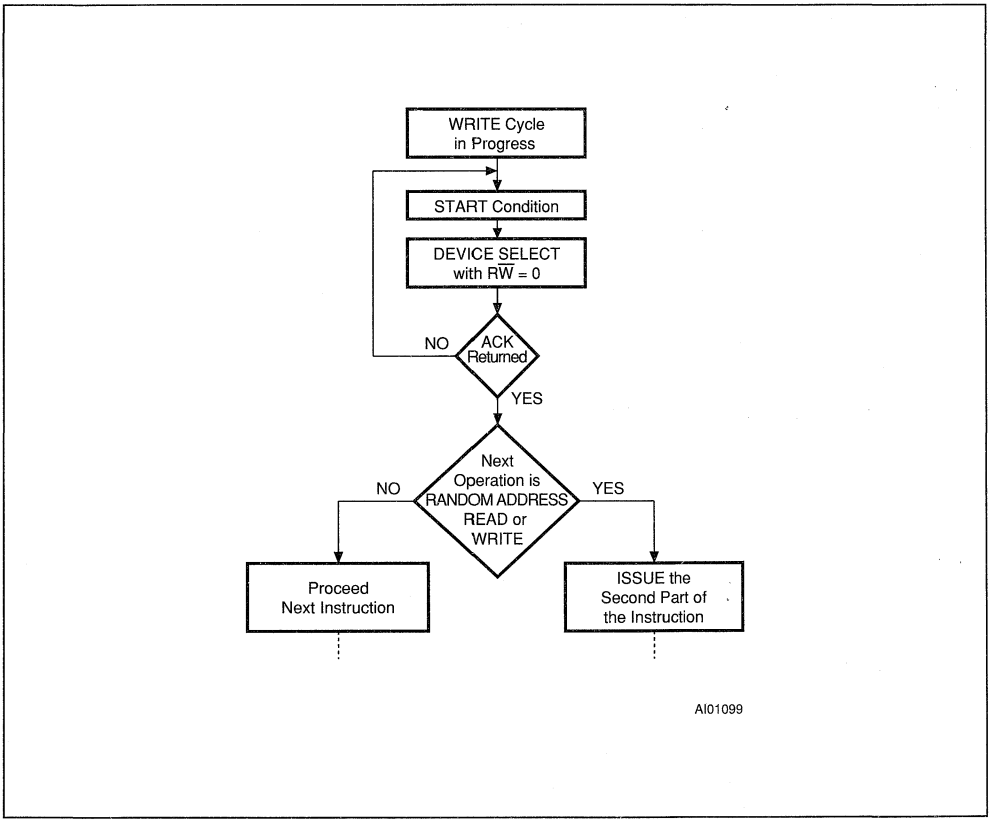
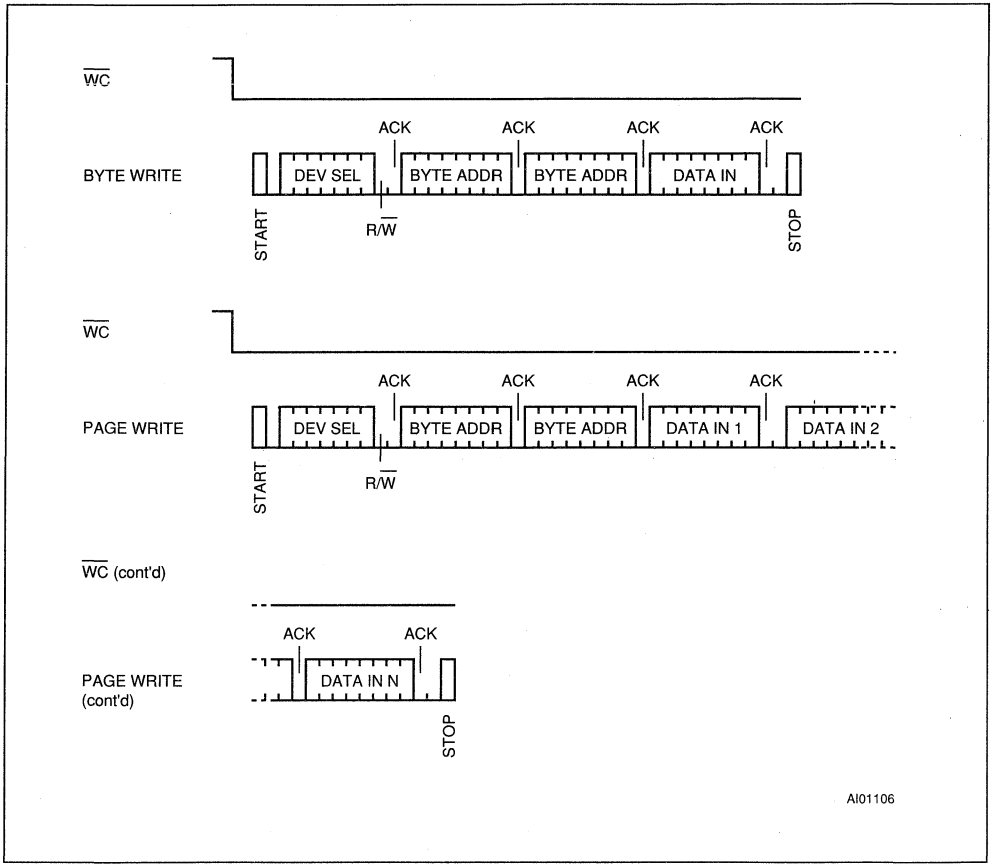


Figure 8. Write Modes Sequence with Write Control = 0



Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E32 have an internal 12 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the R/W bit set to '1'. The ST24/25E32 acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The ST24/25E32 acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

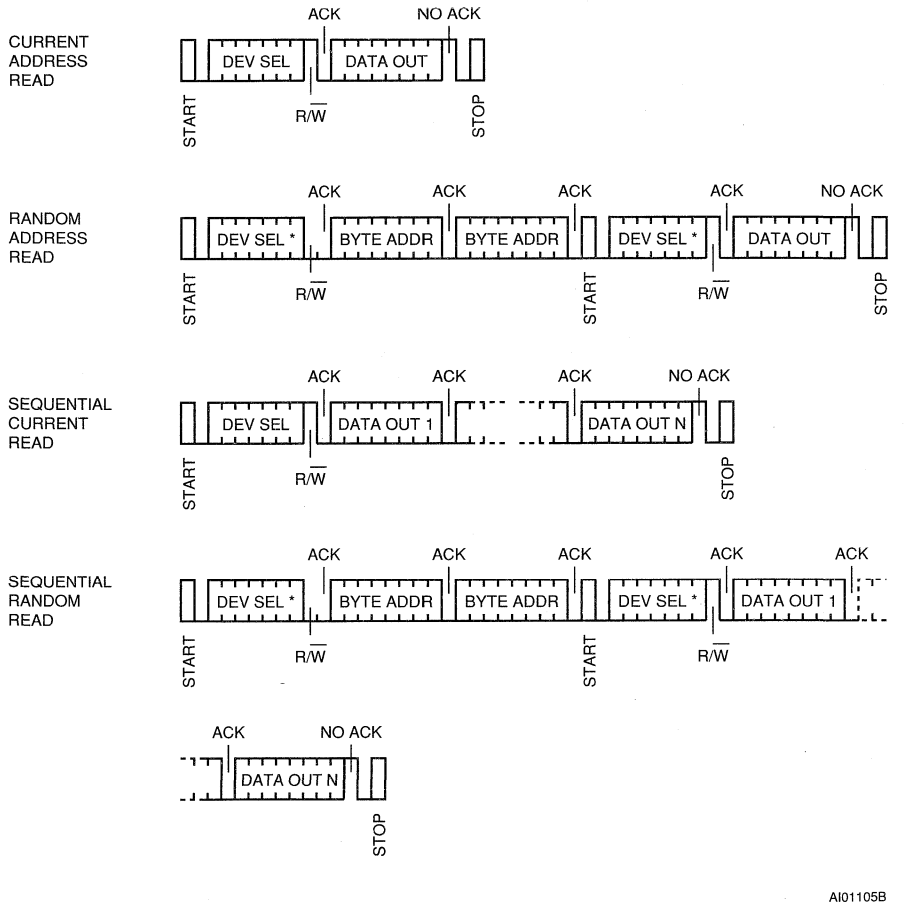
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E32 continue to output the next byte in

Figure 9. Write Modes Sequence with Write Control = 1

sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

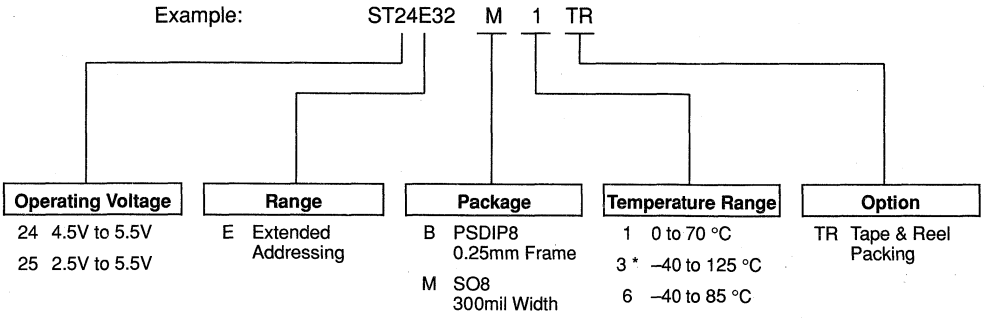
Acknowledge in Read Mode. In all read modes the ST24/25E32 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E32 terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature Range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

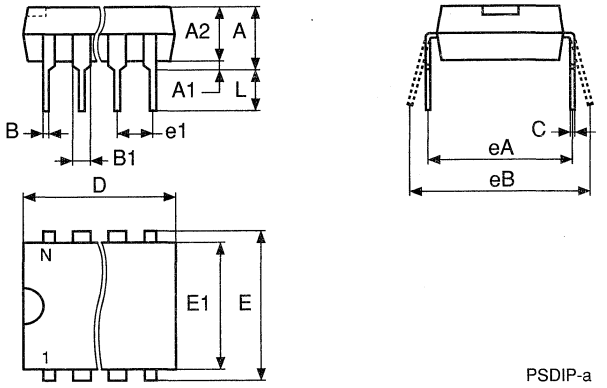
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



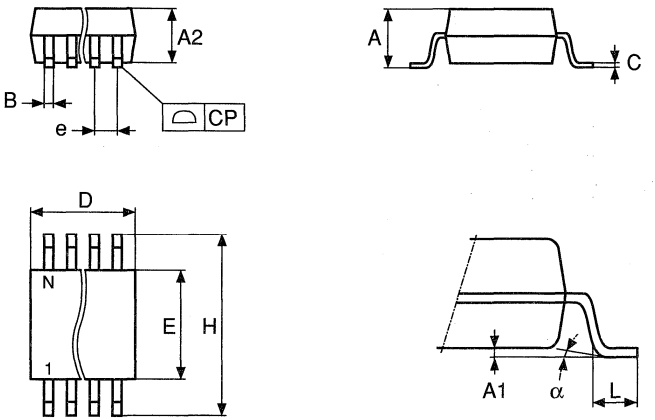
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 300 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N		8			8	
CP			0.10			0.004

SO8



SO-b

Drawing is out of scale

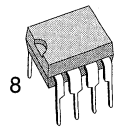
SGS-THOMSON MICROELECTRONICS

ST24E64
ST25E64

SERIAL ACCESS EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS 64K (8K x 8) EEPROM

PRELIMINARY DATA

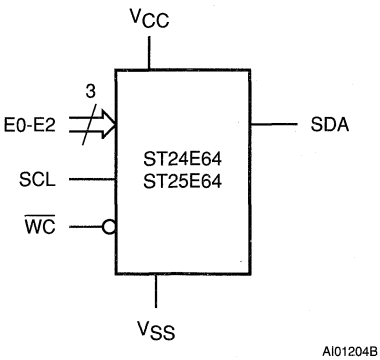
- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 100,000 ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for ST24E64 version
  - 2.5V to 5.5V for ST25E64 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
300mil Width

Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E64 are 64K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 1024 x 8 bits. The ST25E64 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

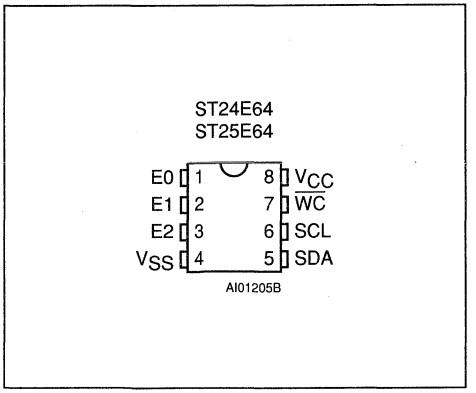


Figure 2B. SO Pin Connections

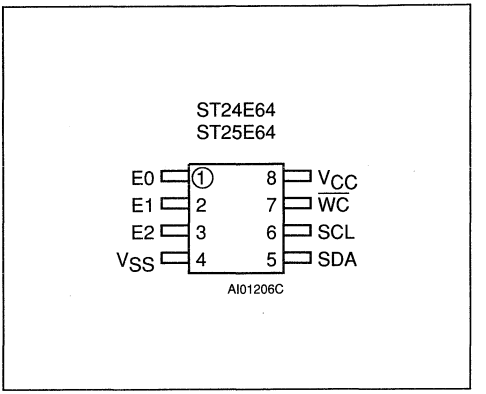


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E64 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E64 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, RW = '1'
Random Address Read	'0'	1	START, Device Select, RW = '0', Address,
	'1'		reSTART, Device Select, RW = '1'
Sequential Read	'1'	1 to 8192	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, RW = '0'
Page Write	'0'	32	START, Device Select, RW = '0'

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E64 may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 512 Kbit.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

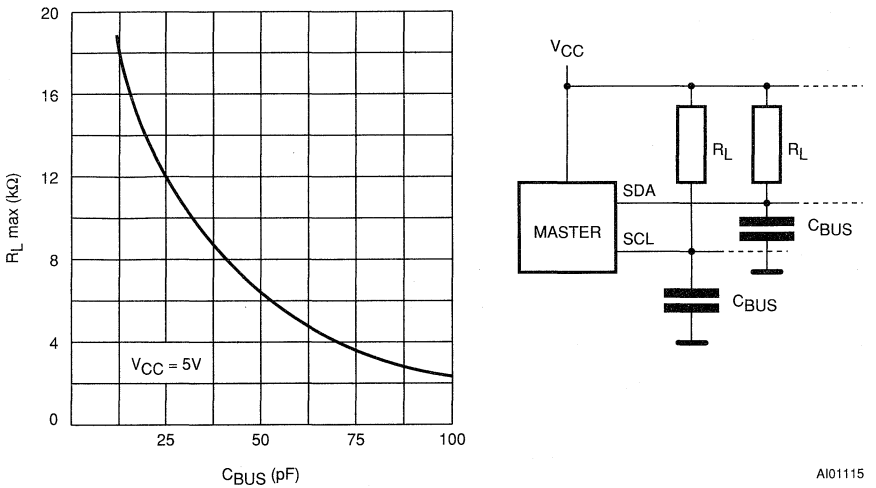
Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as V_{IL} (see Table 5).

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus, f_C = 400kHz



DEVICE OPERATION

I^2C Bus Background

The ST24/25E64 support the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E64 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E64 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E64 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E64 sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E64, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = –40 to 85 °C or 0 to 70 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (ST25 series)			1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = –40 to 85 °C or 0 to 70 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

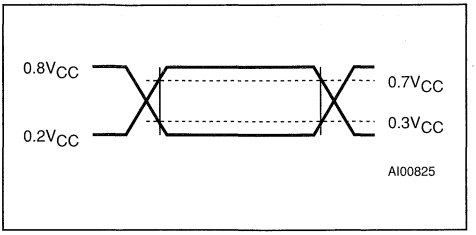
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL1} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b12,b11,b10,b9,b8 of the Most Significant Byte select one block among 32 blocks (one block is 256 bytes).

Most Significant Byte

X	X	X	b12	b11	b10	b9	b8

X = Don't Care.

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

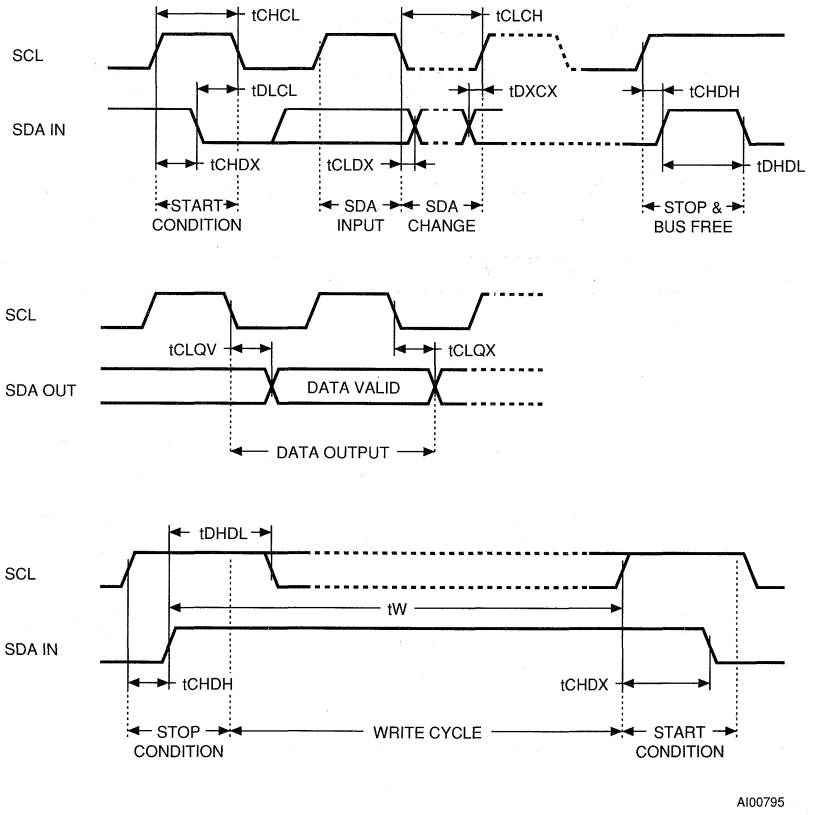
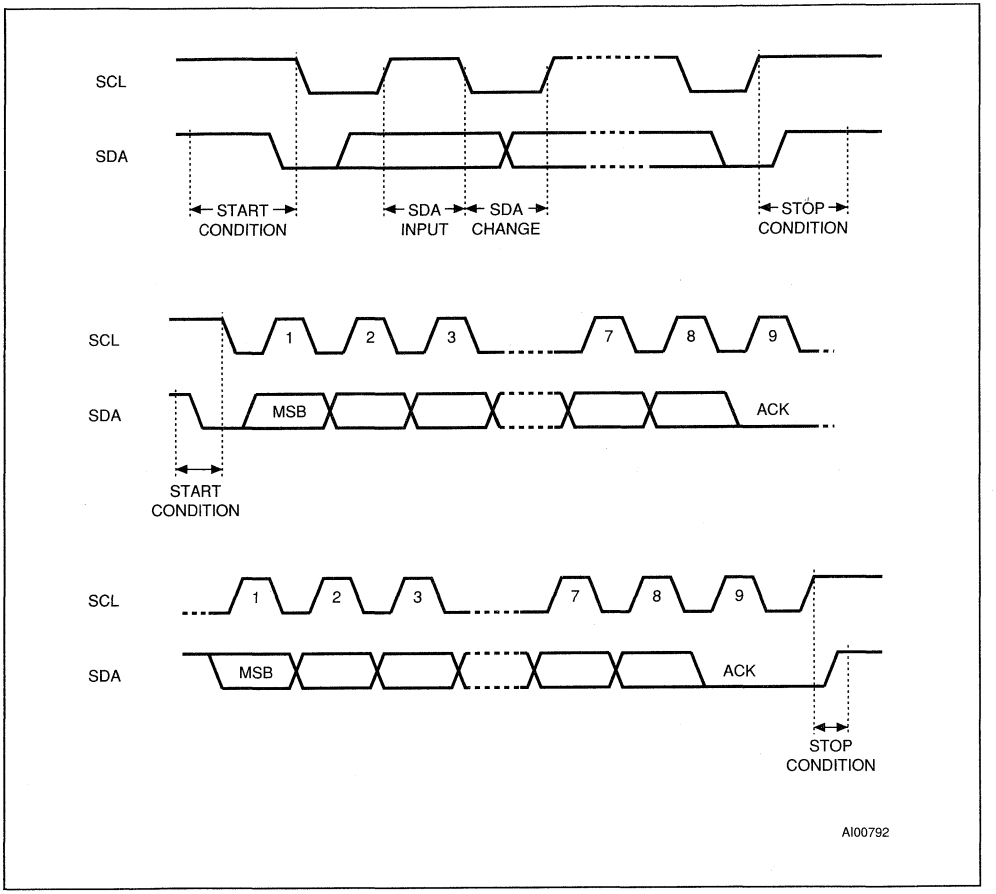


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the R$\overline{W}$ bit reset to '0'. The ST24/25E64 acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 32 blocks of 256 bytes each. Writing in the ST24/25E64 may be inhibited if input pin $\overline{WC}$ is taken high.

For the ST24/25E64 versions, any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E64. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same row of 32 bytes in the memory, that is the same Address bits (b12 to b5). The master sends one up to 32 bytes of data, which are each acknowledged by the ST24/25E64. After each byte is transfered, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory pro-

gram cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the ST24/25E64 will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E64 disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E64 are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E64 have terminated the internal writing, it will issue an ACK. The ST24/25E64 are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK

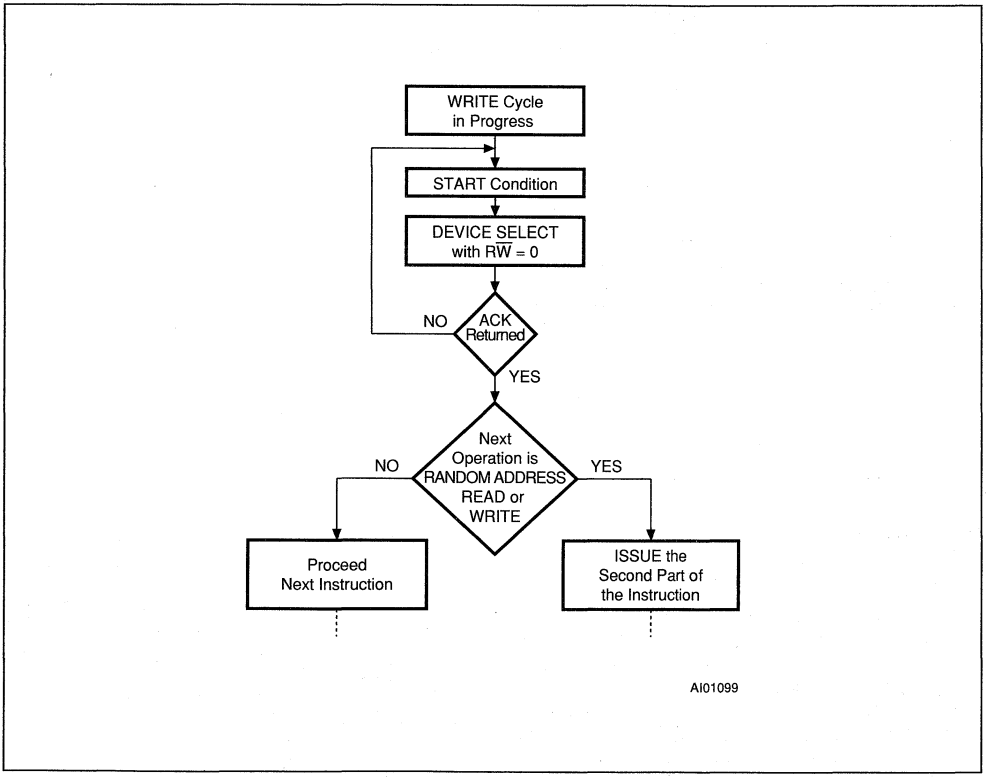
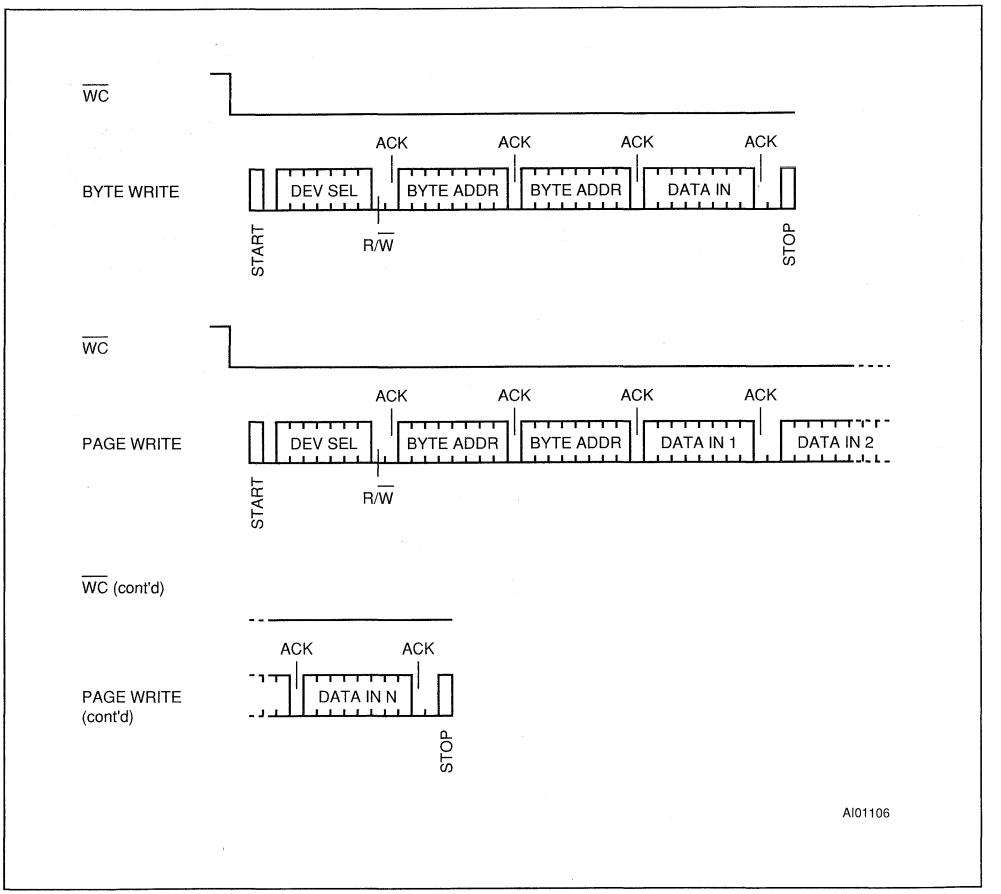


Figure 8. Write Modes Sequence with Write Control = 0



Read Operations

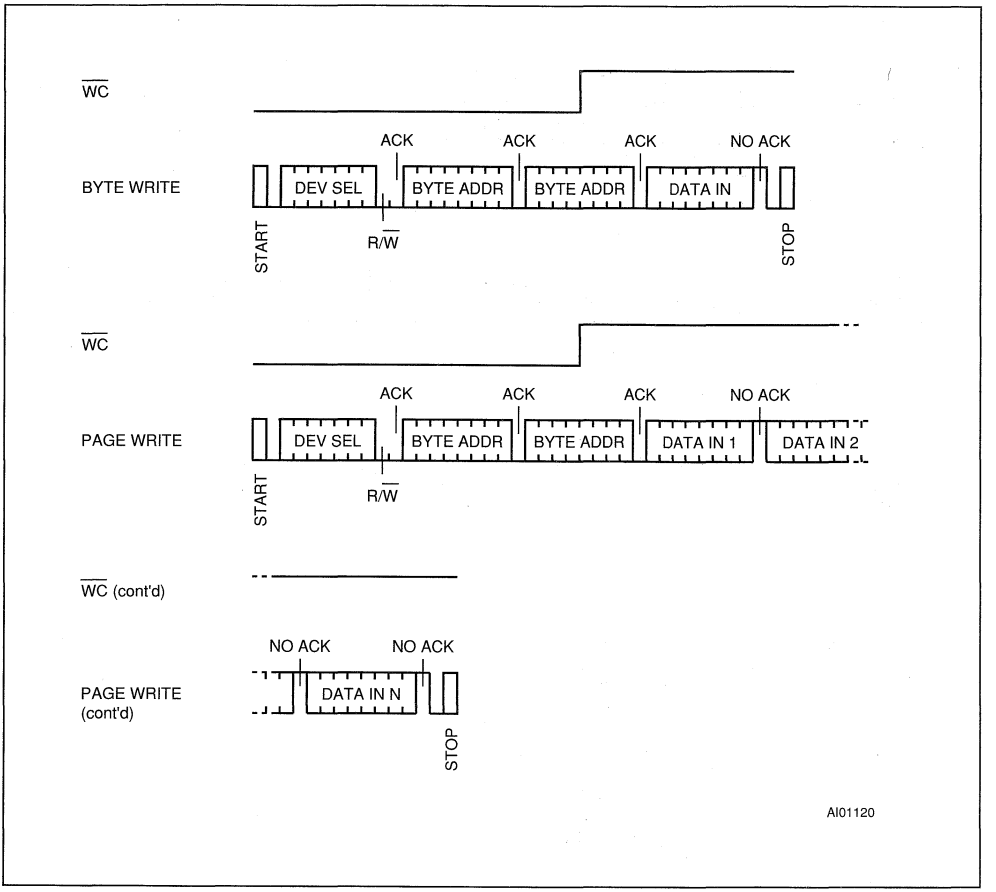
On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E64 have an internal 13 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the R/W bit set to '1'. The ST24/25E64 acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The ST24/25E64 acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E64 continue to output the next byte in

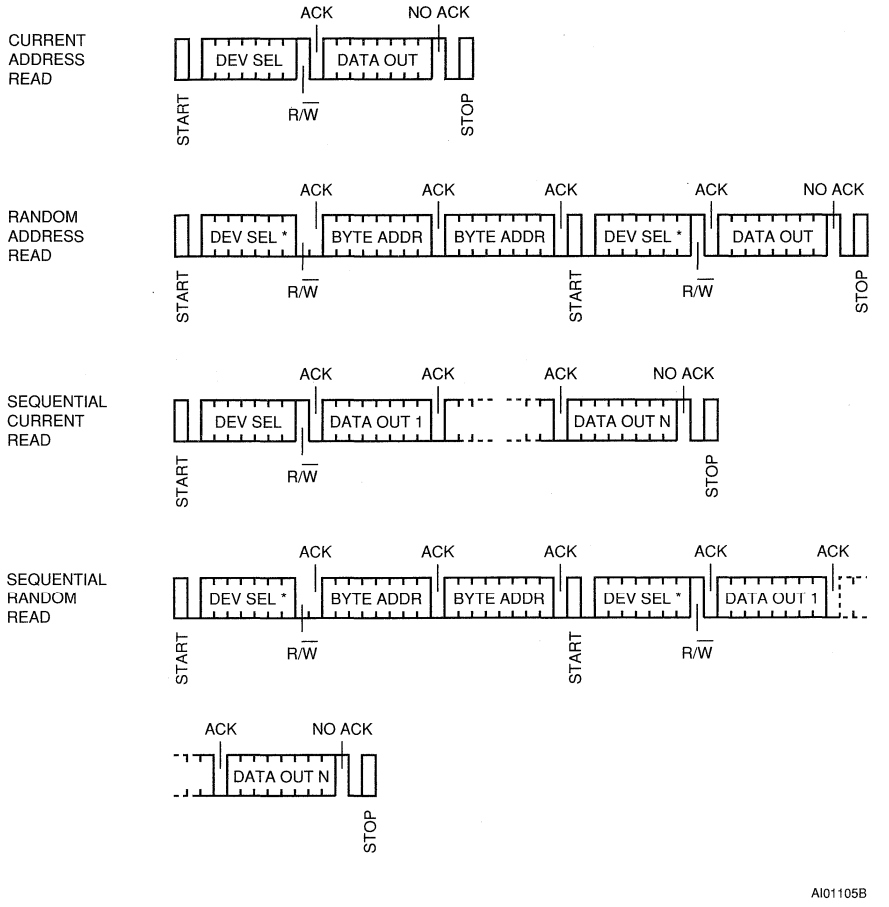
Figure 9. Write Modes Sequence with Write Control = 1



sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

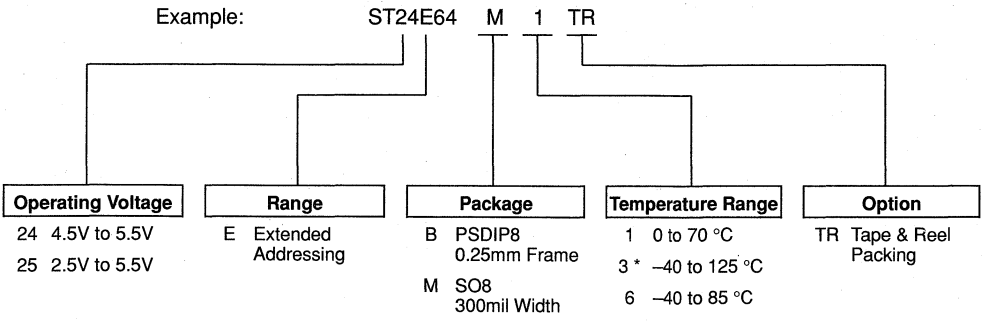
Acknowledge in Read Mode. In all read modes the ST24/25E64 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E64 terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature Range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

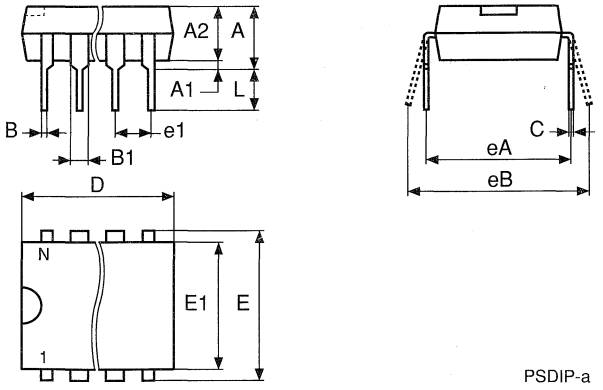
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



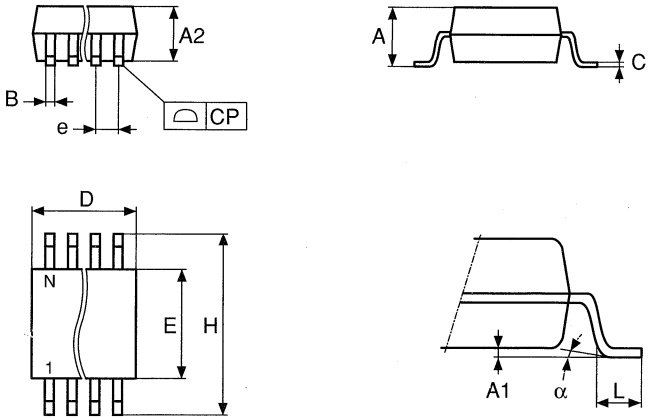
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 300 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N		8			8	
CP			0.10			0.004

SO8



SO-b

Drawing is out of scale

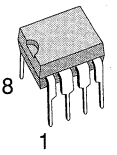
SGS-THOMSON MICROELECTRONICS

ST24E256
ST25E256

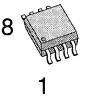
SERIAL ACCESS EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS 256K (32K x 8) EEPROM

PRODUCT PREVIEW

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 100,000 ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for ST24E256 version
  - 2.5V to 5.5V for ST25E256 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 64 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

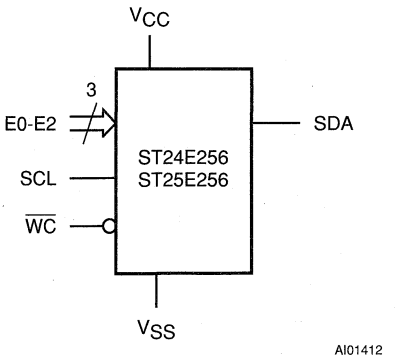


PSDIP8 (B)
0.25mm Frame



SO8 (M)
300mil Width

Figure 1. Logic Diagram



DESCRIPTION

The ST24E256 and ST25E256 are 256K bit electrically erasable programmable memories (EEPROM), organized as 32,768 x 8 bits. The ST25E256 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

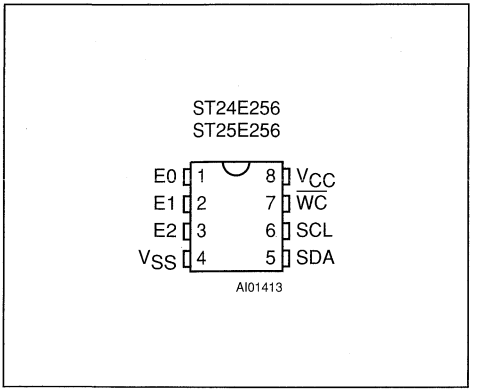


Figure 2B. SO Pin Connections

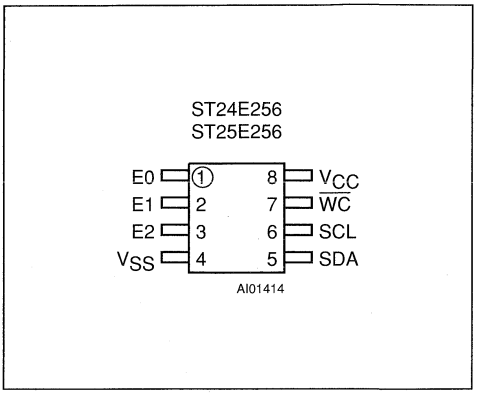


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E256 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E256 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, RW = '1'
Random Address Read	'0'	1	START, Device Select, RW = '0', Address,
	'1'		reSTART, Device Select, RW = '1'
Sequential Read	'1'	1 to 32,768	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, RW = '0'
Page Write	'0'	64	START, Device Select, RW = '0'

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E256 may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 256K bytes.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

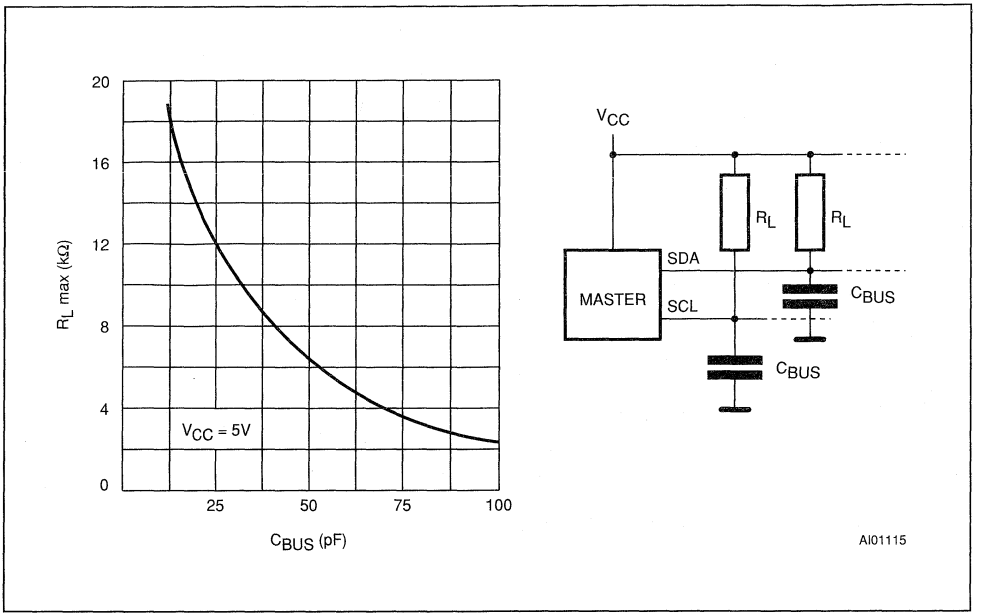
Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When pin $\overline{WC}$ is unconnected, the $\overline{WC}$ input is internally read as V_{IL} (see Table 5).

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acknowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus, f_C = 400kHz



DEVICE OPERATION

I^2C Bus Background

The ST24/25E256 support the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E256 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E256 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E256 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a complete Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E256 sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E256, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = –40 to 85 °C or 0 to 70 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (ST25 series)			1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = –40 to 85 °C or 0 to 70 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

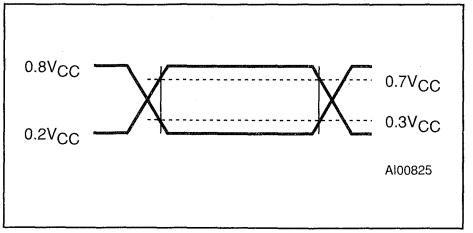
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL1} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b14,b13,b12,b11,b10,b9,b8 of the Most Significant Byte select one block among 128 blocks (one block is 256 bytes).

Most Significant Byte

X	b14	b13	b12	b11	b10	b9	b8

X = Don't Care.

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

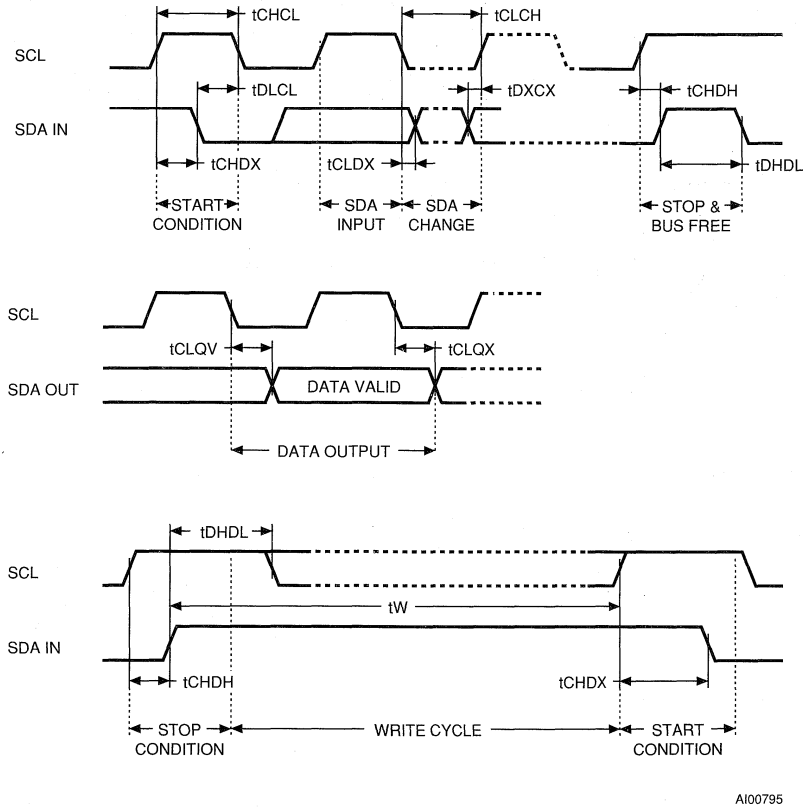
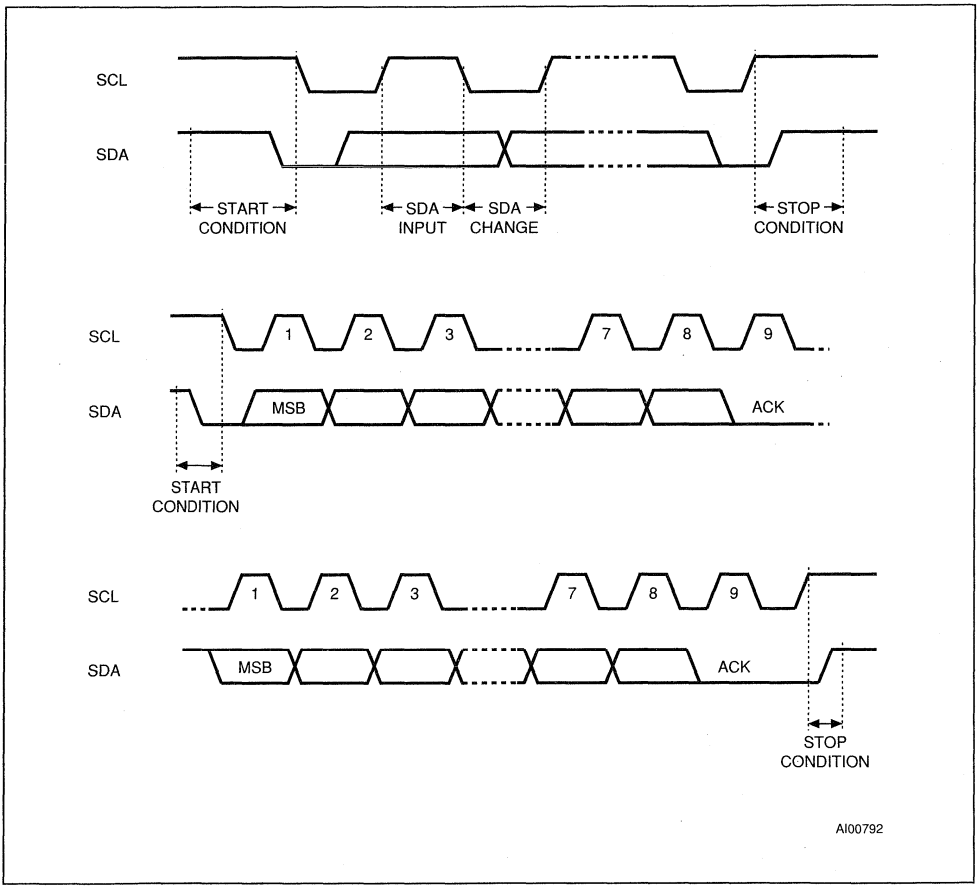


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The ST24/25E256 acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 128 blocks of 256 bytes each. Writing in the ST24/25E256 may be inhibited if input pin $\overline{WC}$ is taken high.

For the ST24/25E256 versions, any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E256. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 64 bytes to be written in a single write cycle, provided that they are all located in the same row of 64 bytes in the memory, that is the same Address bits (b12 to b5). The master sends one up to 32 bytes of data, which are each acknowledged by the ST24/25E256. After each byte is transfered, the internal byte address counter (5 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care

must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the ST24/25E256 will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E256 disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E256 are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E256 have terminated the internal writing, it will issue an ACK. The ST24/25E256 are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK

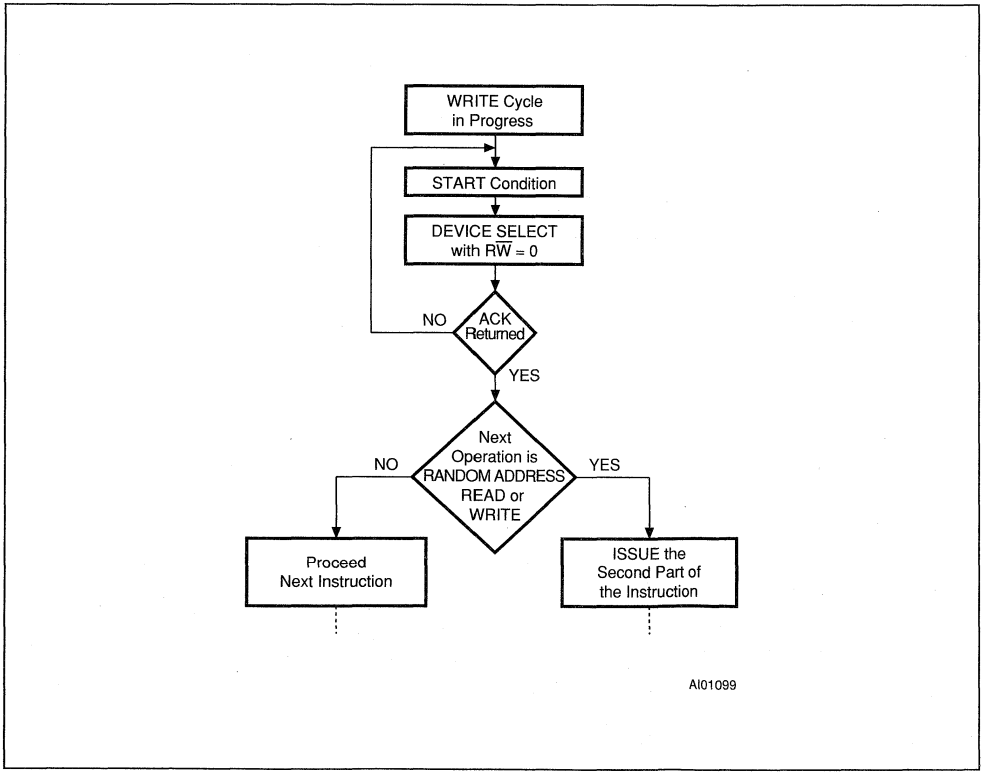
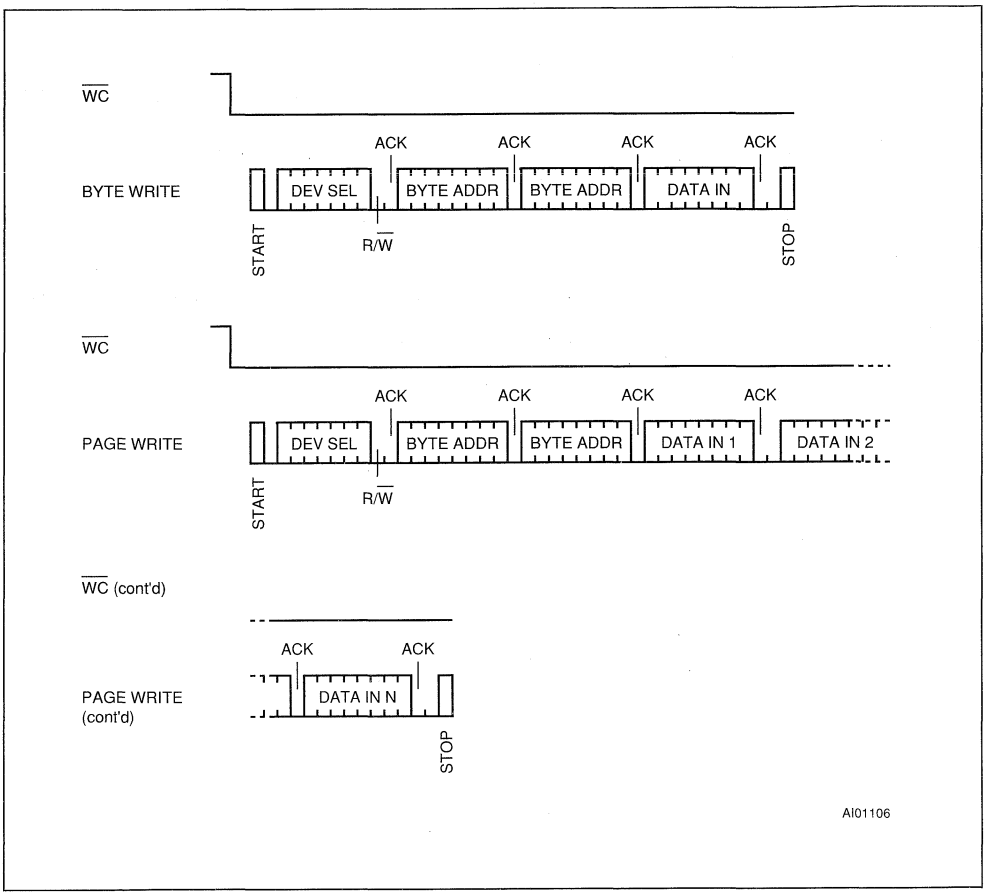


Figure 8. Write Modes Sequence with Write Control = 0



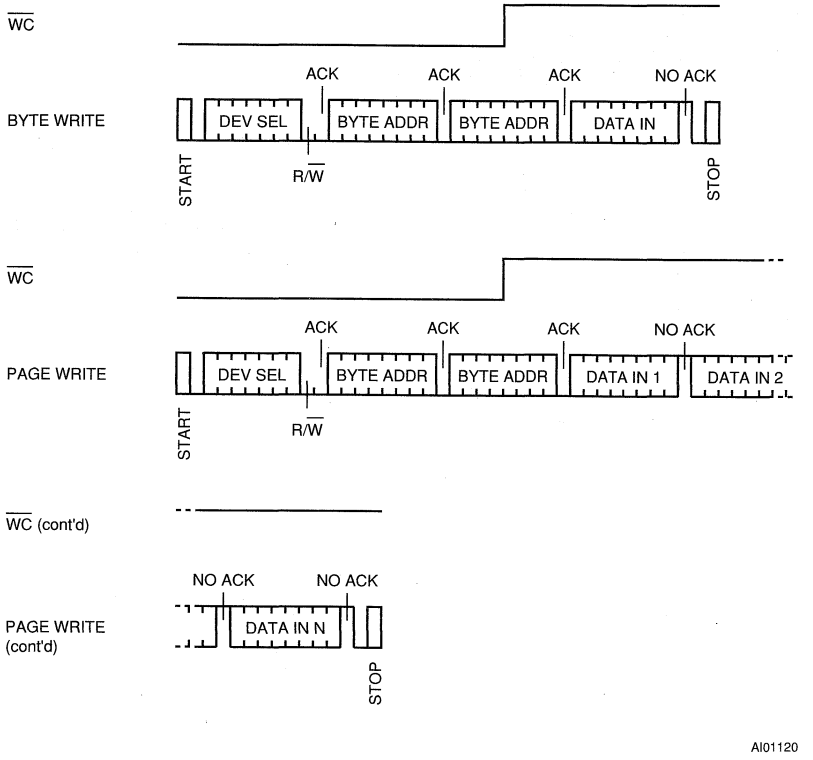
Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E256 have an internal 15 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the RW bit set to '1'. The ST24/25E256 acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the RW bit set to '1'. The ST24/25E256 acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

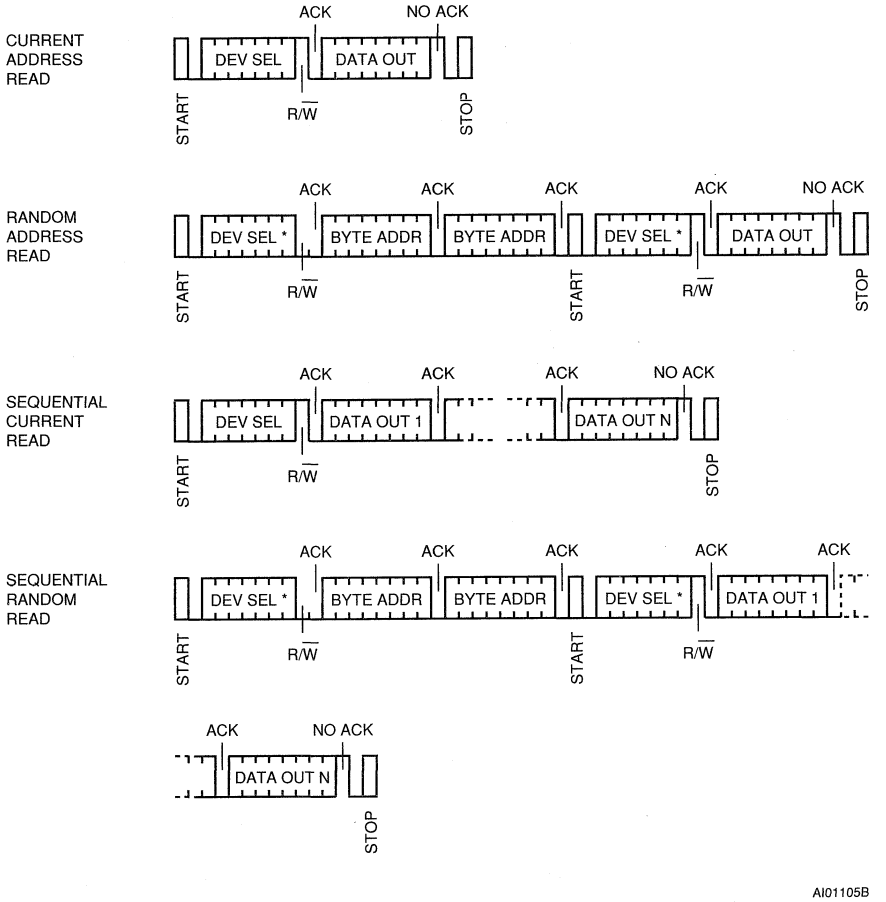
Figure 9. Write Modes Sequence with Write Control = 1



Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E256 continue to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

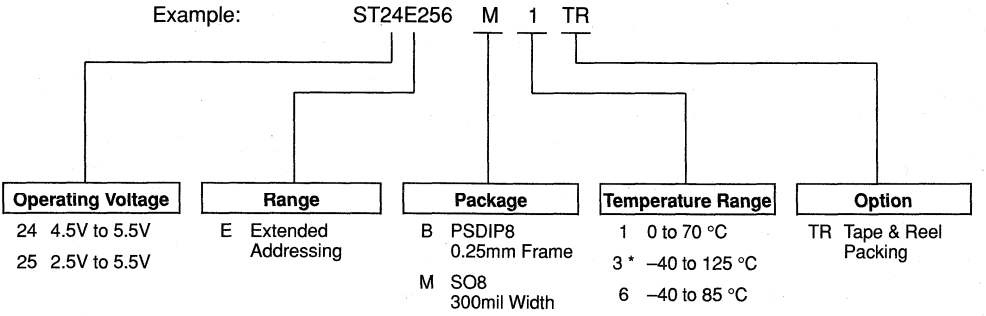
Acknowledge in Read Mode. In all read modes the ST24/25E256 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E256 terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature Range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

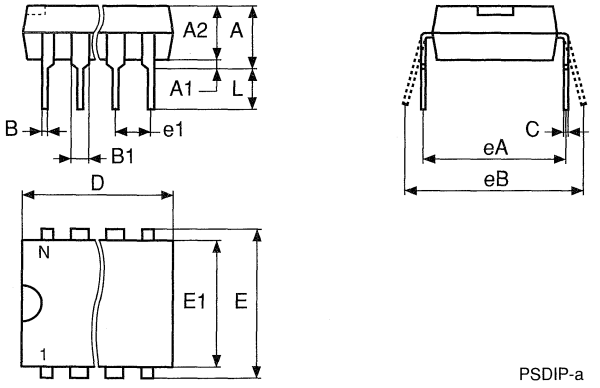
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



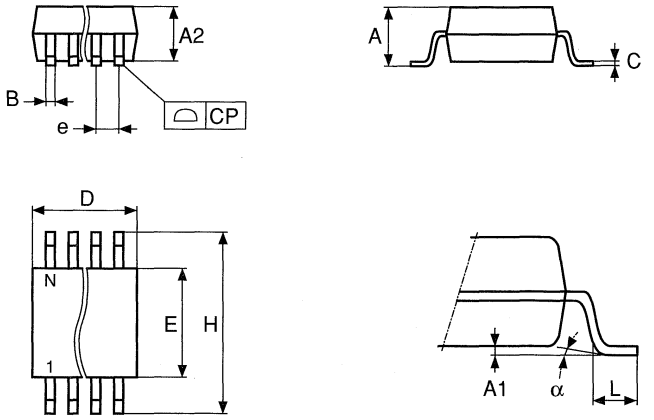
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 300 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N		8			8	
CP			0.10			0.004

SO8



SO-b

Drawing is out of scale

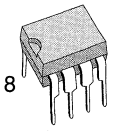
SERIAL ACCESS MICROWIRE BUS EEPROM

SGS-THOMSON MICROELECTRONICS

ST93C06
ST93C06C

SERIAL ACCESS
MICROWIRE BUS 256 bit (16 x 16 or 32 x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 16 x 16 or 32 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSION



PSDIP8 (B)
0.4mm Frame

SO8 (M)

DESCRIPTION

The ST93C06 and ST93C06C are 256 bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. In the text the two products are referred to as ST93C06.

The memory is divided into either 32 x 8 bit bytes or 16 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed through a serial input (D) and by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

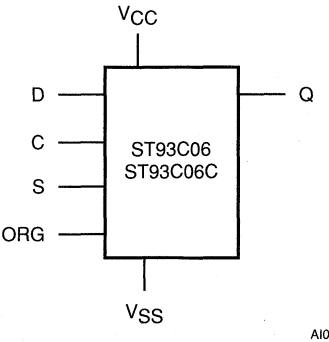
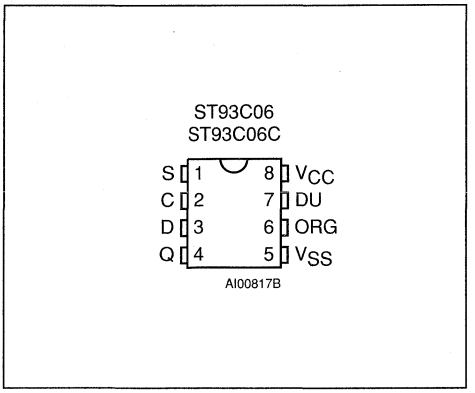
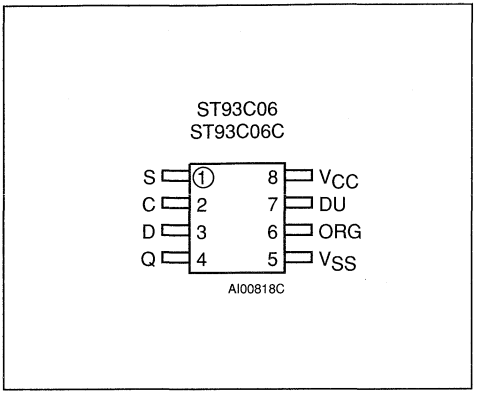


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 -40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST93C06 ST93C06C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST93C06 ST93C06C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C06 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 256 bits long, or continuously as the address counter automatically rolls over to '00' when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 32 bytes or 16 words. After the start of the programming cycle a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

The design of the ST93C06 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 10 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

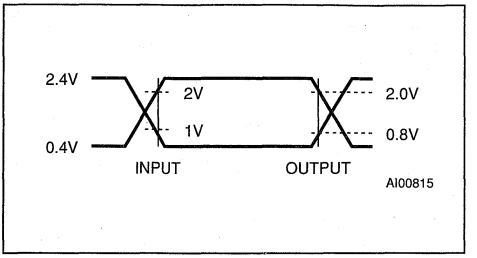


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

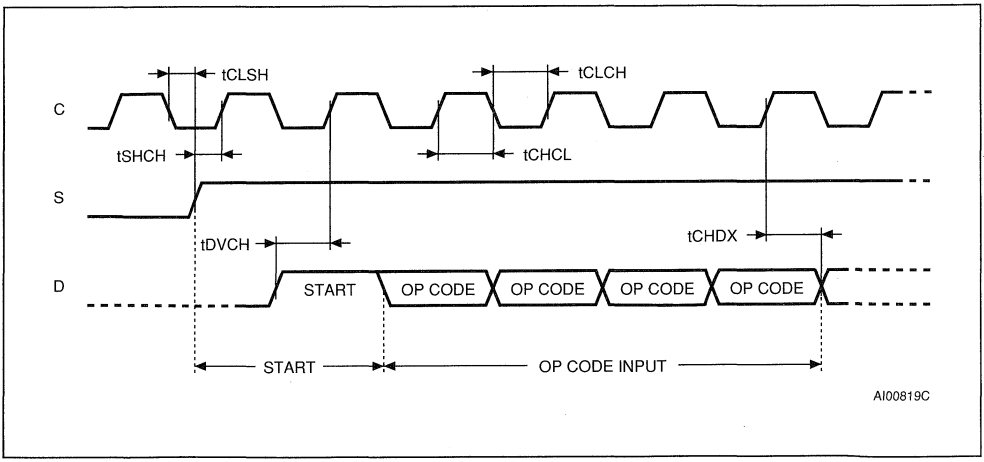
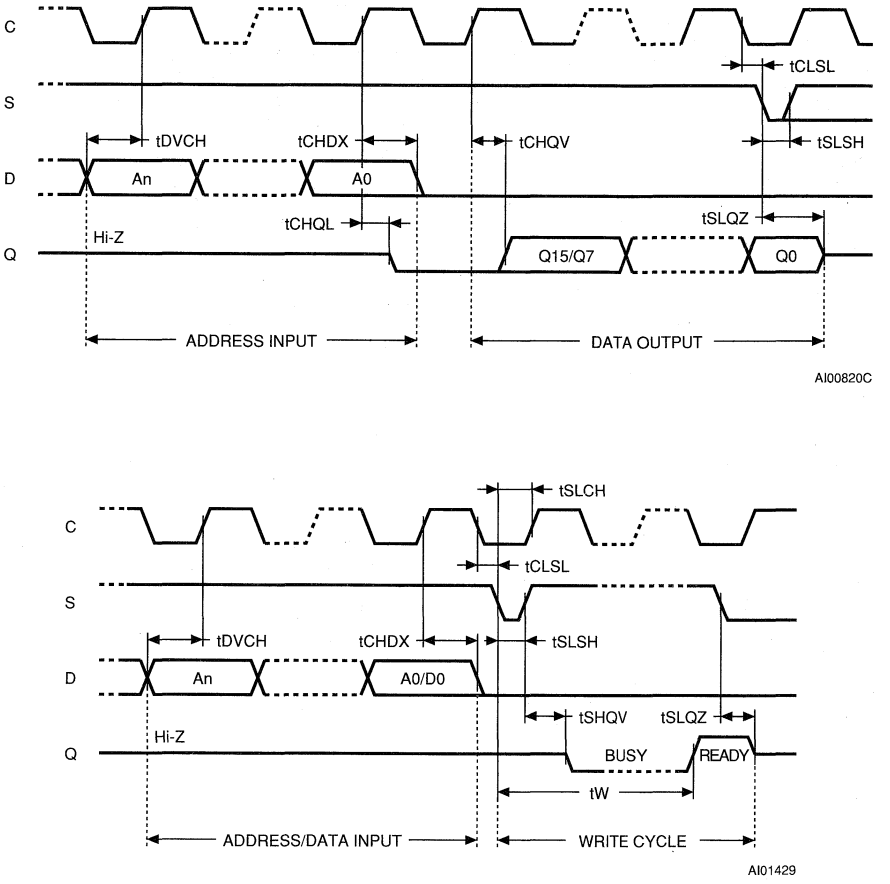


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The ST93C06 is organized as 32 bytes x 8 bits or 16 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C06 is in standby mode, the ORG input should be unconnected or set to either V_{SS} or V_{CC} in order to achieve the minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93C06 has seven instructions, as shown in Table 6. The op-codes of the instructions are made up of 4 bits: some instructions use only the first two bits, others use all four bits to define the op-code. The op-code is followed by an address for the byte/word which is four bits long for the x16 organization or five bits long for the x8 organization.

Each instruction is preceded by the rising edge of the signal applied on the S input (assuming that clock C and data input D are low), followed by a first clock pulse which is ignored by the ST93C06 (optional clock pulse for the ST93C06C). The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C06 as a Start bit. Even though the first clock pulse is ignored, it recommended to pull low the data input D during this first clock pulse in order to keep the timing upwardly compatible with other ST93Cxx devices.

The ST93C06 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C06 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C06 enters the Disable mode. When the Erase/Write Enable instruction (EWEN) is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle. The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

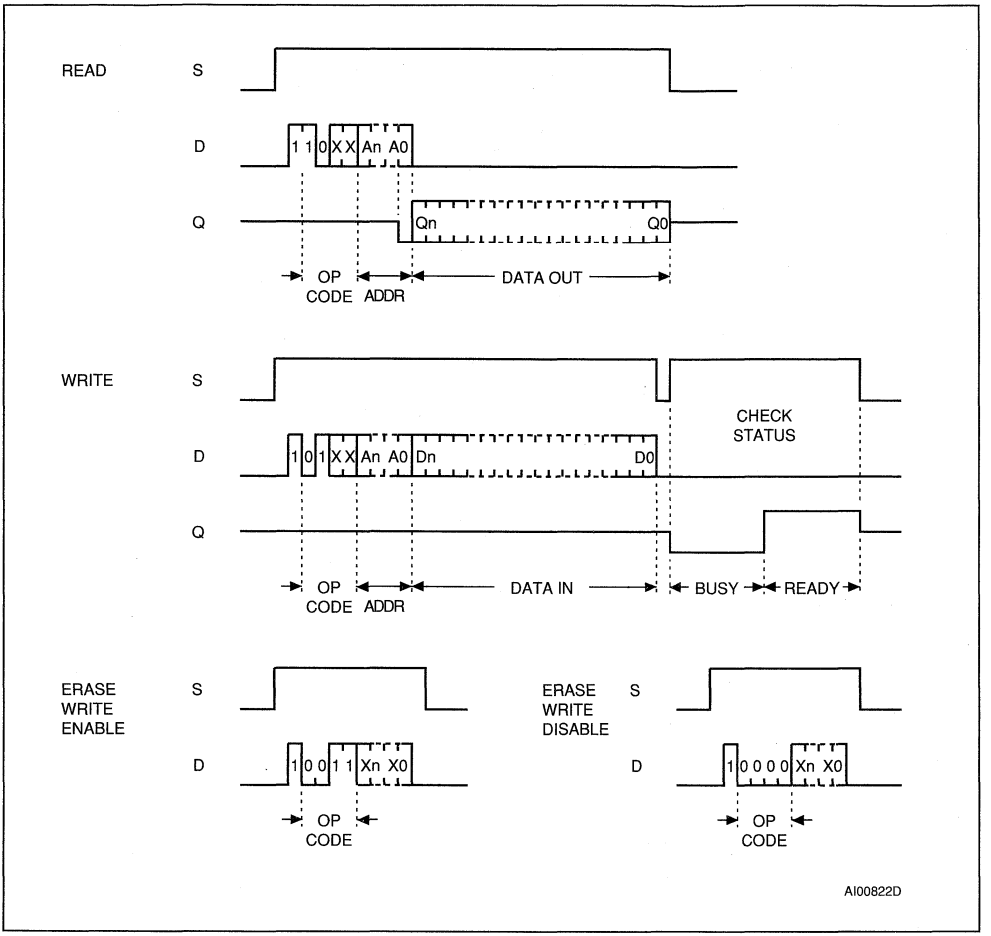
The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0)	Data	x16 Org Address (ORG = 1)	Data
READ	Read Data from Memory	10XX	A4-A0	Q7-Q0	A3-A0	Q15-Q0
WRITE	Write Data to Memory	01XX	A4-A0	D7-D0	A3-A0	D15-D0
EWEN	Erase/Write Enable	0011	XXXXX		XXXX	
EWDS	Erase/Write Disable	0000	XXXXX		XXXX	
ERASE	Erase Byte or Word	11XX	A4-A0		A3-A0	
ERAL	Erase All Memory	0010	XXXXX		XXXX	
WRAL	Write All Memory with same Data	0001	XXXXX	D7-D0	XXXX	D15-D0

Note: X = don't care bit.

Figure 6. READ, WRITE, EWEN, EWDS Sequences



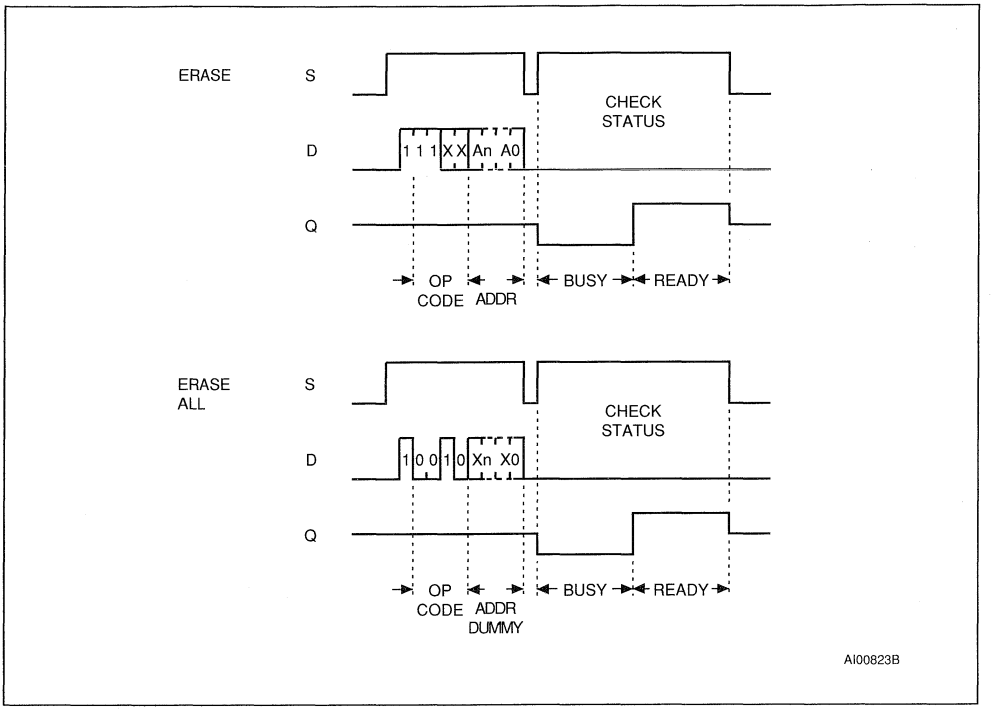
Notes: 1. An: n = 3 for x16 org. and 4 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Write

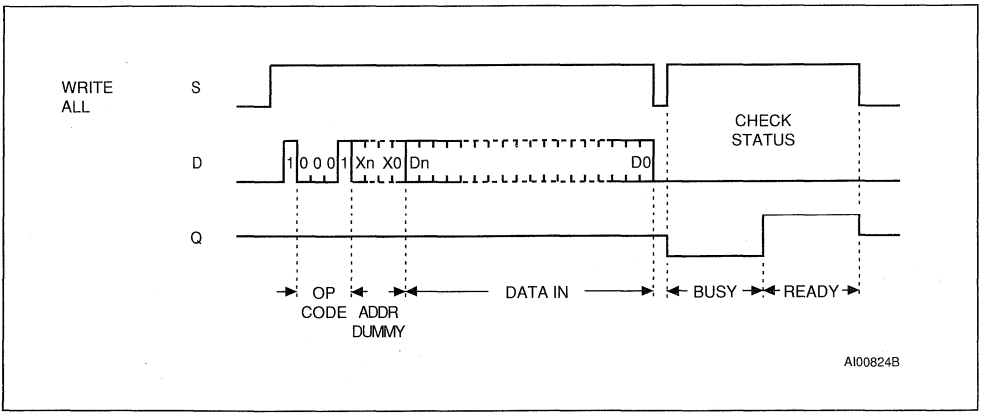
The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 3 for x16 org. and 4 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

Figure 8. WRAL Sequence



Note: 1 Xn: n = 3 for x16 org. and 4 for x8 org.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction: the WRAL instruction DOES NOT perform an automatic erase before writing. The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C06 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader may also refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

DIFFERENCES BETWEEN ST93C06 AND ST93C06C

Each instruction of the ST93C06 requires an Additional Dummy clock pulse after the rising edge of the Chip Select input (S) and before the START bit, see Figure 9. When replacing the ST93C06 with the ST93C06C in an application, it must be checked that this Dummy Clock cycle DOES NOT HAPPEN when D = 1: if it is so, this clock pulse will latch an information which is decoded by the ST93C06C as a START bit (see Figure 10) and the following bits will be decoded with a shift of one bit.

Figure 9. ST93C06 Timing

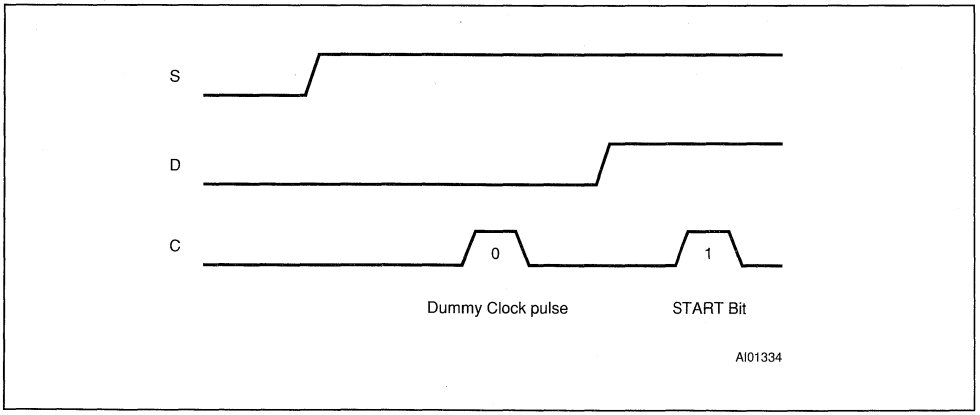


Figure 10. Comparative Timings

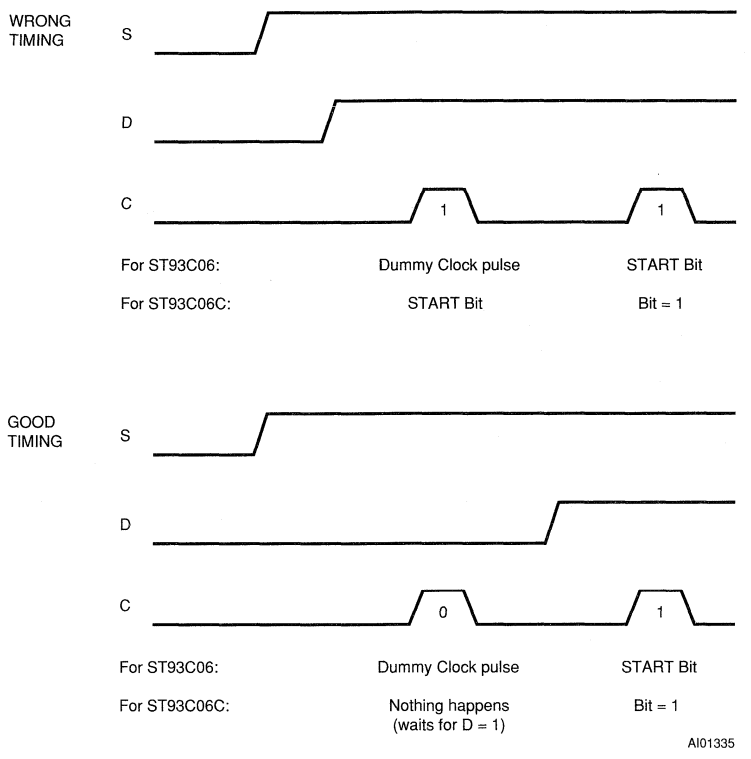
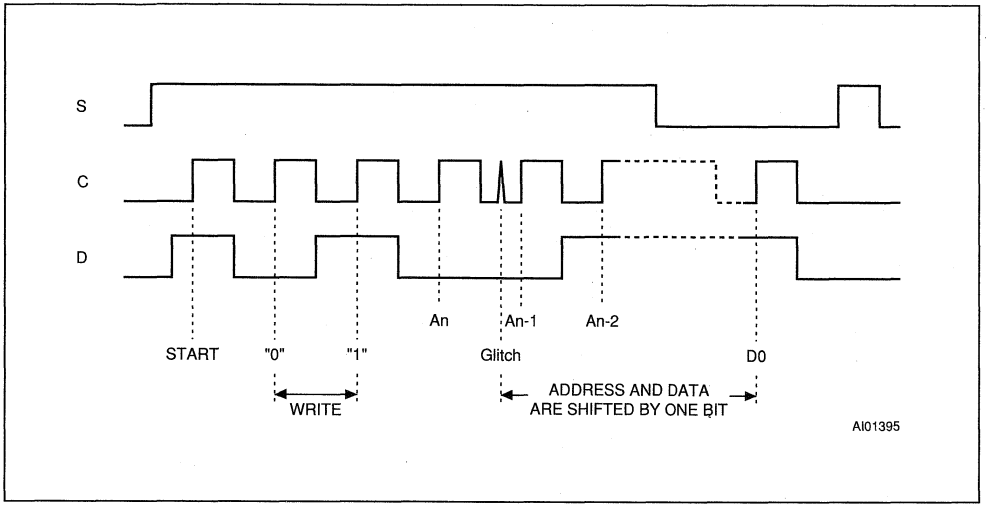


Figure 11. WRITE Swquence with One Clock Glitch



DIFFERENCES BETWEEN ST93C06 AND ST93C06C (cont'd)

The ST93C06C is an enhanced version of the ST93C06A and offers the following extra features:

- Enhanced ESD voltage
- Functional security filtering glitches on the clock input (C).

Refer to Table 2 (Absolute Maximum Ratings) for more about ESD limits. The following description will detail the Clock pulses counter (available only on the ST93C06C).

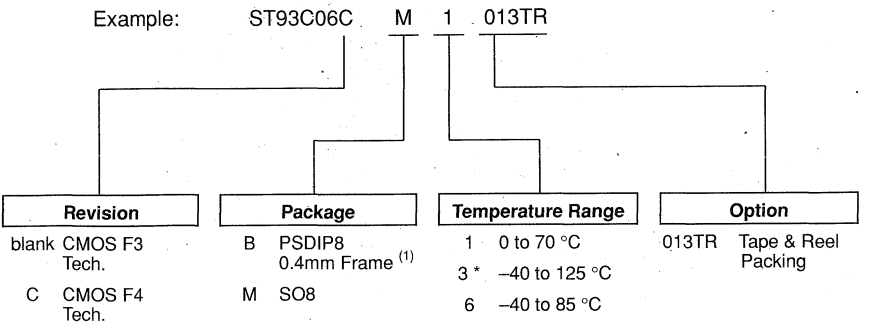
In a normal environment, the ST93C06 is expected to receive the exact amount of data on the D input, that is the exact amount of clock pulses on the C input.

In a noisy environment, the amount of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the ST93C06C. In such a case, a part of the instruction is delayed by one bit (see Figure 11), and it may induce an erroneous write of data at a wrong address.

The ST93C46C has an on-board counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal. For the WRITE instructions, the number of clock pulses incoming to the counter must be exactly 18 (with the Organisation by 8) from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 bits of Op-code + 7 bits of Address + 8 bits of Data = 18): if so, the ST93C06C executes the WRITE instruction; if the number of clock pulses is not equal to 18, the instruction will not be executed (and data will not be corrupted).

In the same way, when the Organisation by 16 is selected, the number of clock pulses incoming to the counter must be exactly 25 (1 Start bit + 2 bits of Op-code + 6 bits of Address + 16 bits of Data = 25) from the Start bit to the falling edge of Chip Select signal: if so, the ST93C06C executes the WRITE instruction; if the number of clock pulses is not equal to 25, the instruction will not be executed (and data will not be corrupted). The clock pulse counter is active only on ERASE and WRITE instructions (WRITE, ERASE, ERAL, WRALL).

ORDERING INFORMATION SCHEME



Notes: 1. ST93C06CB1 is available with 0.25mm lead Frame only.
3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

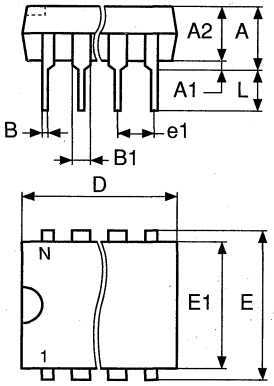
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

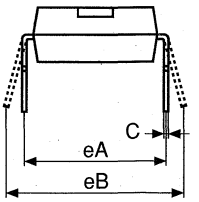
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8





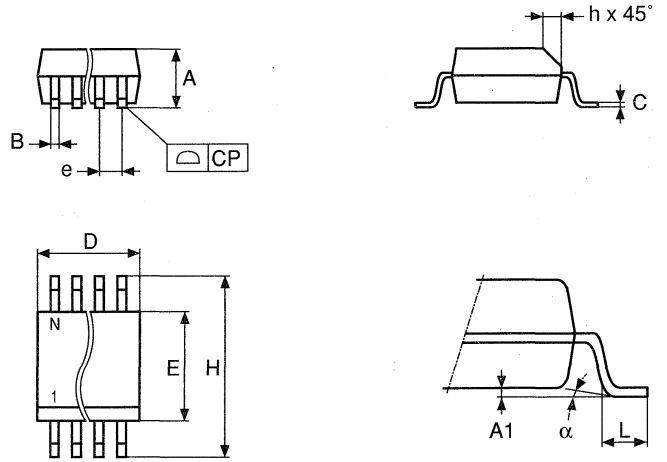
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



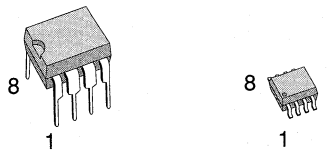
SO-a

Drawing is out of scale

ST93C46A, ST93C46C ST93C46T

SERIAL ACCESS MICROWIRE BUS 1K (64 x 16 or 128 x 8) EEPROM

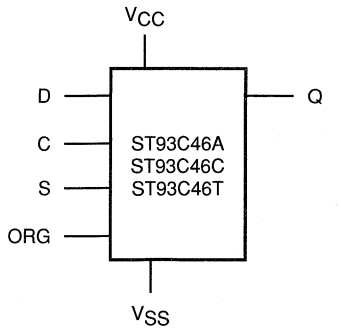
- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 64 x 16 or 128 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSION



PSDIP8 (B)
0.4mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

This specification covers a range of 1K bit EEPROM products, the ST93C46A, ST93C46C and ST93C46T. In the text, products are referred to as ST93C46. The ST93C46 is a 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input (D) and output (Q).

The 1K bit memory is divided into either 128 x 8 bit bytes or 64 x 16 bit words. The organization may be selected by a signal on the ORG input.

Table 1. Signal Names

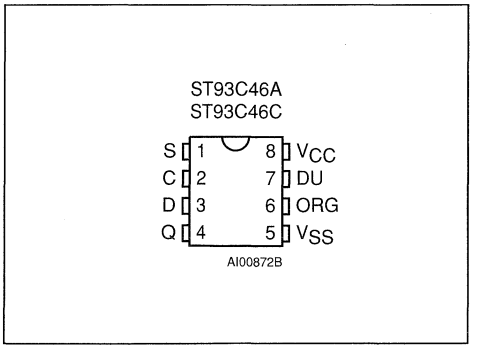
S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST93C46A,T ST93C46C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST93C46	500	V

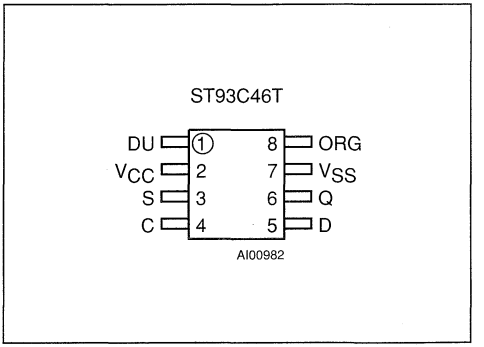
Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Figure 2A. DIP Pin Connections



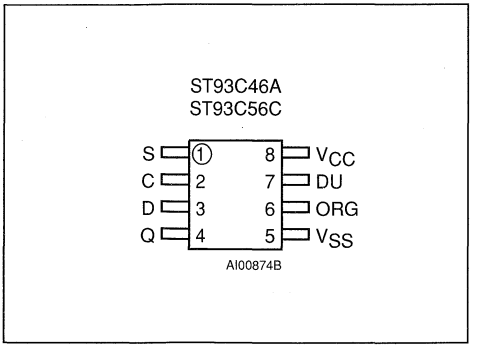
Warning: DU = Don't Use

Figure 2B. SO, 90° Turn, Pin Connections



Warning: DU = Don't Use

Figure 2C. SO Pin Connections



Warning: DU = Don't Use

DESCRIPTION (cont'd)

The memory is accessed by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All.

A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data is then clocked out serially.

The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C46 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 1024 bits long, or continuously as the address counter automatically rolls over to '00' when the highest address is reached.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

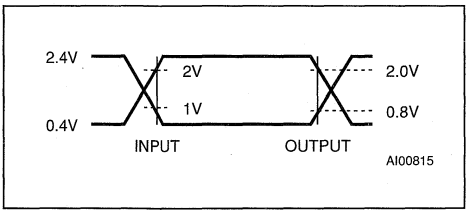


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

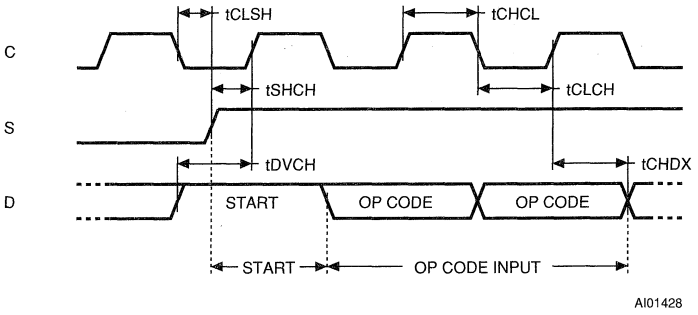
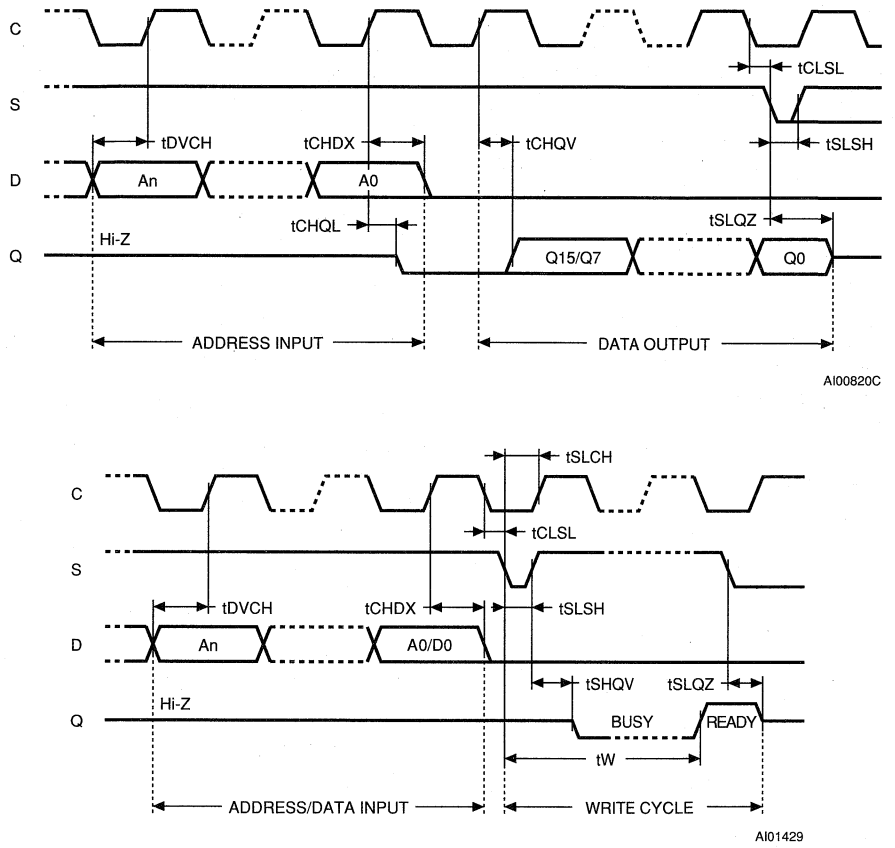


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 128 bytes or 64 words. After the start of the programming cycle a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is High.

An internal feature of the ST93C46 provides Power-on Data Protection by inhibiting any operation when the Supply is too low. The design of the ST93C46 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The ST93C46 is organised as 128 bytes x 8 bits or 64 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C46 is in standby mode, the ORG input should be unconnected or set to either V_{SS} or V_{CC} in order to get minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

During power-up, A Power On Reset sequence is run in order to reset all internal programming circuitry and the device is set in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction.

INSTRUCTIONS

The ST93C46 has seven instructions, as shown in Table 6. Each instruction is preceded by the rising edge of the signal applied on the S input (assuming that the clock C is low), followed by a '1' read on D input during the rising edge of the clock C. The op-codes of the instructions are made up of the 2 following bits. Some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is followed by an address for the byte/word which is made up of six bits for the x16 organization or seven bits for the x8 organization.

Remark: *a rising edge of the Chip Select (S) when both inputs Clock (C) and Data Input (D) are high is also decoded as a Start bit. However, it is preferable not to use such a sequence.*

The ST93C46 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C46 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) freezes the execution of the following Erase/Write instructions. When power is first applied to the ST93C46, Erase/Write is inhibited. When the EWEN instruction is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset threshold. To protect the memory contents from accidental corruption, it is

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0)	Data	x16 Org Address (ORG = 1)	Data
READ	Read Data from Memory	10	A6-A0	Q7-Q0	A5-A0	Q15-Q0
WRITE	Write Data to Memory	01	A6-A0	D7-D0	A5-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXXXX		11XXXX	
EWDS	Erase/Write Disable	00	00XXXXX		00XXXX	
ERASE	Erase Byte or Word	11	A6-A0		A5-A0	
ERAL	Erase All Memory	00	10XXXXX		10XXXX	
WRAL	Write All Memory with same Data	00	01XXXXX	D7-D0	01XXXX	D15-D0

Note: X = don't care bit.

advisable to issue the EWDS instruction after every write cycle.

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

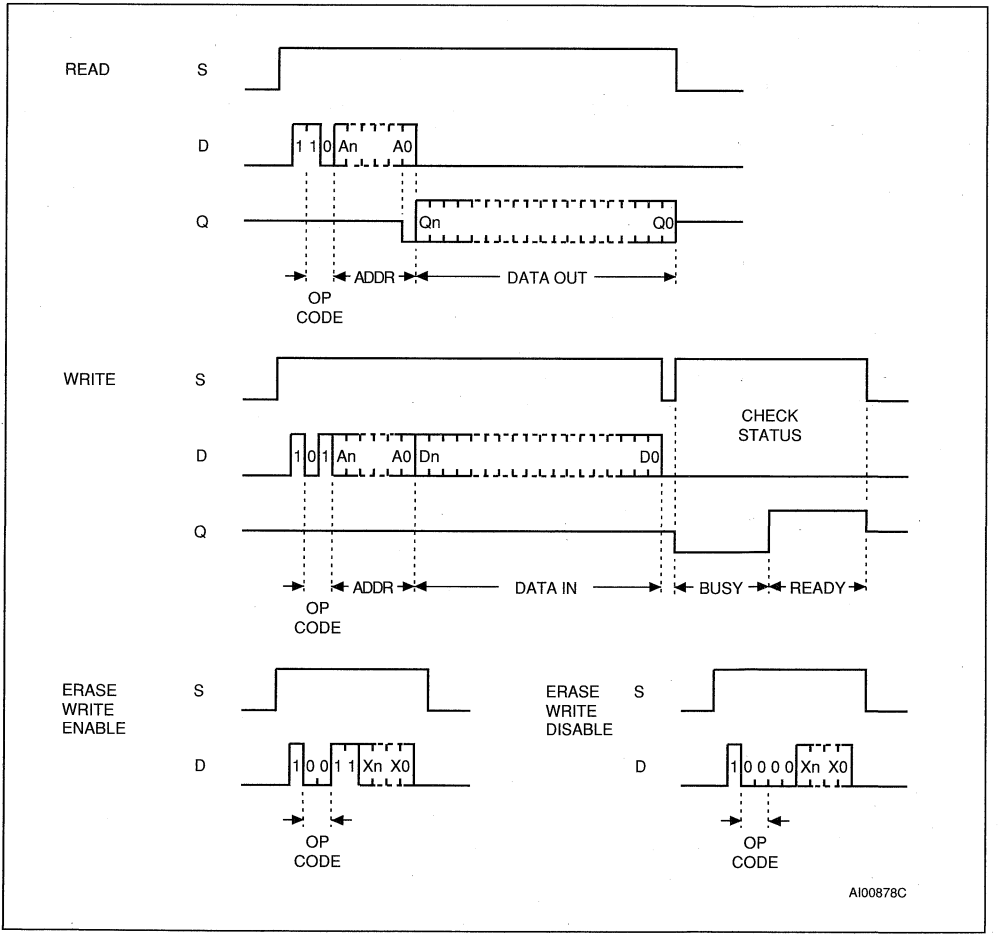
The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) starts a self-timed programming cycle.

If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Write

The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled,

Figure 6. READ, WRITE, EWEN, EWDS Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 4 for x16 org. and 5 for x8 org.

INSTRUCTIONS (cont'd)

Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

The Write instruction includes an automatic Erase cycle before writing the data, it is therefore unnecessary to execute an Erase instruction before a Write instruction execution.

Erase All

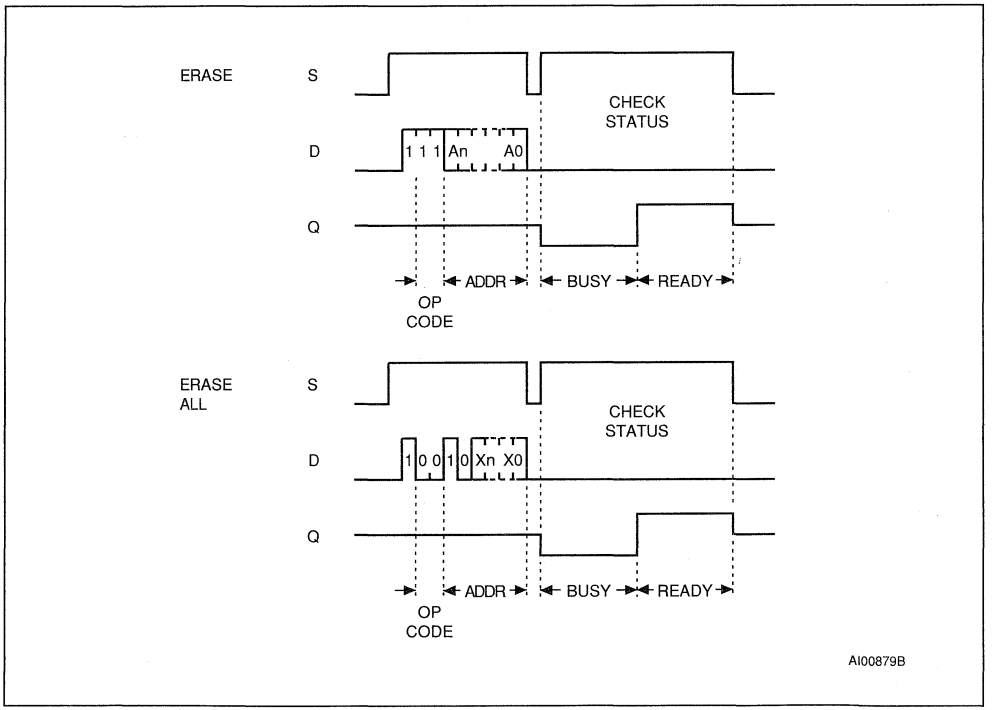
The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to "1"). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction above. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction.

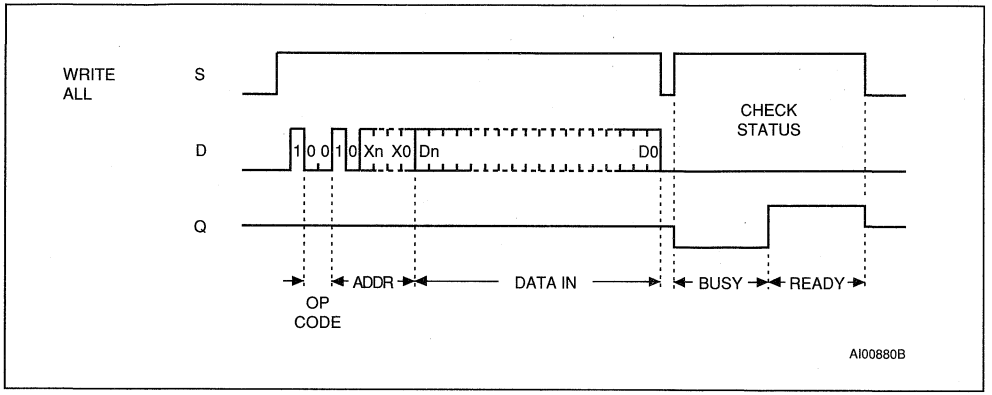
The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. In the WRAL instruction, NO automatic erase is made so all bytes/words must be erased before the WRAL instruction. If the ST93C46 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C46 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C46 is ready to receive a new instruction.

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 5 for x16 org. and 6 for x8 org.
2. Xn: n = 4 for x16 org. and 5 for x8 org.

Figure 8. WRAL Sequence



Note: 1. Xn: n = 4 for x16 org. and 5 for x8 org.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select is driven High. Once the ST93C46 is Ready, the Data Output is set to '1' until a new start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

DIFFERENCES BETWEEN ST93C46A AND ST93C46C

The ST93C46C is an enhanced version of the ST93C46A and offers the following extra features:

- Enhanced ESD voltage
- Functional security filtering glitches on the clock input (C).

Refer to Table 2 (Absolute Maximum Ratings) for more about ESD limits. The following description will detail the Clock pulses counter (available only on the ST93C46C).

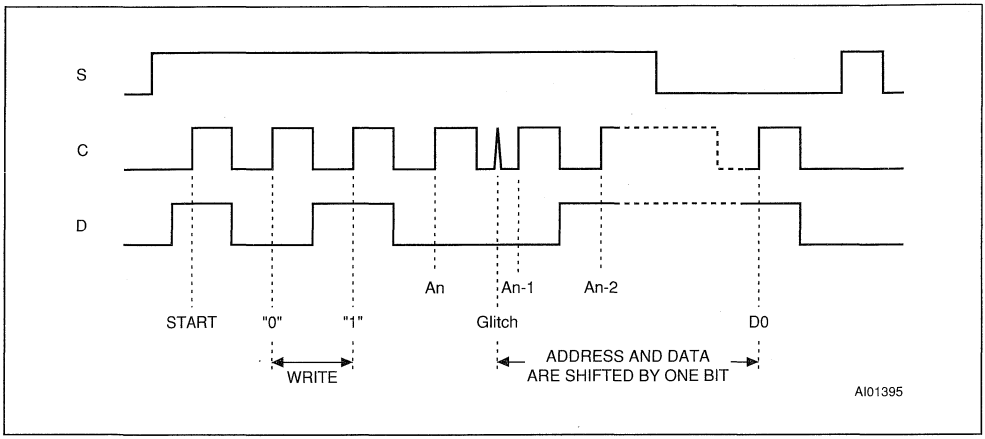
In a normal environment, the ST93C46 is expected to receive the exact amount of data on the D input, that is the exact amount of clock pulses on the C input.

In a noisy environment, the amount of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the ST93C46C. In such a case, a part of the instruction is delayed by one bit (see Figure 9), and it may induce an erroneous write of data at a wrong address.

The ST93C46C has an on-board counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal. For the WRITE instructions, the number of clock pulses incoming to the counter must be exactly 18 (with the Organisation by 8) from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 bits of Op-code + 7 bits of Address + 8 bits of Data = 18): if so, the ST93C46C executes the WRITE instruction; if the number of clock pulses is not equal to 18, the instruction will not be executed (and data will not be corrupted).

In the same way, when the Organisation by 16 is selected, the number of clock pulses incoming to the counter must be exactly 25 (1 Start bit + 2 bits of Op-code + 6 bits of Address + 16 bits of Data = 25) from the Start bit to the falling edge of Chip Select signal: if so, the ST93C46C executes the WRITE instruction; if the number of clock pulses is not equal to 25, the instruction will not be executed (and data will not be corrupted). The clock pulse counter is active only on ERASE and WRITE instructions (WRITE, ERASE, ERAL, WRALL).

Figure 9. WRITE Sequence with One Clock Glitch



ORDERING INFORMATION SCHEME

Example: ST93C46A M 1 013TR

Revision	Package	Temperature Range	Option
A CMOS F3 Tech.	B PSDIP8 0.4 mm Frame(1)	1 0 to 70 °C	013TR Tape & Reel Packing (A, T version)
C CMOS F4 Tech.	M SO8	3 * –40 to 125 °C	TR Tape & Reel Packing (C version)
T CMOS F3 Tech. 90° Turn pin out		6 –40 to 85 °C	

Notes: 1. ST93C46CB1 is available in 0.25mm lead Frame only.
3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

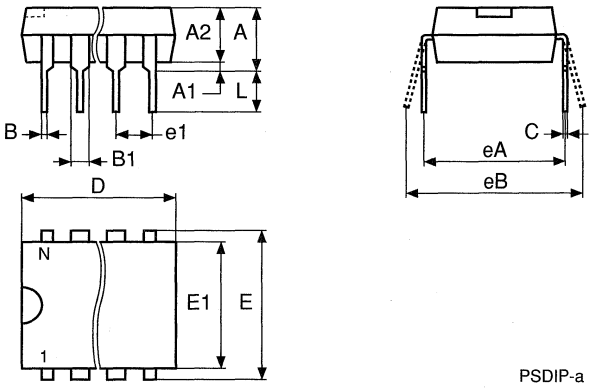
For a list of available options (Revision, Package etc...) refer to the the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



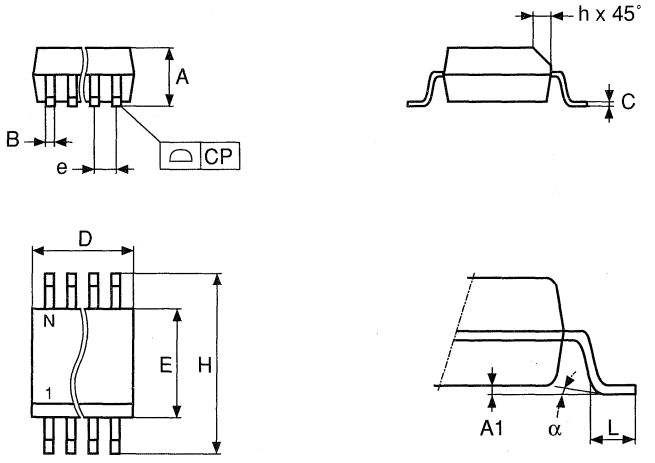
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8

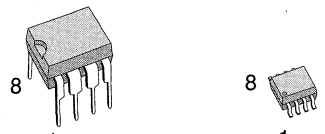


SO-a

Drawing is out of scale

SERIAL ACCESS MICROWIRE BUS 2K (128 x 16 or 256 x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 128 x 16 or 256 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

SO8 (M)

DESCRIPTION

The ST93C56 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input (D).

The memory is divided into either 256 x 8 bit bytes or 128 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and,

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

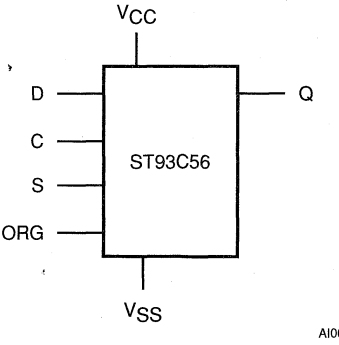
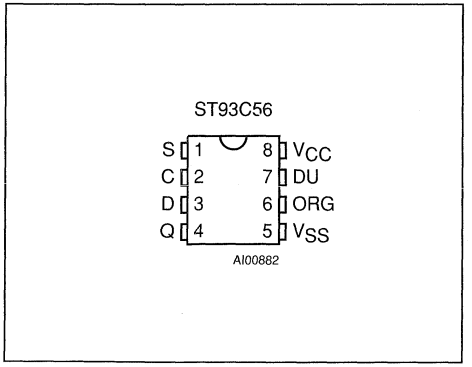
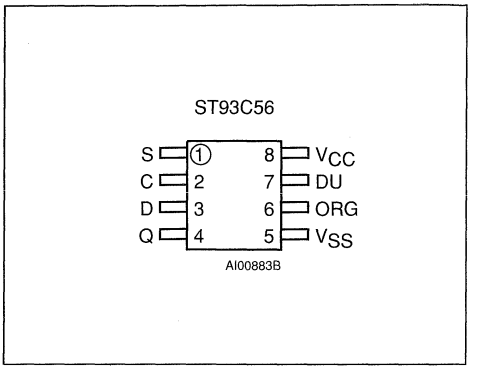


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)		–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		6000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

if the Chip Select input (S) is held High, the ST93C56 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 2048 bits long, or continuously as the address counter automatically rolls over to '00' when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 256 bytes or 128 words. After the start of the programming cycle, a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

The design of the ST93C56 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

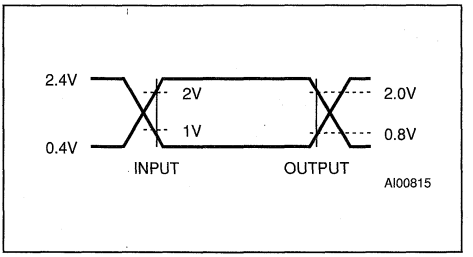


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

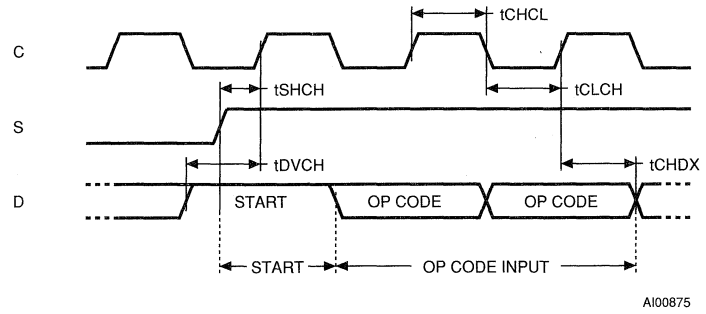
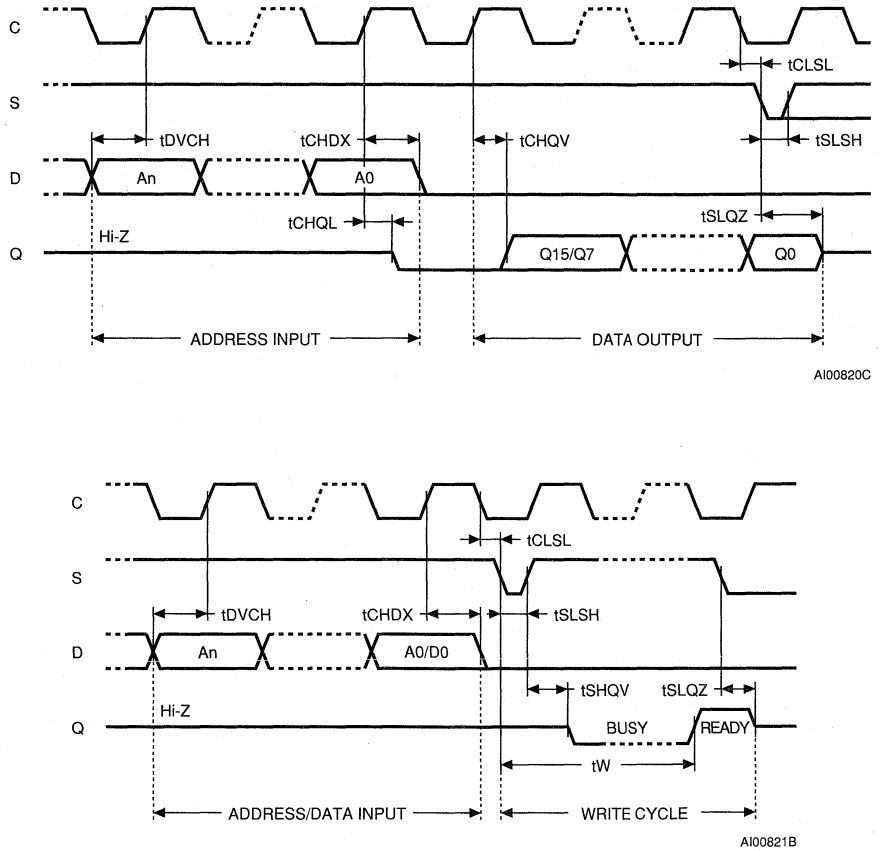


Figure 5. Synchronous Timing, Read or Write



MEMORY ORGANIZATION

The ST93C56 is organized as 256 bytes x 8 bits or 128 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C56 is in standby mode, the ORG input should be unconnected or set to either V_{SS} or V_{CC} in order to achieve the minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied, before applying any logic signal.

INSTRUCTIONS

The ST93C56 has seven instructions, as shown in Table 6. The op-codes of the instructions are made up of 2 bits. The op-code is followed by an address for the byte/word which is eight bits long for the x16 organization or nine bits long for the x8 organization. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that the clock C is low). The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C56 as a Start bit.

Remark. *A rising edge of Chip Select (S) when both inputs Clock (C) and Data Input (D) are high is also decoded as a Start bit. However, it is preferable not to use such a sequence.*

The ST93C56 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first, followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C56 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C56 enters the Disable mode. When the EWEN instruction is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset threshold. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle.

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

If the ST93C56 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction.

Write

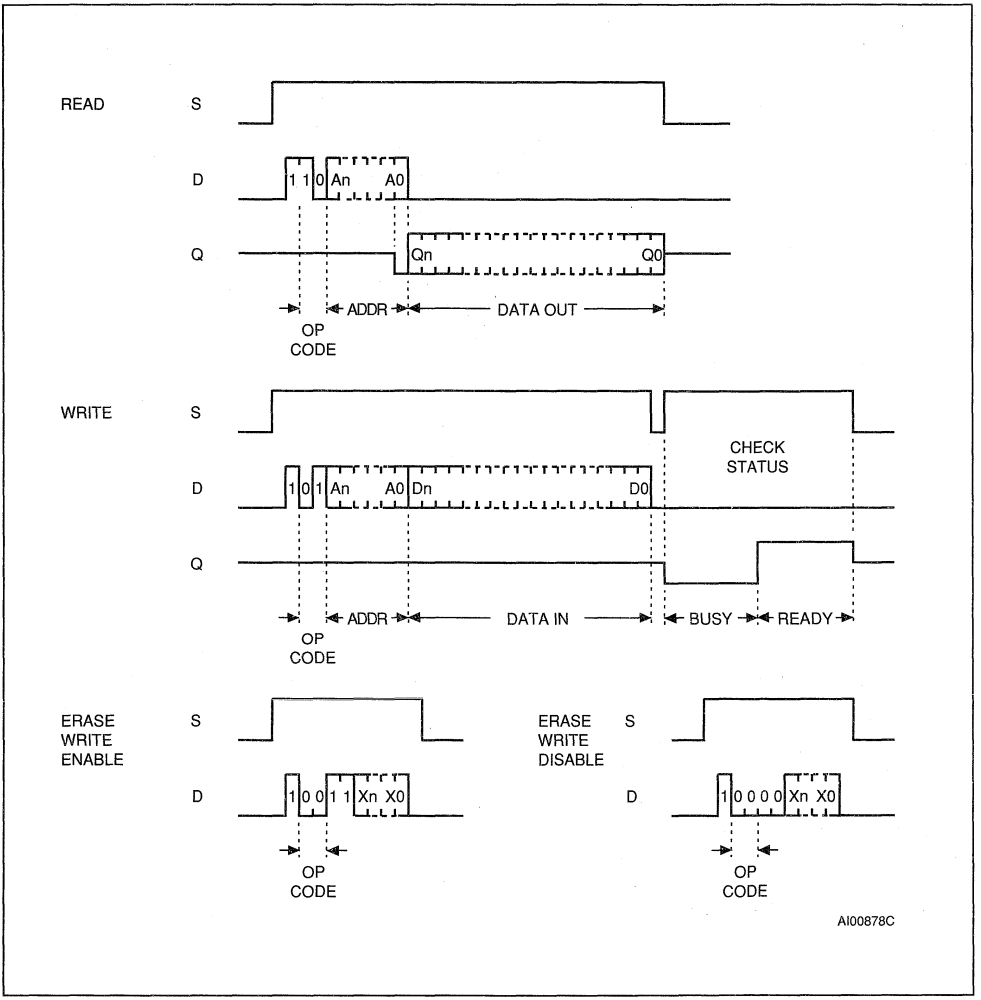
The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0) (1, 2)	Data	x16 Org Address (ORG = 1) (1, 3)	Data
READ	Read Data from Memory	10	A8-A0	Q7-Q0	A7-A0	Q15-Q0
WRITE	Write Data to Memory	01	A8-A0	D7-D0	A7-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXX XXXX		11XX XXXX	
EWDS	Erase/Write Disable	00	00XXX XXXX		00XX XXXX	
ERASE	Erase Byte or Word	11	A8-A0		A7-A0	
ERAL	Erase All Memory	00	10XXX XXXX		10XX XXXX	
WRAL	Write All Memory with same Data	00	01XXX XXXX	D7-D0	01XX XXXX	D15-D0

Notes: 1. X = don't care bit.
2. Address bit A8 is not decoded by the ST93C56.
3. Address bit A7 is not decoded by the ST93C56.

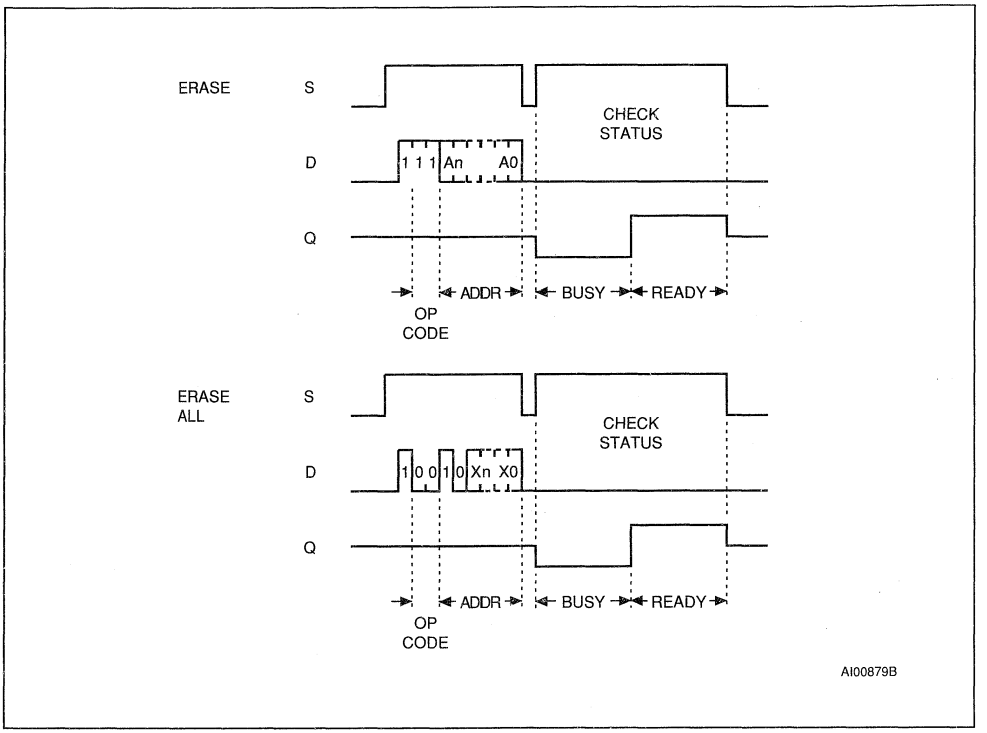
Figure 6. READ, WRITE, EWEN, EWDS Sequences



Notes: 1. An: n = 7 for x16 org. and 8 for x8 org.
2. Xn: n – 5 for x16 org. and 6 for x8 org.

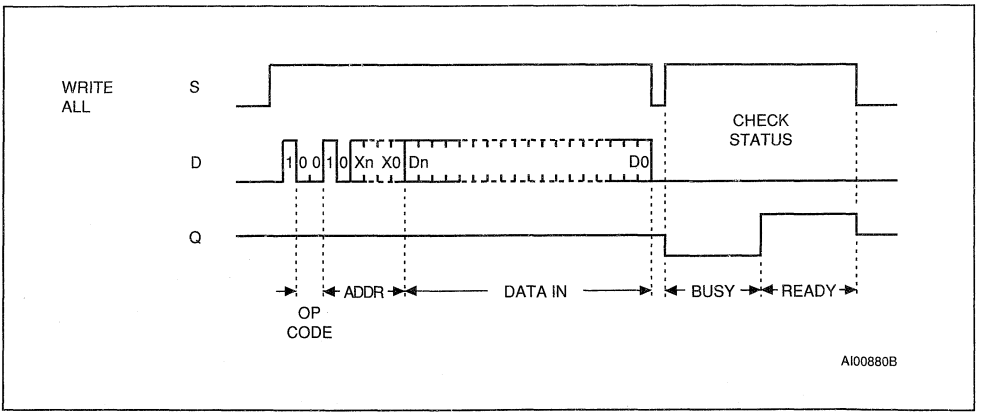
next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C56 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 7 for x16 org. and 8 for x8 org.
2. Xn: n = 5 for x16 org. and 6 for x8 org.

Figure 8. WRAL Sequence



Note: 1. Xn: n = 5 for x16 org. and 6 for x8 org.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C56 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction.

Write All

The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C56 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C56 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C56 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C56 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader may also refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

ORDERING INFORMATION SCHEME

Example: ST93C56 M 1 013TR

Package		Temperature Range		Option	
B	PSDIP8 0.4 mm Frame	1	0 to 70 °C	013TR	Tape & Reel Packaging
M	SO8	3 *	–40 to 125 °C		
		6	–40 to 85 °C		

Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

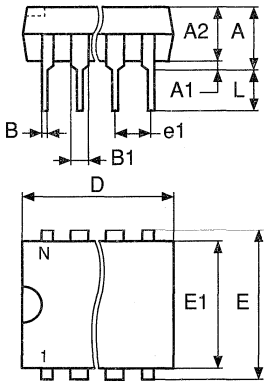
For a list of available options (Package, Temperature Range etc...) refer to the the current Memory Shortform catalogue.

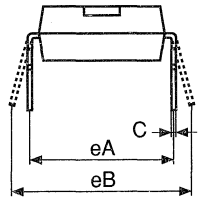
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8





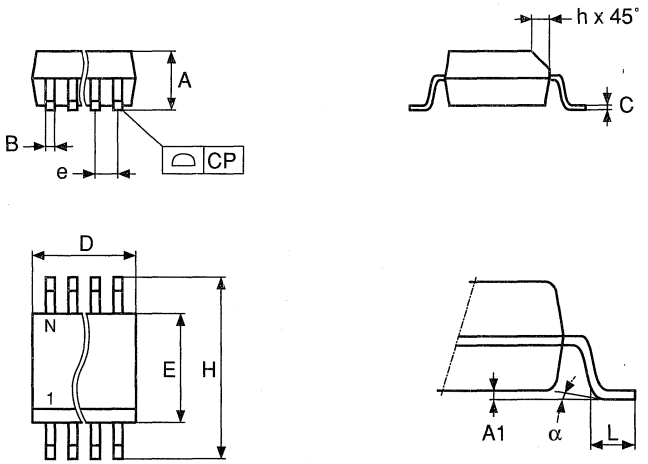
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



SO-a

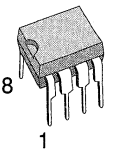
Drawing is out of scale

SGS-THOMSON MICROELECTRONICS

ST93C66

SERIAL ACCESS MICROWIRE BUS 4K (256 x 16 or 512 x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- DUAL ORGANIZATION: 256 x 16 or 512 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

SO8 (M)

DESCRIPTION

The ST93C66 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input (D).

The memory is divided into either 512 x 8 bit bytes or 256 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data contained at this address is then clocked out serially.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

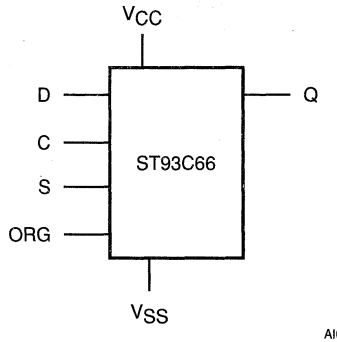
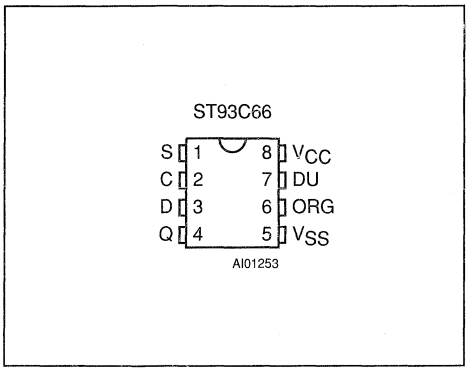
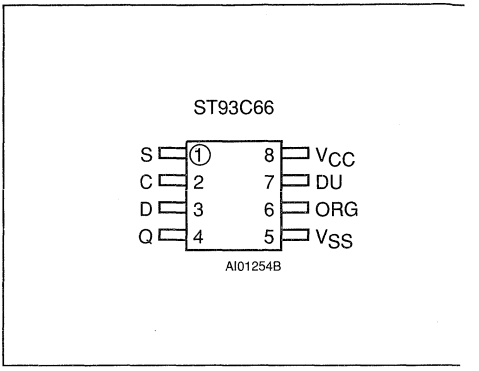


Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			7000	V
	Electrostatic Discharge Voltage (Machine model) (3)			1000	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C66 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 4096 bits long, or continuously as the address counter automatically rolls over to '00' when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 512 bytes or 256 words.

After the start of the programming cycle, a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

The design of the ST93C66 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 10 years.

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

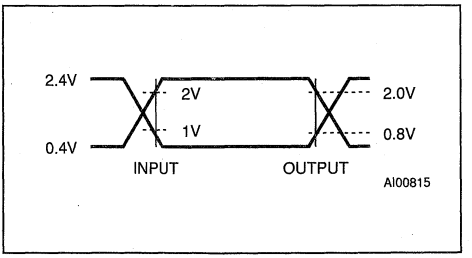


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ±10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ±10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	tDIH	Clock High to Input Transition		200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
tw	t_{WP}	Erase/Write Cycle time			10	ms
fc	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

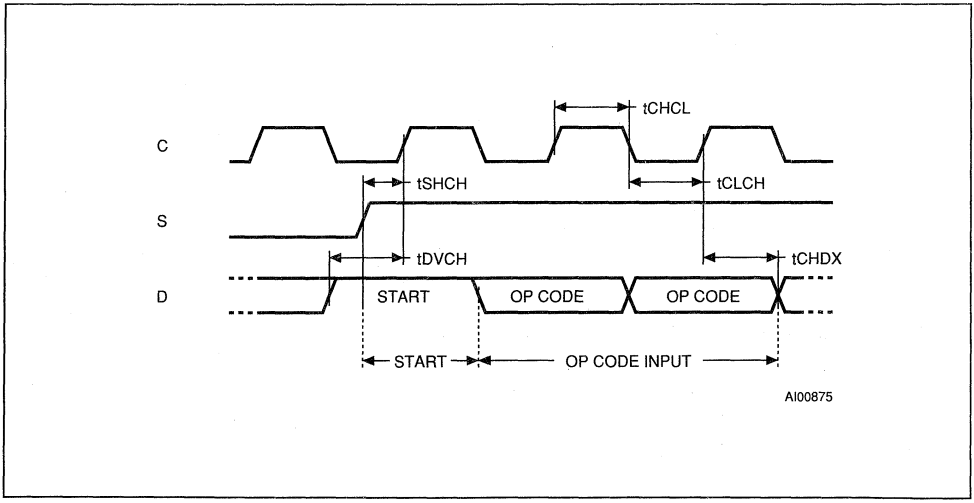
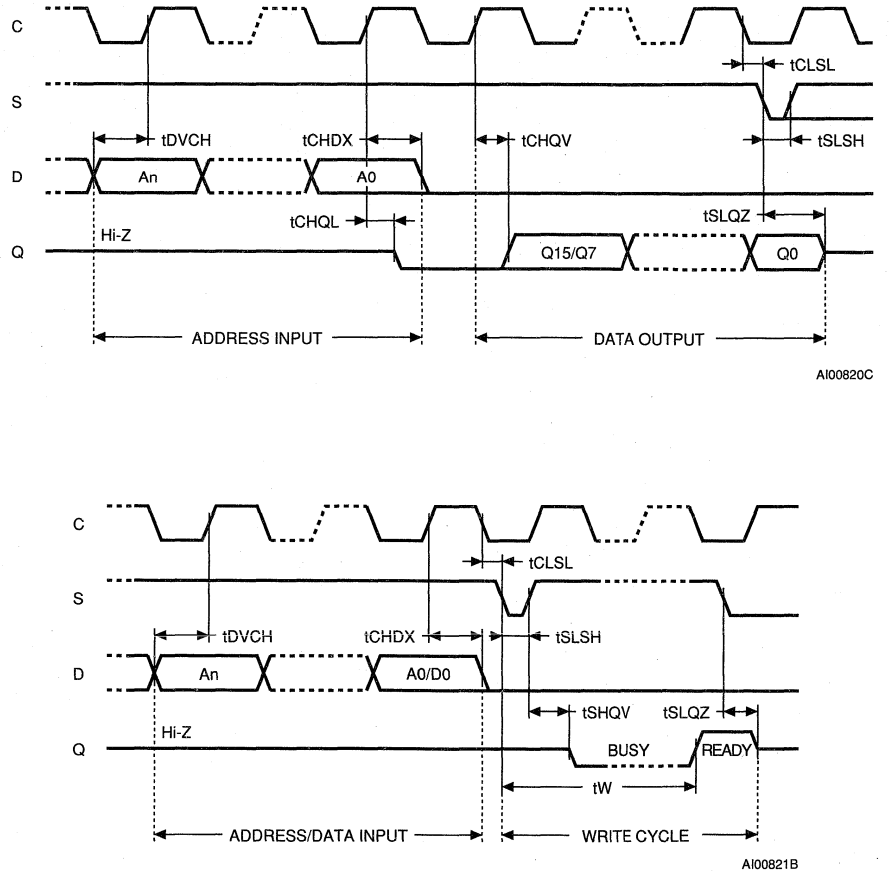


Figure 5. Synchronous Timing, Read or Write



MEMORY ORGANIZATION

The ST93C66 is organized as 512 bytes x 8 bits or 256 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C66 is in standby mode, the ORG input should be unconnected or set to either V_{SS} or V_{CC} in order to achieve the minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied, before applying any logic signal.

INSTRUCTIONS

The ST93C66 has seven instructions, as shown in Table 6. The op-codes of the instructions are made up of 2 bits. The op-code is followed by an address for the byte/word which is eight bits long for the x16 organization or nine bits long for the x8 organization. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that tha Clock C is low). The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C66 as a Start bit.

Remark. *A rising edge of Chip Select (S) when both inputs Clock (C) and Data Input (D) are high is also decoded as a Start bit. However, it is preferable not to use such a sequence.*

The ST93C66 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first, followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C66 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C66 enters the Disable mode. When the EWEN instruction is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset threshold. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle.

The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

If the ST93C66 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction.

Write

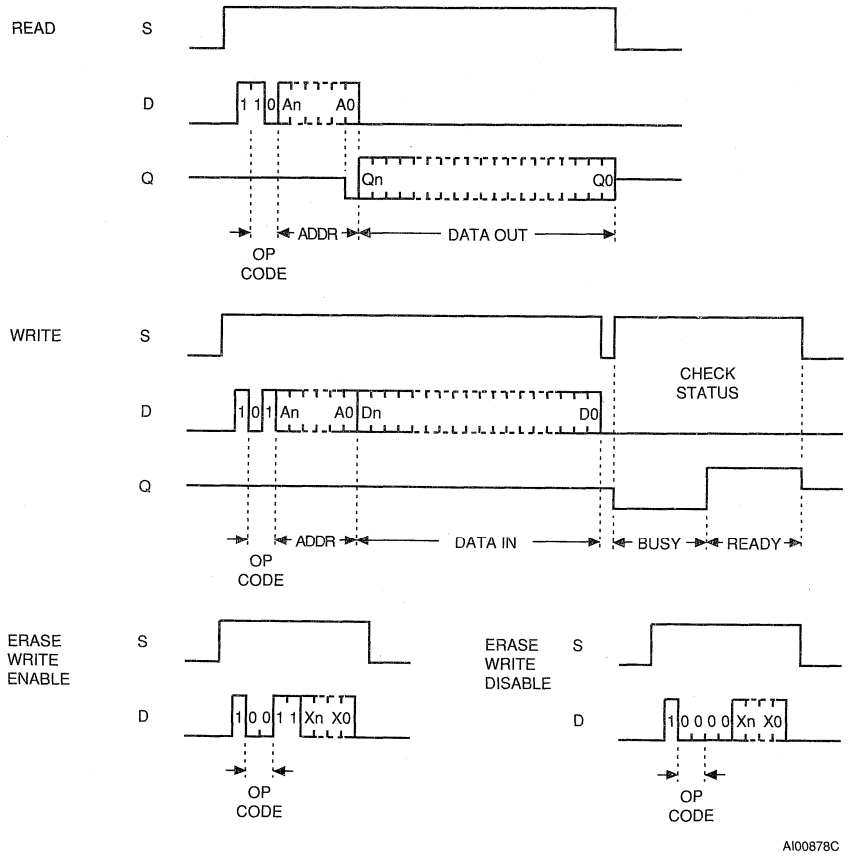
The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0) (1)	Data	x16 Org Address (ORG = 1) (1)	Data
READ	Read Data from Memory	10	A8-A0	Q7-Q0	A7-A0	Q15-Q0
WRITE	Write Data to Memory	01	A8-A0	D7-D0	A7-A0	D15-D0
EWEN	Erase/Write Enable	00	11XXX XXXX		11XX XXXX	
EWDS	Erase/Write Disable	00	00XXX XXXX		00XX XXXX	
ERASE	Erase Byte or Word	11	A8-A0		A7-A0	
ERAL	Erase All Memory	00	10XXX XXXX		10XX XXXX	
WRAL	Write All Memory with same Data	00	01XXX XXXX	D7-D0	01XX XXXX	D15-D0

Note: 1. X = don't care bit.

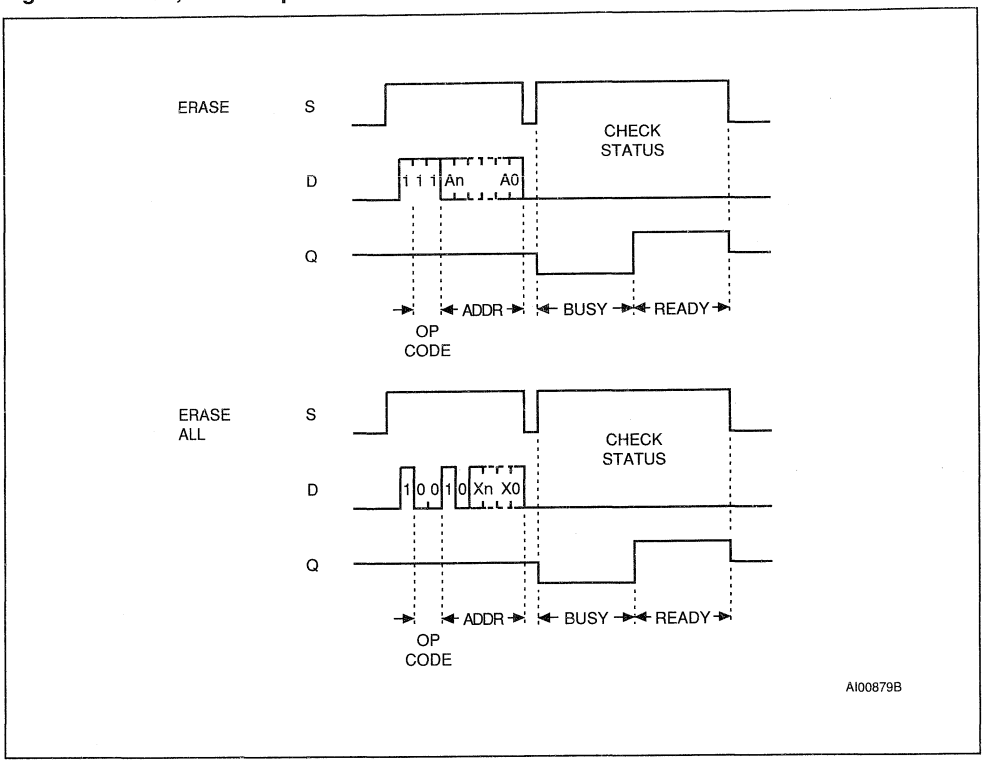
Figure 6. READ, WRITE, EWEN, EWDS Sequences



Notes: 1. An: n = 7 for x16 org. and 8 for x8 org.
2. Xn: n = 5 for x16 org. and 6 for x8 org.

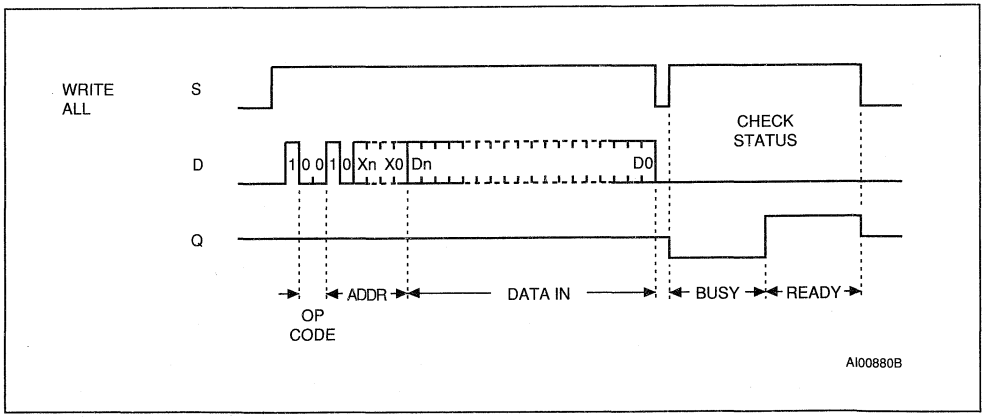
next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C66 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 7 for x16 org. and 8 for x8 org.
2. Xn: n = 5 for x16 org. and 6 for x8 org.

Figure 8. WRAL Sequence



Note: 2. Xn: n = 5 for x16 org. and 6 for x8 org.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C66 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction: the WRAL instruction DOES NOT perform an automatic erase before writing. The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C66 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C66 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C66 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C66 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader may also refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

ORDERING INFORMATION SCHEME

Example: ST93C66 M 3 TR

Package		Temperature Range		Option	
B	PSDIP8 0.4 mm Frame	1	0 to 70 °C	TR	Tape & Reel Packing
M	SO8	3 *	–40 to 125 °C		
		6	–40 to 85 °C		

Note: 3 * Temperature range on request only.

Parts are shipped with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

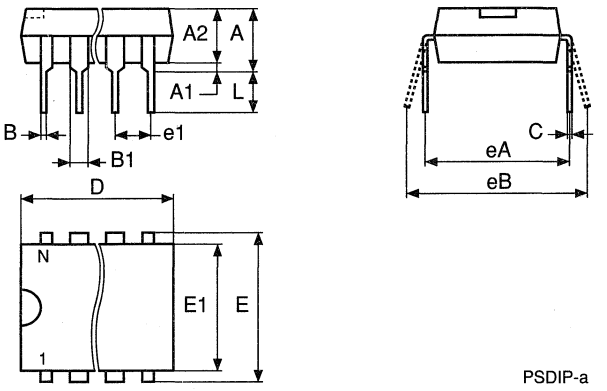
For a list of available options (Package, Temperature Range etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



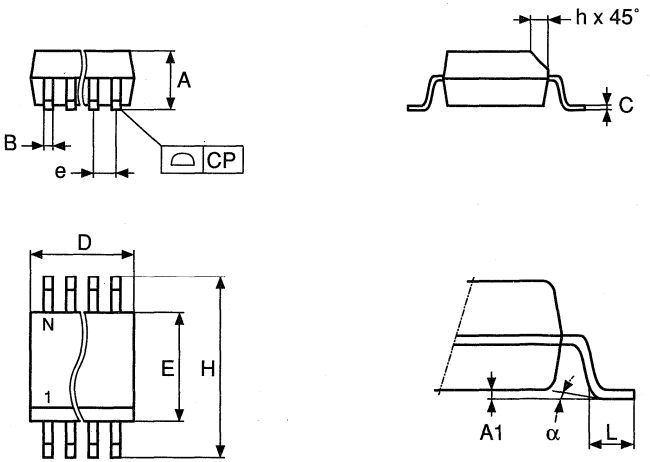
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8

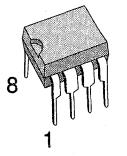


SO-a

Drawing is out of scale

SERIAL ACCESS MICROWIRE BUS 1K (64 x 16) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 3V to 5.5V for the ST93CS46
  - 2.5V to 5.5V for the ST93CS47
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 WORDS)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.4mm Frame

SO8 (M)

DESCRIPTION

The ST93CS46 and ST93CS47 are 1K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input D and output Q.

The 1K bit memory is organized as 64 x 16 bit words.The memory is accessed by a set of instructions which include Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer.

The data is then clocked out serially. The address pointer is automatically incremented after the data

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

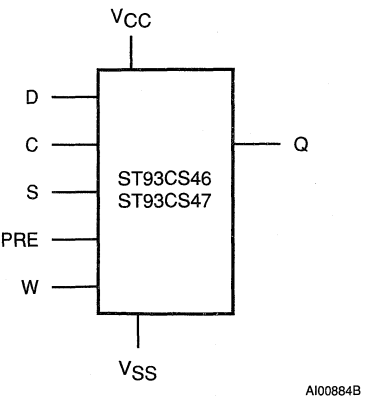


Figure 2A. DIP Pin Connections

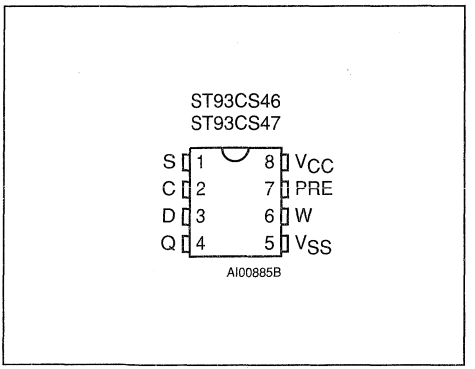


Figure 2B. SO Pin Connections

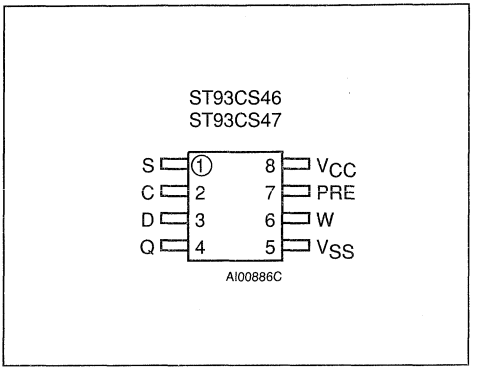


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			3000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

is output and, if the Chip Select input (S) is held High, the ST93CS46/47 can output a sequential stream of data words. In this way, the memory can be read as a data stream of 16 to 1024 bits, or continuously as the address counter automatically rolls over to 00 when the highest address is reached. Within the time required by a programming cycle (t_W), up to 4 words may be written with the help of the Page Write instruction; the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programing bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at one time into one of the 64 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area.

After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when the Chip Select (S) input pin is driven High.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

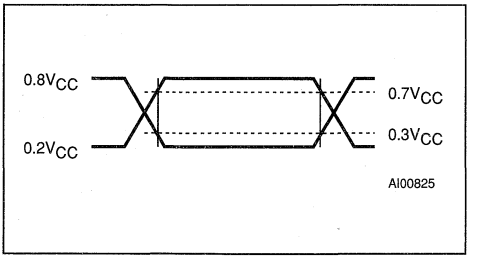


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS46 and V_{CC} = 2.5V to 5.5V for ST93CS47)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}		50	µA
V_{IL}	Input Low Voltage (ST93CS46,47)	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
	Input Low Voltage (ST93CS46)	$3V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
	Input Low Voltage (ST93CS47)	$2.5V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage (ST93CS46,47)	$4.5V \le V_{CC} \le 5.5V$	2	V_{CC} + 1	V
	Input High Voltage (ST93CS46)	$3V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
	Input High Voltage (ST93CS47)	$2.5V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS46 and V_{CC} = 2.5V to 5.5V for ST93CS47)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

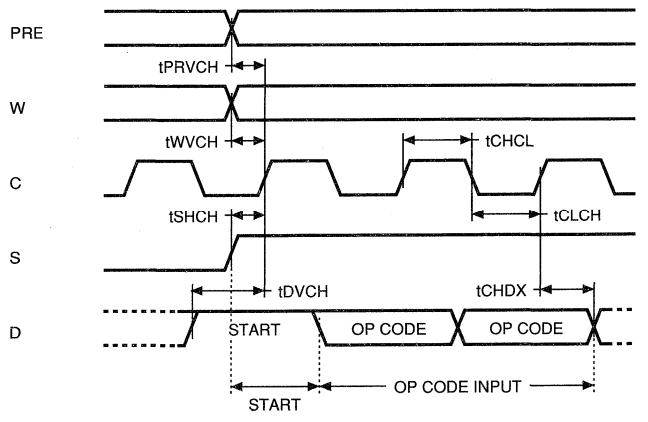
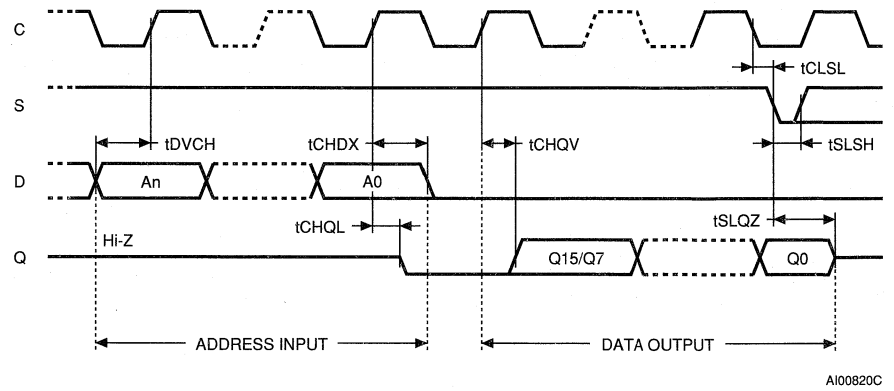
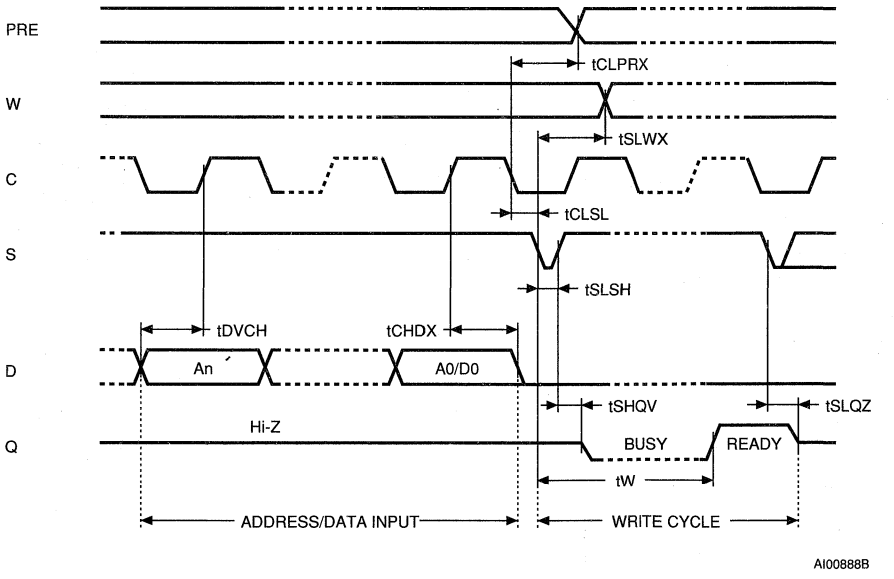


Figure 5. Synchronous Timing, Read or Write





POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93CS46/47 has eleven instructions, as shown in Table 6. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that the Clock C is low), followed by a '1' read on D input during the rising edge of the clock C. The op-codes of the instructions are made up of the 2 following bits. Some instructions use only these first two bits, others use also the first two bits of the address field to define the op-code. The address field is six bits long (A5-A0).

The ST93CS46/47 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first.

Table 6. Instruction Set

Instruction	Description	W Pin (1)	PRE Pin	Op Code	Address (1)	Data	Additional Information
READ	Read Data from Memory	X	'0'	10	A5-A0	Q15-Q0	
WRITE	Write Data to Memory	'1'	'0'	01	A5-A0	D15-D0	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	11	A5-A0	D15-D0	Write is executed if all the addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	00	01XXXX	D15-D0	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	00	11XXXX		
WDS	Write Disable	X	'0'	00	00XXXX		
PRREAD	Protect Register Read	X	'1'	10	XXXXXX	Q8-Q0	Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	01	A5-A0		Data above specified address A5-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	11	111111		Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	00	11XXXX		
PRDS	Protect Register Disable	'1'	'1'	00	000000		OTP bit is set permanently

Note: 1. X = don't care bit.

Output data changes are triggered by the Low to High transition of the Clock (C). The ST93CS46/47 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed, the Write Disable instruction (WDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93CS46/47 enters the Disable mode. When the Write Enable instruction (WEN) is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle.

The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is followed by the address and the word to be written. The Write Enable signal (W) must be held high during the WRITE instruction. Data input D is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle, providing that the address is NOT in the protected area. If the ST93CS46/47 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS46/47 is ready to receive a new instruction.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the Write instruction. Input address and data are read on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits A5-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same four upper order address bits as the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the ST93CS46/47 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS46/47 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write instruction. Input address and data are read on the Low to High transition of the clock. If the ST93CS46/47 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS46/47 is ready to receive a new instruction.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The ST93CS46/47 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the protection of the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS; this PREN instruction being used together with the signals applied on the input pins PRE

Figure 6. READ, WRITE, WEN, WDS Sequences

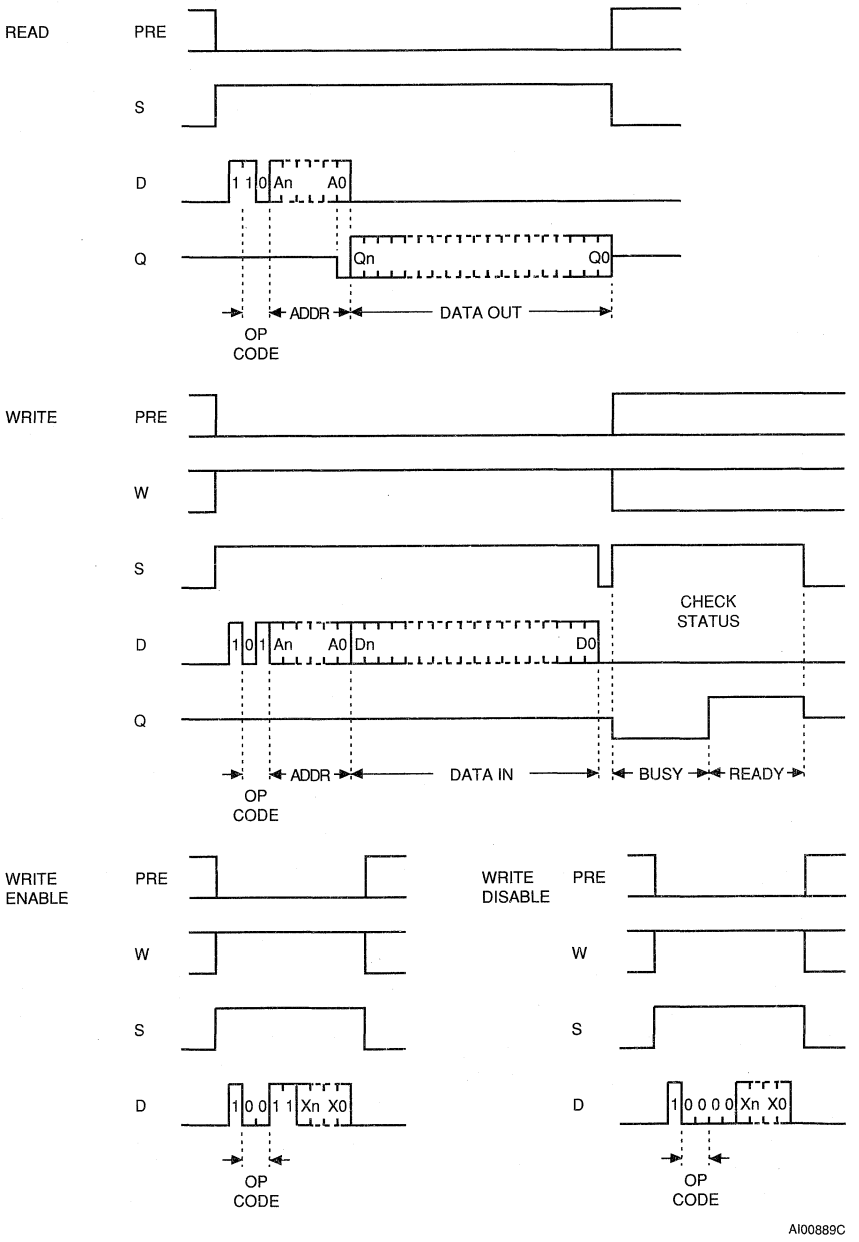
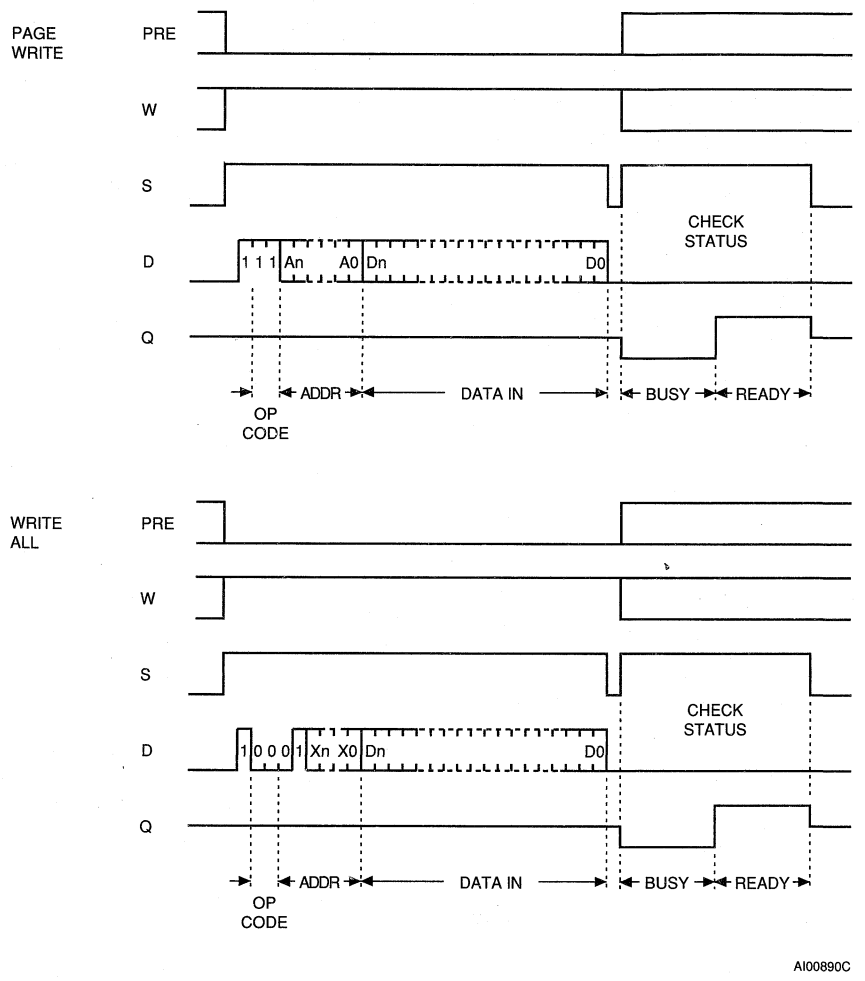


Figure 7. PAWRITE, WRALL Sequences



MEMORY WRITE PROTECTION (cont'd)

(Protect Register Enable pin) and W (Write Enable).

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q); when the OTP bit is not set, the Busy status appear on the Data output (Q).

A PREN instruction must immediately precede the PRDS instruction.

READY/BUSY Status

When the ST93CS46/47 is performing the write cycle, the Busy signal (Q = 0) is returned if S is driven high, and the ST93CS46/47 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate, if S is driven high, that the ST93CS46/47 is ready to receive a new instruction. Once the ST93CS46/47 is Ready, the Data Output Q is set to '1' until a new Start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

Figure 8. PRREAD, PRWRITE, PREN Sequences

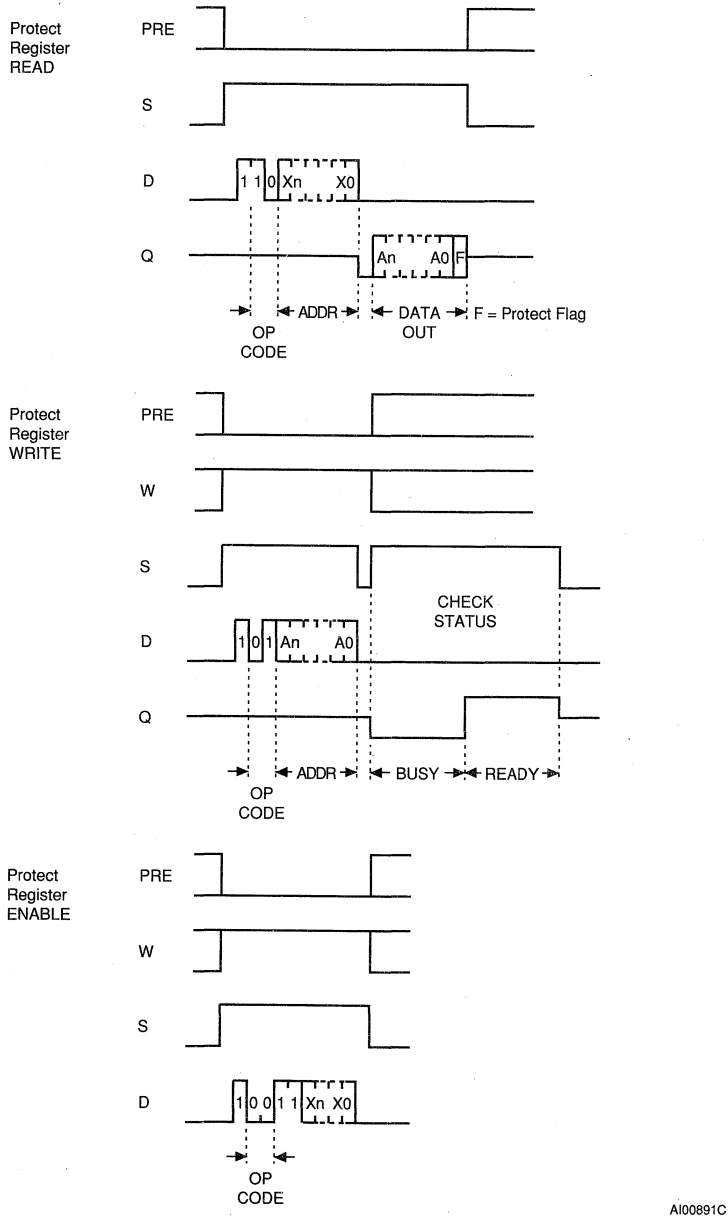
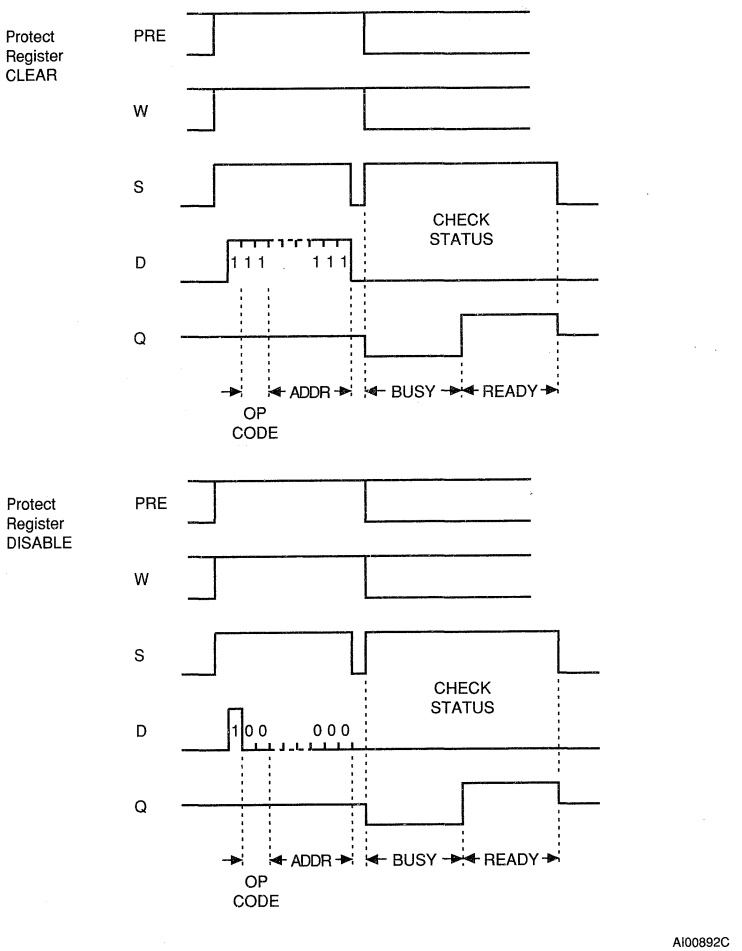
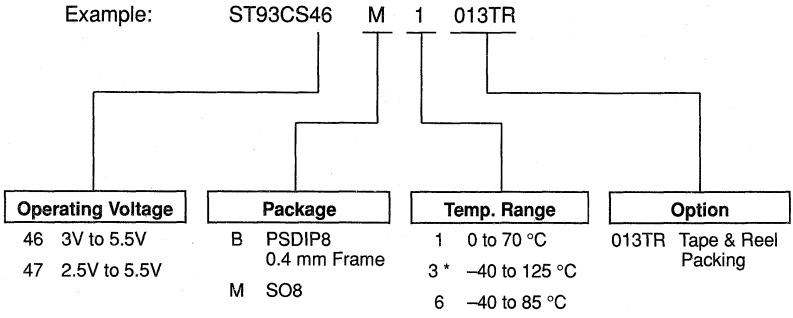


Figure 9. PRCLEAR, PRDS Sequences



ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on request only.

Parts are shipped with the memory content set at all "1's" (FFFFh).

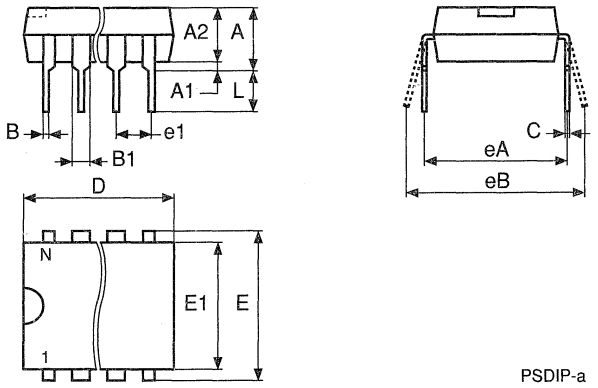
For a list of available options (Operating Voltage, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



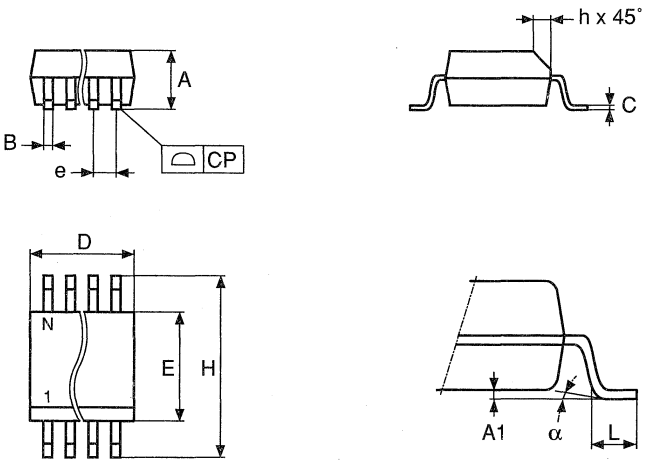
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8

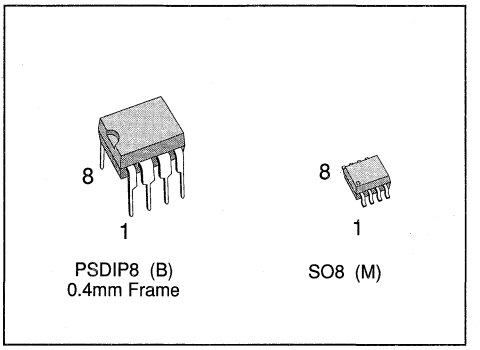


SO-a

Drawing is out of scale

SERIAL ACCESS MICROWIRE BUS 2K (128 x 16) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 3V to 5.5V for the ST93CS56
  - 2.5V to 5.5V for the ST93CS57
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 WORDS)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



DESCRIPTION

The ST93CS56 and ST93CS57 are 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input D and output Q.

The 2K bit memory is organized as 128 x 16 bit words.The memory is accessed by a set of instructions which include Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer.

The data is then clocked out serially. The address pointer is automatically incremented after the data

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

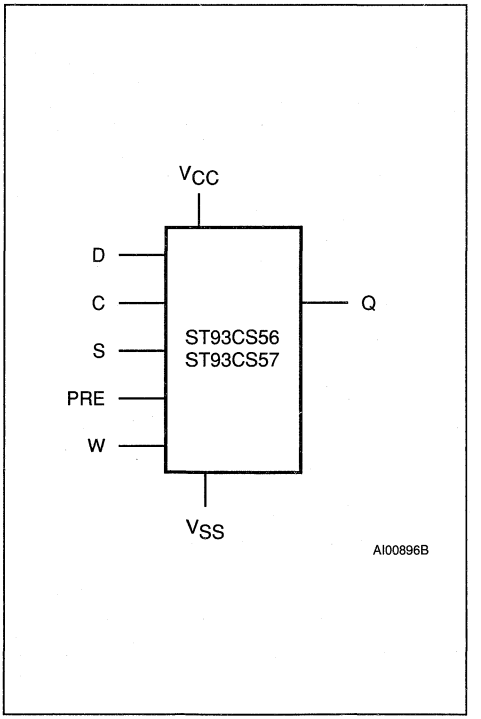


Figure 2A. DIP Pin Connections

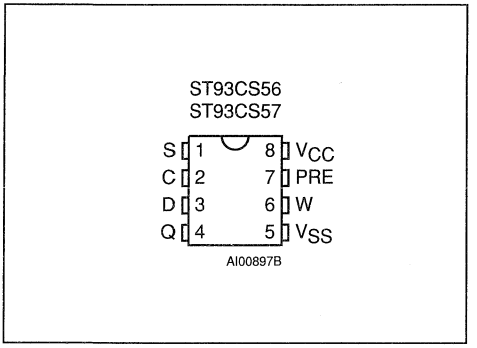


Figure 2B. SO Pin Connections

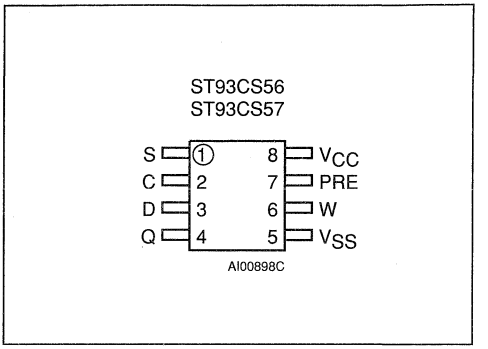


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			3000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

is output and, if the Chip Select input (S) is held High, the ST93CS56/57 can output a sequential stream of data words. In this way, the memory can be read as a data stream of 16 to 2048 bits, or continuously as the address counter automatically rolls over to 00 when the highest address is reached. Within the time required by a programming cycle (t_W), up to 4 words may be written with the help of the Page Write instruction; the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programing bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at one time into one of the 128 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area.

After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when the Chip Select (S) input pin is driven High.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

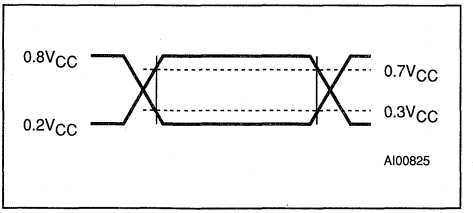


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS56 and V_{CC} = 2.5V to 5.5V for ST93CS57)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}		50	µA
V_{IL}	Input Low Voltage (ST93CS56,57)	4.5V ≤ V_{CC} ≤ 5.5V	–0.1	0.8	V
	Input Low Voltage (ST93CS56)	3V ≤ V_{CC} ≤ 5.5V	–0.1	0.2 V_{CC}	V
	Input Low Voltage (ST93CS57)	2.5V ≤ V_{CC} ≤ 5.5V	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage (ST93CS56,57)	4.5V ≤ V_{CC} ≤ 5.5V	2	V_{CC} + 1	V
	Input High Voltage (ST93CS56)	3V ≤ V_{CC} ≤ 5.5V	0.8 V_{CC}	V_{CC} + 1	V
	Input High Voltage (ST93CS57)	2.5V ≤ V_{CC} ≤ 5.5V	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS56 and V_{CC} = 2.5V to 5.5V for ST93CS57)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

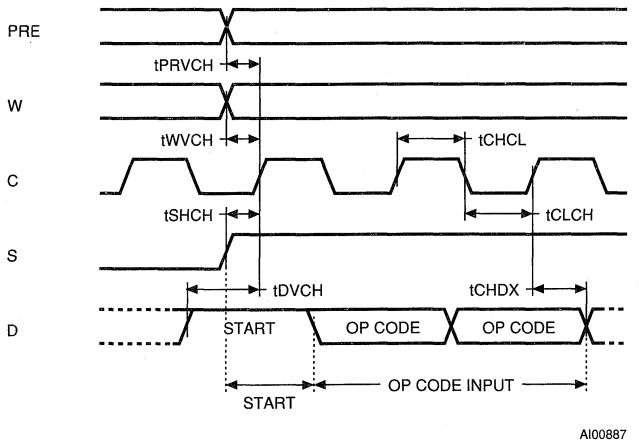
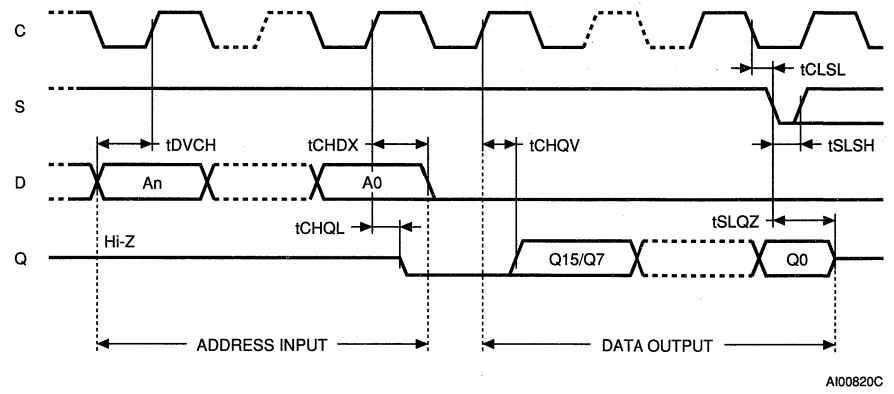
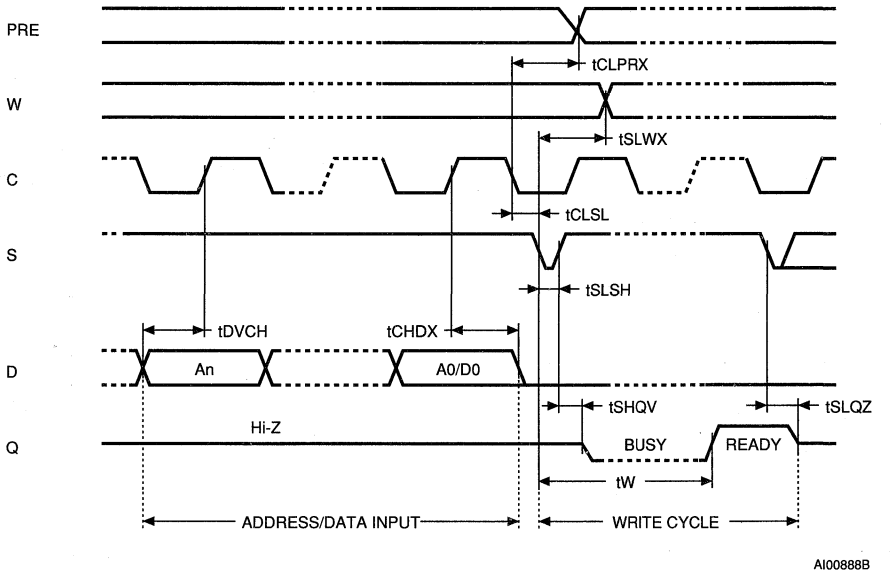


Figure 5. Synchronous Timing, Read or Write





POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93CS56/57 has eleven instructions, as shown in Table 6. Each instruction is composed of a 2 bit op-code and an 8 bit address. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that the Clock C is low). The data input D is then sampled upon the following rising edges of the clock C until a '1' is sampled and decoded by the ST93CS56/57 as a Start bit.

The ST93CS56/57 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first.

Table 6. Instruction Set

Instruction	Description	W pin (1)	PRE pin	Op Code	Address (1, 2)	Data	Additional Information
READ	Read Data from Memory	X	'0'	10	A7-A0	Q15-Q0	
WRITE	Write Data to Memory	'1'	'0'	01	A7-A0	D15-D0	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	11	A7-A0	D15-D0	Write is executed if all the addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	00	01XX XXXX	D15-D0	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	00	11XX XXXX		
WDS	Write Disable	X	'0'	00	00XX XXXX		
PRREAD	Protect Register Read	X	'1'	10	XXXX XXXX	Q8-Q0	Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	01	A7-A0		Data above specified address A7-A0 are protected (2)
PRCLEAR	Protect Register Clear	'1'	'1'	11	1111 1111		Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	00	11XX XXXX		
PRDS	Protect Register Disable	'1'	'1'	00	0000 0000		OTP bit is set permanently

Notes: 1. X = don't care bit.
2. Address bit A7 is not decoded by the ST93CS56/57.

Output data changes are triggered by the Low to High transition of the Clock (C). The ST93CS56/57 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed, the Write Disable instruction (WDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93CS56/57 enters the Disable mode. When the Write Enable instruction (WEN) is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle.

The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is followed by the address and the word to be written. The Write Enable signal (W) must be held high during the WRITE instruction. Data input D is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle, providing that the address is NOT in the protected area. If the ST93CS56/57 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS56/57 is ready to receive a new instruction.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the Write instruction. Input address and data are read on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same five upper order address bits as the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the ST93CS56/57 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS56/57 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write instruction. Input address and data are read on the Low to High transition of the clock. If the ST93CS56/57 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS56/57 is ready to receive a new instruction.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The ST93CS56/57 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the protection of the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS; this PREN instruction being used together with the signals applied on the input pins PRE (Protect Register Enable pin) and W (Write Enable).

Figure 6. READ, WRITE, WEN, WDS Sequences

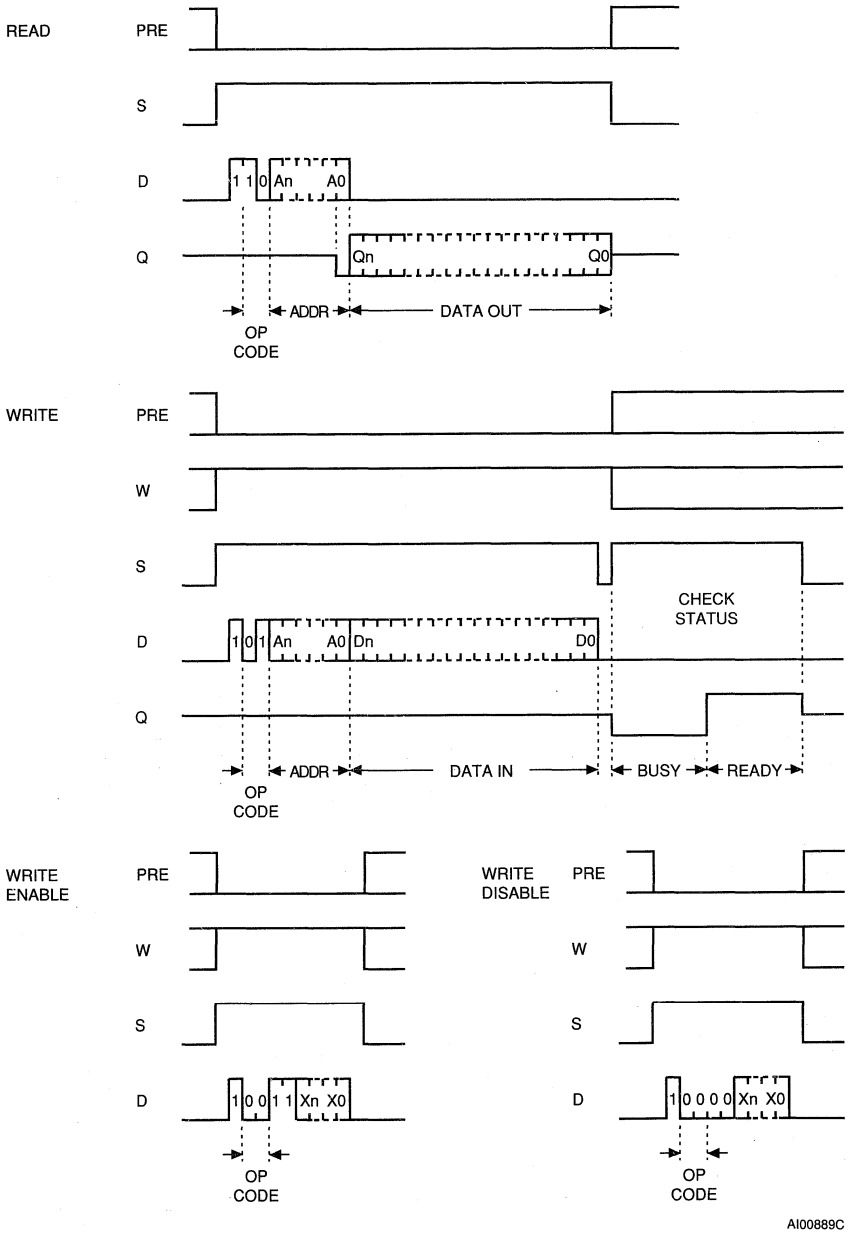
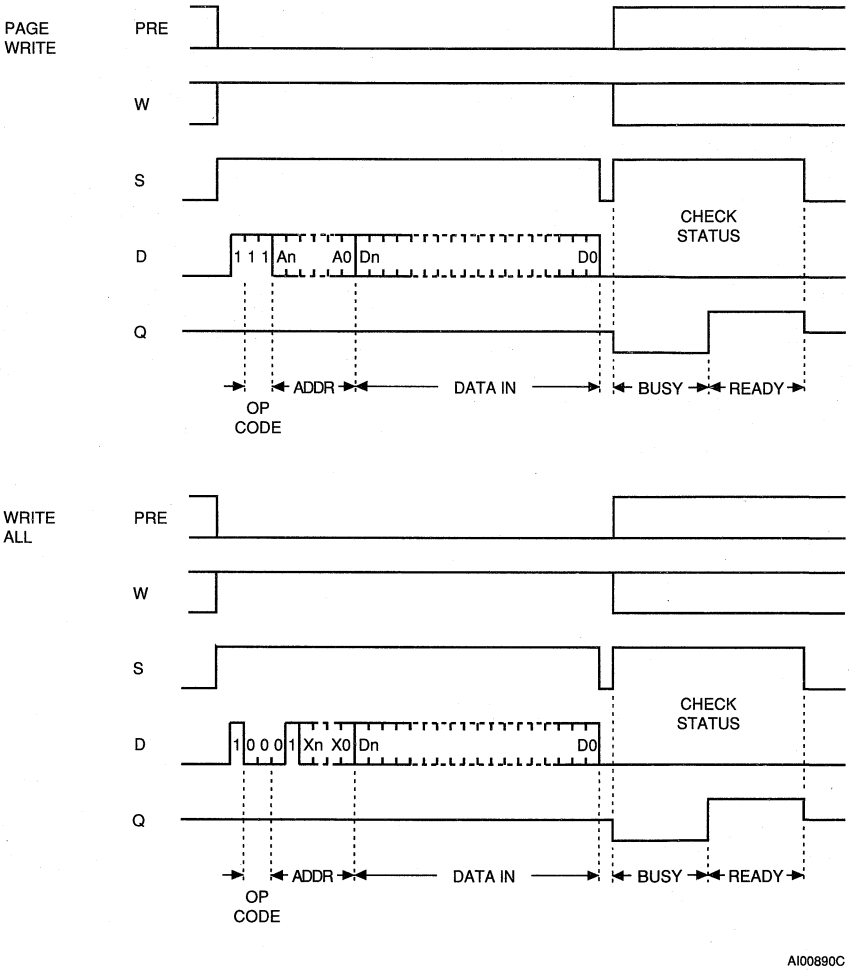


Figure 7. PAWRITE, WRALL Sequences



MEMORY WRITE PROTECTION (cont'd)

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q); when the OTP bit is not set, the Busy status appear on the Data output (Q).

A PREN instruction must immediately precede the PRDS instruction.

READY/BUSY Status

When the ST93CS56/57 is performing the write cycle, the Busy signal (Q = 0) is returned if S is driven high, and the ST93CS56/57 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate, if S is driven high, that the ST93CS56/57 is ready to receive a new instruction. Once the ST93CS56/57 is Ready, the Data Output Q is set to '1' until a new Start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

Figure 8. PRREAD, PRWRITE, PREN Sequences

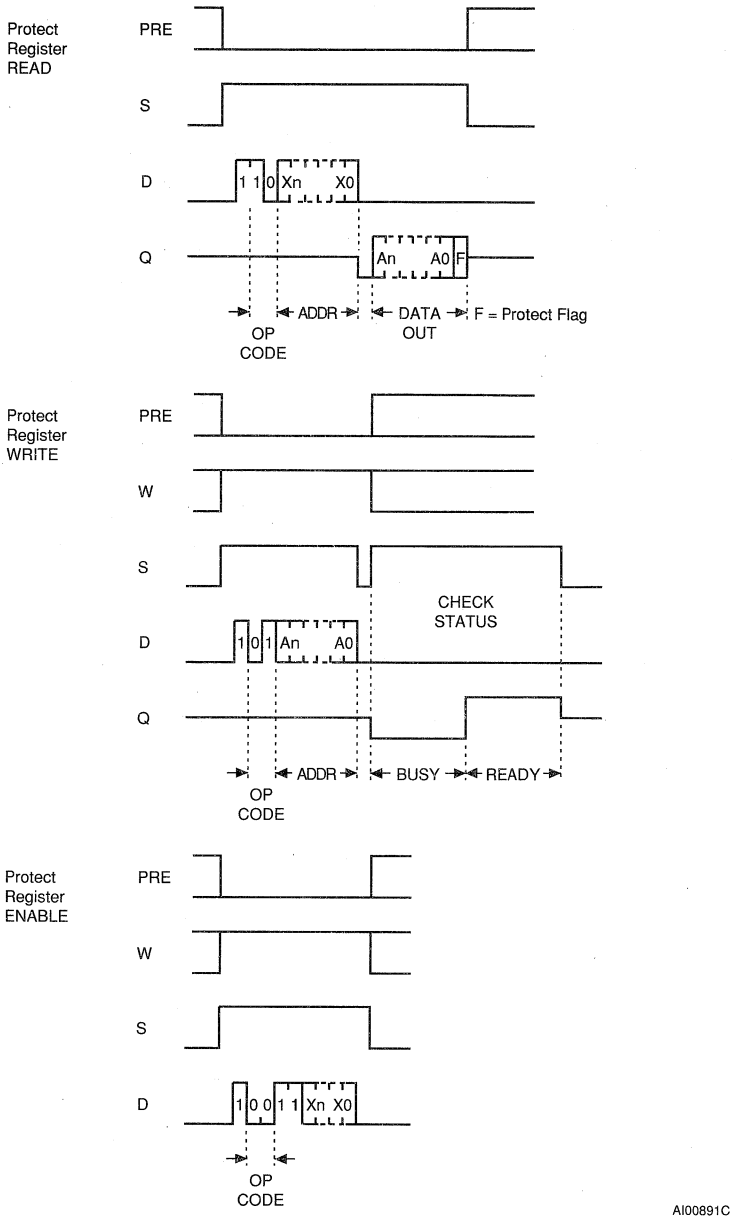
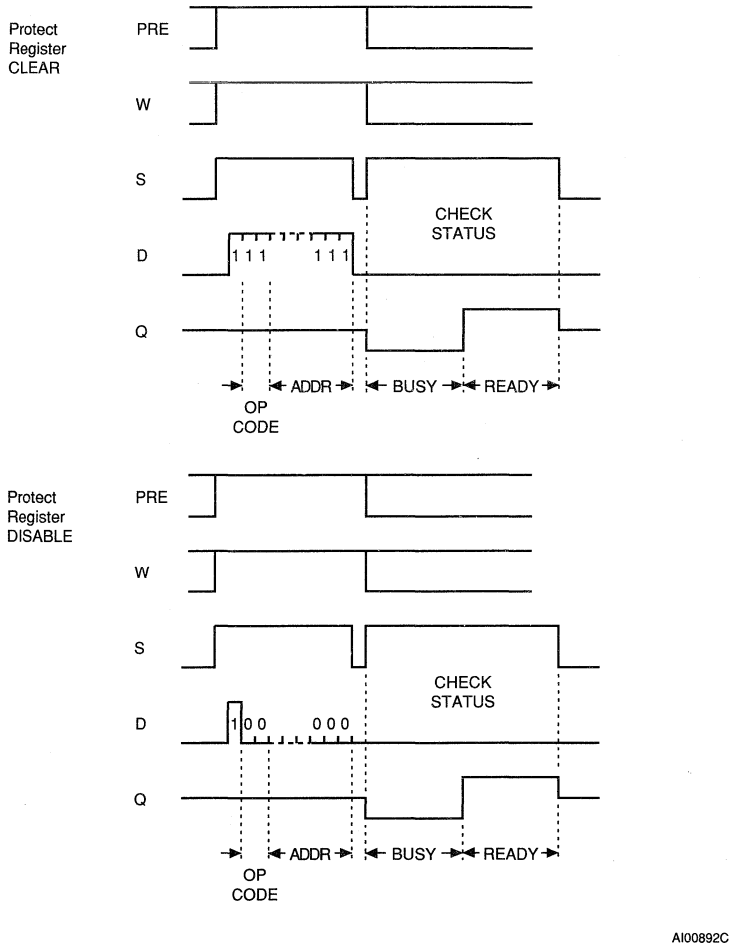
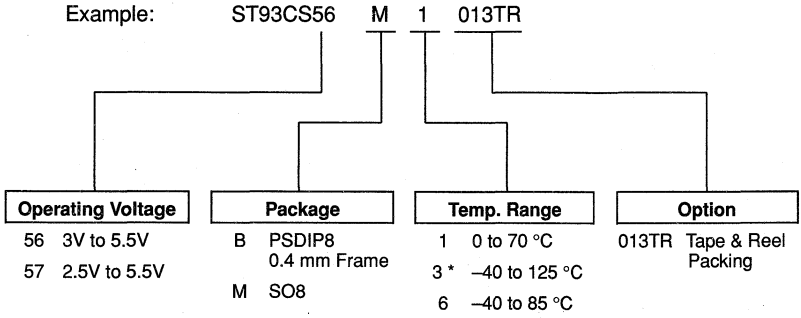


Figure 9. PRCLEAR, PRDS Sequences



ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFFFh).

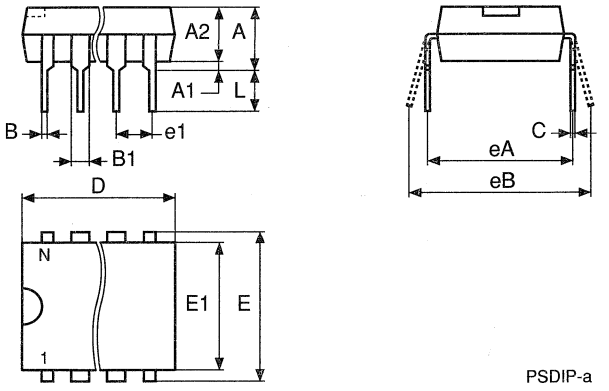
For a list of available options (Operating Voltage, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



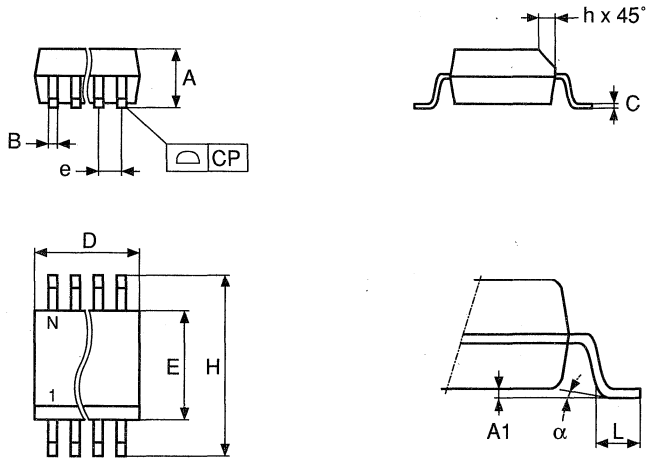
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8

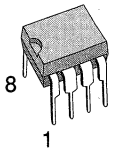


SO-a

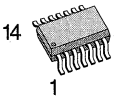
Drawing is out of scale

SERIAL ACCESS MICROWIRE BUS 4K (256 x 16) EEPROM

- 1 MILLION ERASE/WRITE CYCLES, with 10 YEARS DATA RETENTION
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE
  - 3V to 5.5V for the ST93CS66
  - 2.5V to 5.5V for the ST93CS67
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 WORDS)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME



PSDIP8 (B)
0.25mm Frame



SO14 (ML)

DESCRIPTION

The ST93CS66 and ST93CS67 are 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed through a serial input D and output Q.

The 4K bit memory is organized as 256 x 16 bit words.The memory is accessed by a set of instructions which include Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer.

The data is then clocked out serially. The address pointer is automatically incremented after the data

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

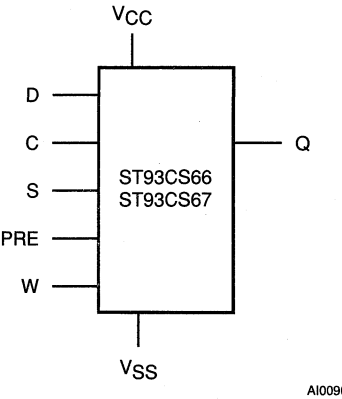


Figure 2A. DIP Pin Connections

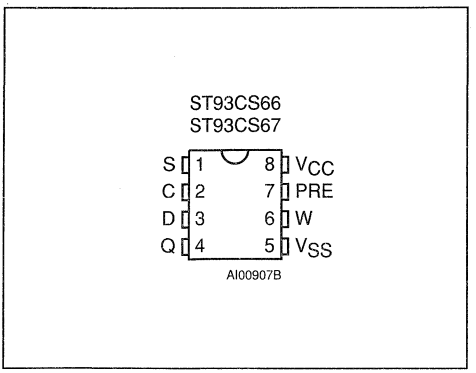
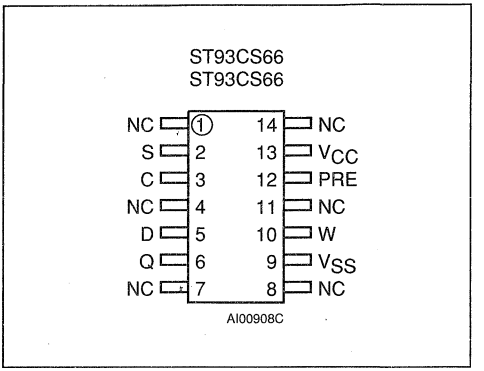


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO14 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			2000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

is output and, if the Chip Select input (S) is held High, the ST93CS66/67 can output a sequential stream of data words. In this way, the memory can be read as a data stream of 16 to 4096 bits, or continuously as the address counter automatically rolls over to 00 when the highest address is reached.

Within the time required by a programming cycle (t_W), up to 4 words may be written with the help of the Page Write instruction; the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programing bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at one time into one of the 256 words, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area. After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when the Chip Select (S) input pin is driven High.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

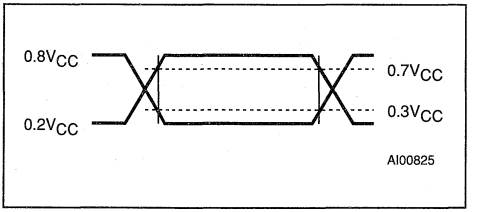


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS66 and V_{CC} = 2.5V to 5.5V for ST93CS67)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}		50	µA
V_{IL}	Input Low Voltage (ST93CS66,67)	$4.5V \le V_{CC} \le 5.5V$	–0.1	0.8	V
	Input Low Voltage (ST93CS66)	$3V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
	Input Low Voltage (ST93CS67)	$2.5V \le V_{CC} \le 5.5V$	–0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage (ST93CS66,67)	$4.5V \le V_{CC} \le 5.5V$	2	V_{CC} + 1	V
	Input High Voltage (ST93CS66)	$3V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
	Input High Voltage (ST93CS67)	$2.5V \le V_{CC} \le 5.5V$	0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics (T_A = 0 to 70° or, –40 to 85°C; V_{CC} = 3V to 5.5V for ST93CS66 and V_{CC} = 2.5V to 5.5V for ST93CS67)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High		50		ns
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition		100		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition		250		ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Transition		0		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z			300	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

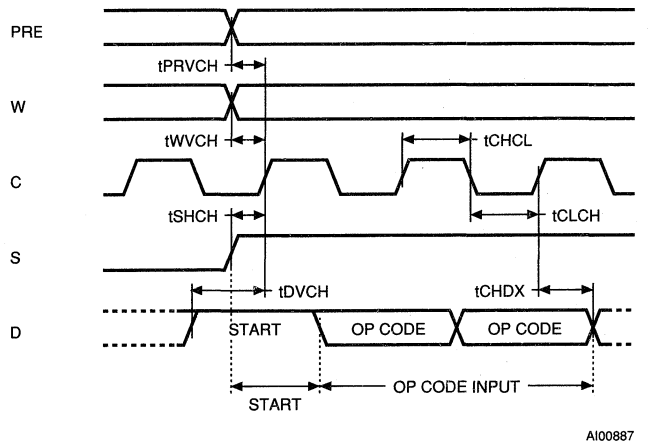
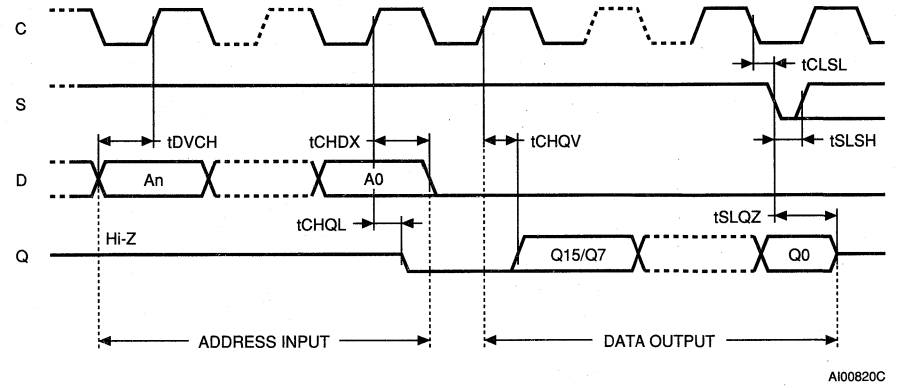
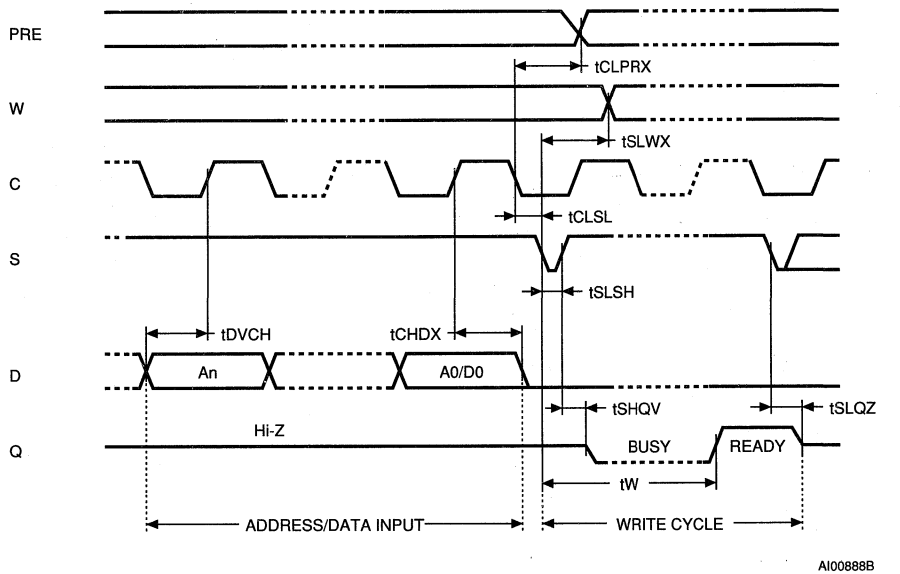


Figure 5. Synchronous Timing, Read or Write





POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93CS66/67 has eleven instructions, as shown in Table 6. Each instruction is composed of a 2 bit op-code and an 8 bit address. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that the Clock C is low). The data input D is then sampled upon the following rising edges of the clock C until a '1' is sampled and decoded by the ST93CS66/67 as a Start bit.

The ST93CS66/67 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first.

Table 6. Instruction Set

Instruction	Description	W pin (1)	PRE pin	Op Code	Address (1)	Data	Additional Information
READ	Read Data from Memory	X	'0'	10	A7-A0	Q15-Q0	
WRITE	Write Data to Memory	'1'	'0'	01	A7-A0	D15-D0	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	11	A7-A0	D15-D0	Write is executed if all the addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	00	01XX XXXX	D15-D0	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	00	11XX XXXX		
WDS	Write Disable	X	'0'	00	00XX XXXX		
PRREAD	Protect Register Read	X	'1'	10	XXXX XXXX	Q8-Q0	Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	01	A7-A0		Data above specified address A7-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	11	1111 1111		Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	00	11XX XXXX		
PRDS	Protect Register Disable	'1'	'1'	00	0000 0000		OTP bit is set permanently

Note: 1. X = don't care bit.

Output data changes are triggered by the Low to High transition of the Clock (C). The ST93CS66/67 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed, the Write Disable instruction (WDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93CS66/67 enters the Disable mode. When the Write Enable instruction (WEN) is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle.

The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is followed by the address and the word to be written. The Write Enable signal (W) must be held high during the WRITE instruction. Data input D is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C), in order to start the self-timed programming cycle, providing that the address is NOT in the protected area. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the Write instruction. Input address and data are read on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits A7-A2 remaining unchanged. Users must take care by software to ensure that the last word address has the same six upper order address bits as the initial address transmitted to avoid address roll-over.

After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C). The falling edge of Chip Select (S) initiates the internal, self-timed write cycle. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write instruction. Input address and data are read on the Low to High transition of the clock. If the ST93CS66/67 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93CS66/67 is ready to receive a new instruction.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The ST93CS66/67 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the protection of the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS; this PREN instruction being used together with the signals applied on the input pins PRE (Protect Register Enable pin) and W (Write Enable).

Figure 6. READ, WRITE, WEN, WDS Sequences

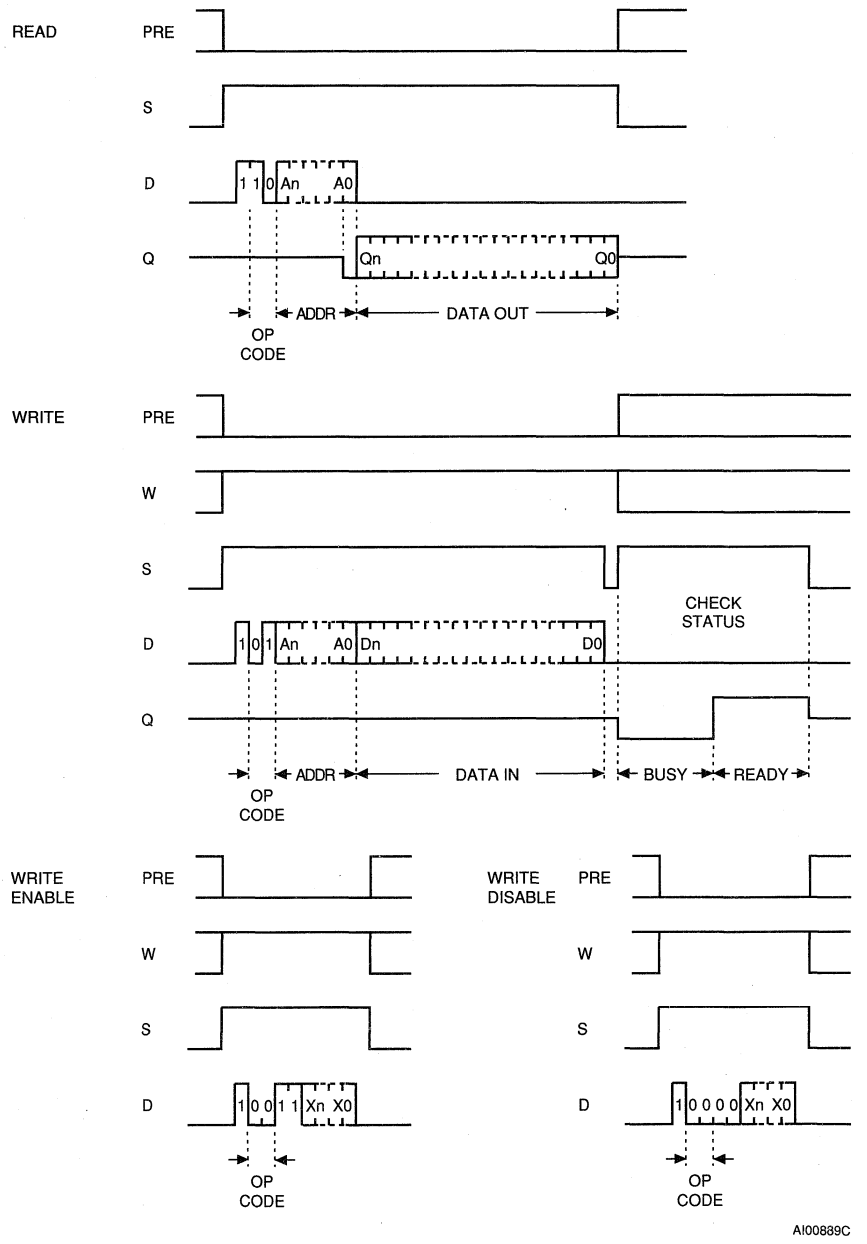
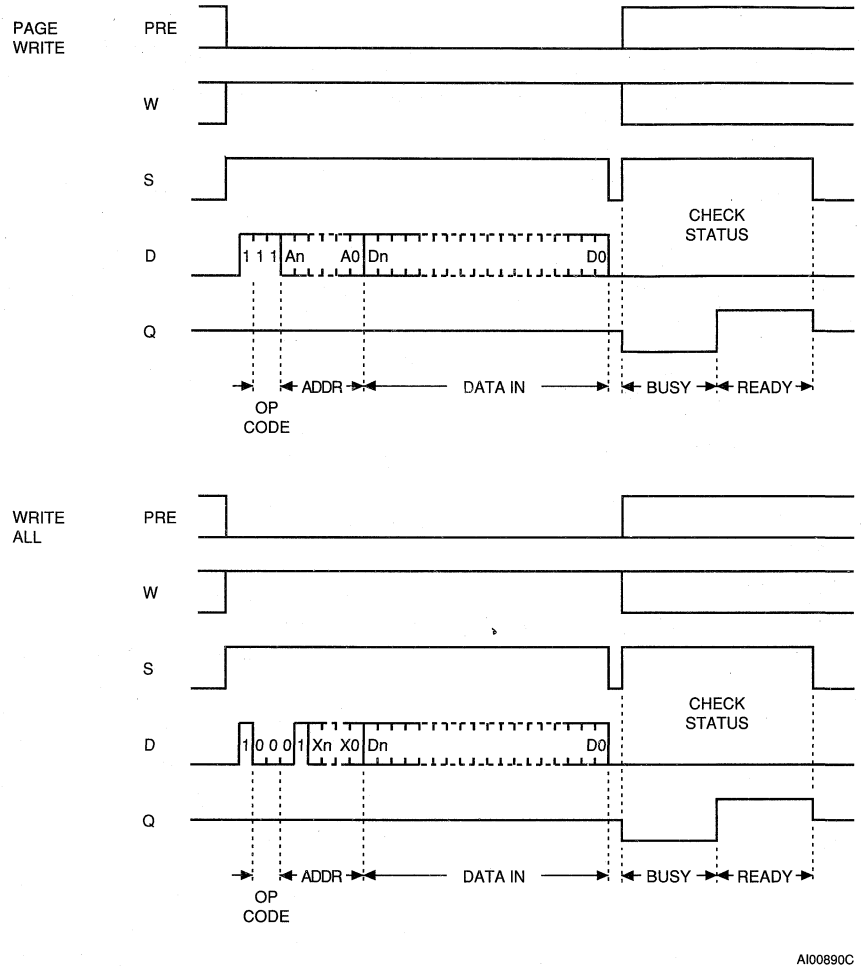


Figure 7. PAWRITE, WRALL Sequences



MEMORY WRITE PROTECTION (cont'd)

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction. As in the Read instruction a dummy '0' bit is output first.

Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q); when the OTP bit is not set, the Busy status appear on the Data output (Q).

A PREN instruction must immediately precede the PRDS instruction.

READY/BUSY Status

When the ST93CS66/67 is performing the write cycle, the Busy signal (Q = 0) is returned if S is driven high, and the ST93CS66/67 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate, if S is driven high, that the ST93CS66/67 is ready to receive a new instruction. Once the ST93CS66/67 is Ready, the Data Output Q is set to '1' until a new Start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

Figure 8. PRREAD, PRWRITE, PREN Sequences

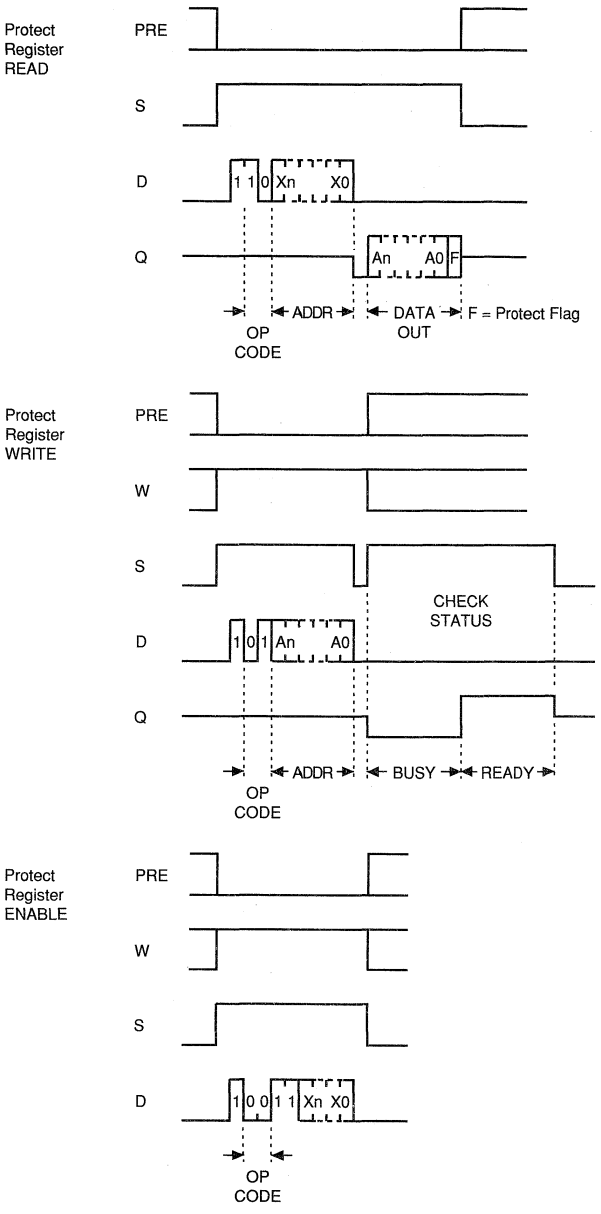
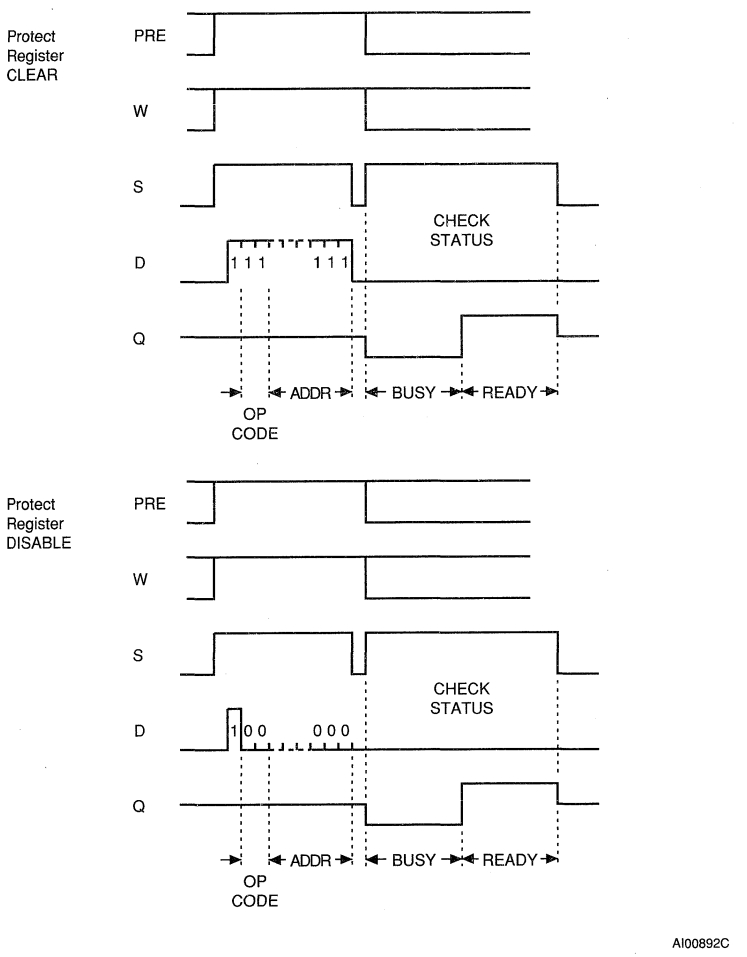
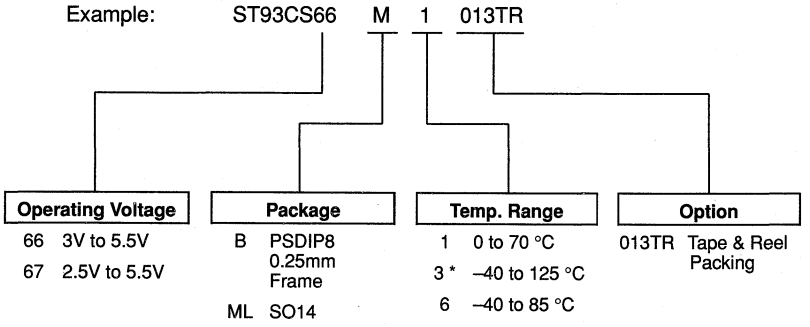


Figure 9. PRCLEAR, PRDS Sequences



ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on request only.

Parts are shipped with the memory content set at all "1's" (FFFFh).

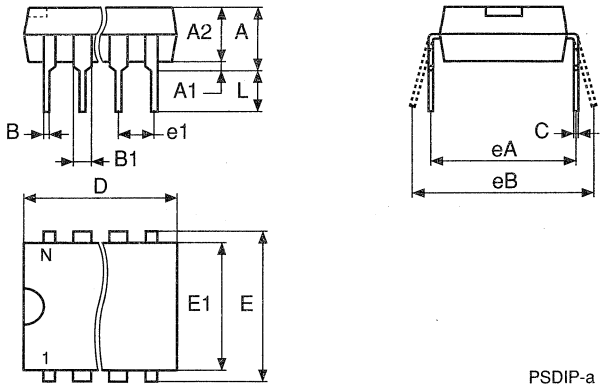
For a list of available options (Operating Voltage, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



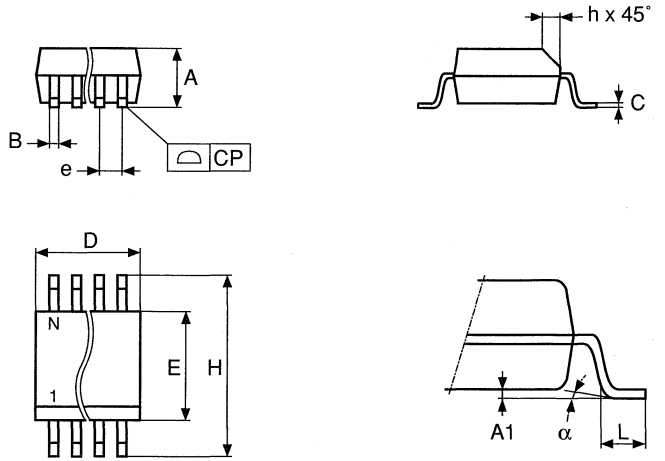
PSDIP-a

Drawing is out of scale

SO14 - 14 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		8.55	8.75		0.337	0.344
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.80		0.016	0.031
α		0°	8°		0°	8°
N	14			14		
CP			0.10			0.004

SO14



SO-a

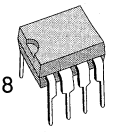
Drawing is out of scale

SERIAL ACCESS
SPI BUS EEPROM

SERIAL ACCESS SPI BUS 2K (256 x 8) EEPROM

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- ***The ST95P02 will be replaced shortly by the updated version ST95020***



PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

The ST95P02 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 2K bit memory is organised as 16 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

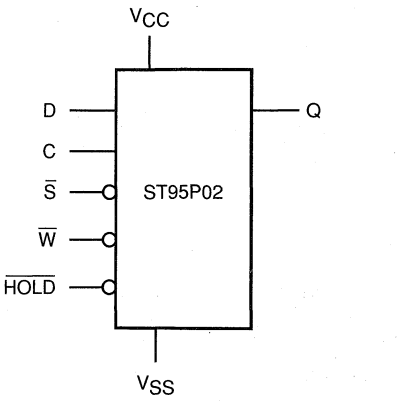


Figure 2A. DIP Pin Connections

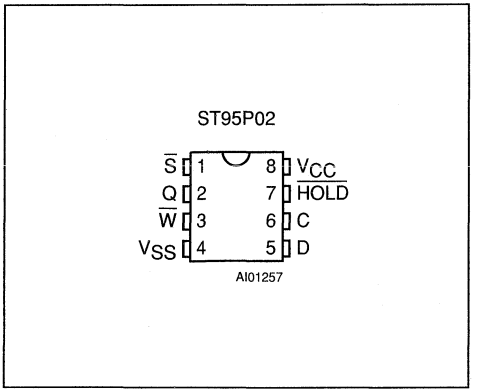


Figure 2B. SO Pin Connections

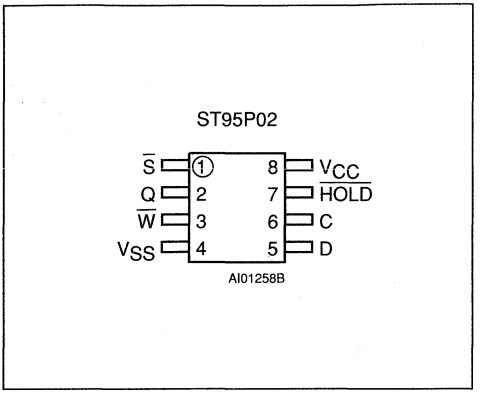


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

SIGNALS DESCRIPTION

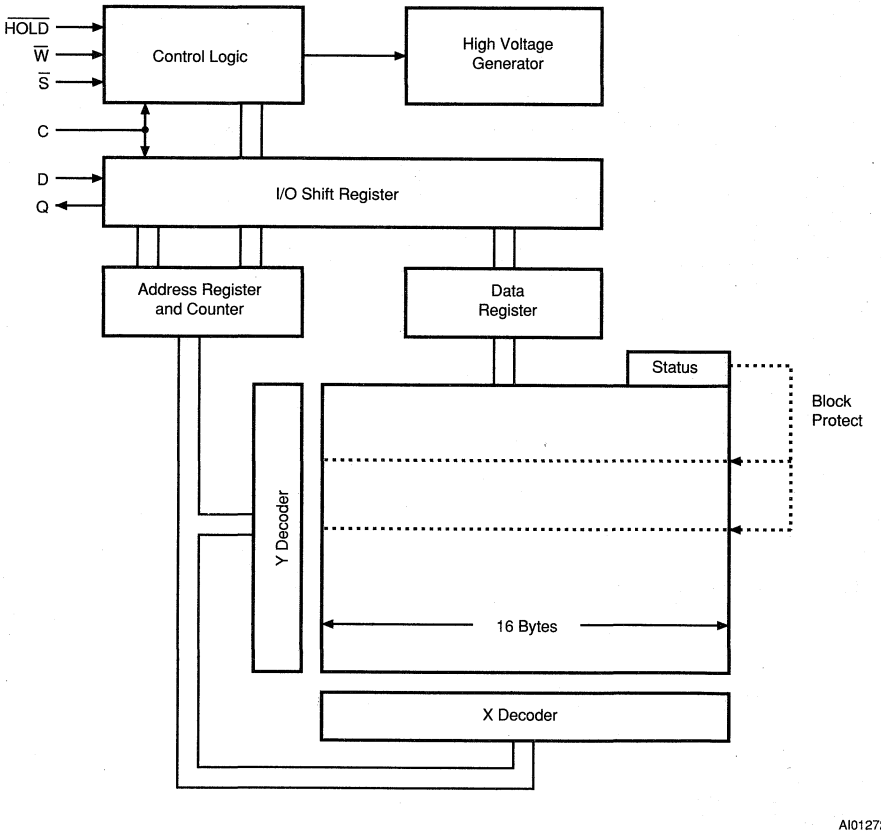
Serial Output (Q). The output pin is used to transfer data serially out of the ST95P02. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). This input is used to select the ST95P02. The chip is selected by a high to low transition on the $\overline{S}$ pin when C is at '0' state. At any time, the chip is deselected by a low to high transition on the $\overline{S}$ pin when C is at '0' state. As soon as the chip is deselected, the Q pin is at high impedance state. This pin allows multiple ST95P02 to share the same SPI bus. After power up, the chip is at the deselect state. Transitions of $\overline{S}$ are ignored when C is at '1' state.

Figure 3. Block Diagram



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Input Output Waveforms

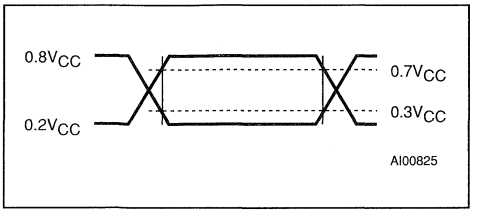


Figure 5. AC Testing Load Circuit

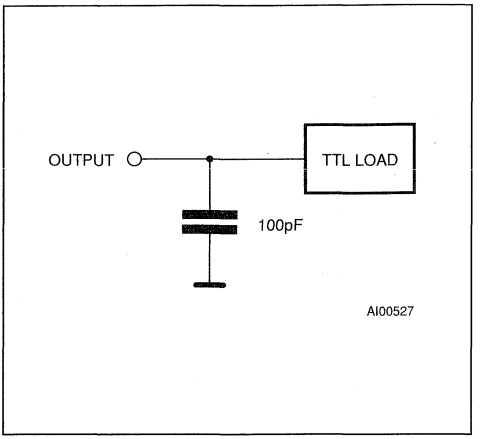


Table 3. Input Parameters (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width		10	ns

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V		50	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 2mA	0.8 V_{CC}		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCH}	t_{SU}	$\overline{S}$ Setup Time		50		ns
t_{CLSH}	t_{SH}	$\overline{S}$ Hold Time		50		ns
t_{CH}	t_{WH}	Clock High Time		200		ns
t_{CL}	t_{WL}	Clock Low Time		300		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HXCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		50		ns
t_{CLHX}	t_{HH}	$\overline{HOLD}$ Hold Time		50		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	4.5V < V_{CC} < 5.5V	200		ns
			3V < V_{CC} < 4.5V	250		ns
t_{SLQZ}	t_{DIS}	Output Disable Time			150	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			150	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			150	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data is available.

Figure 6. Output Timing

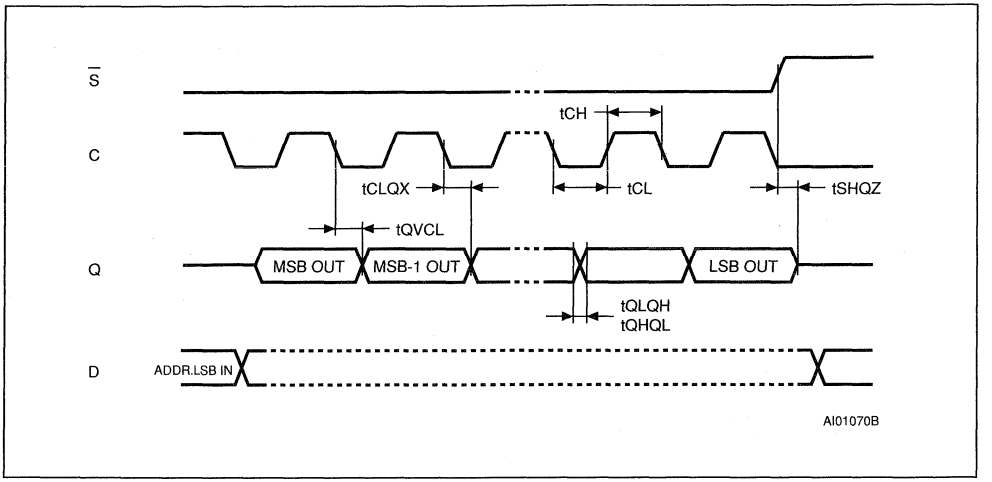


Figure 7. Serial Input Timing

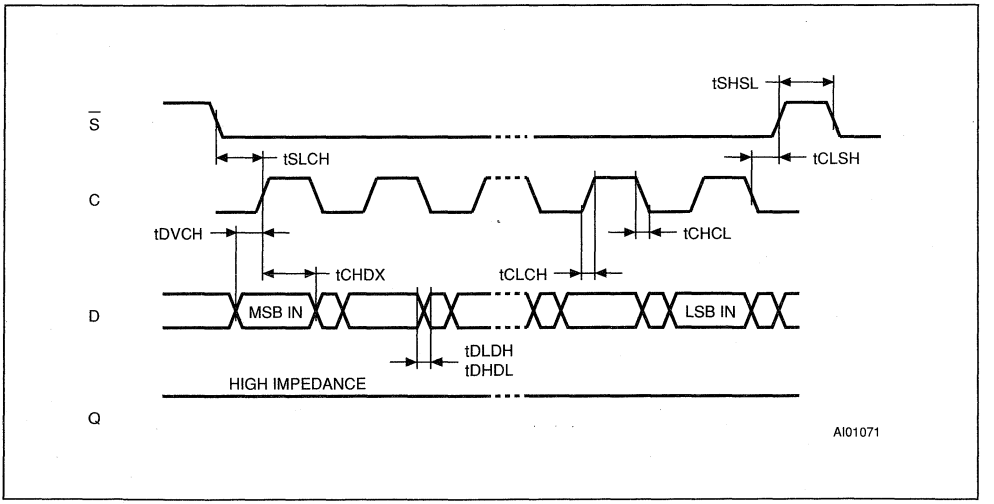
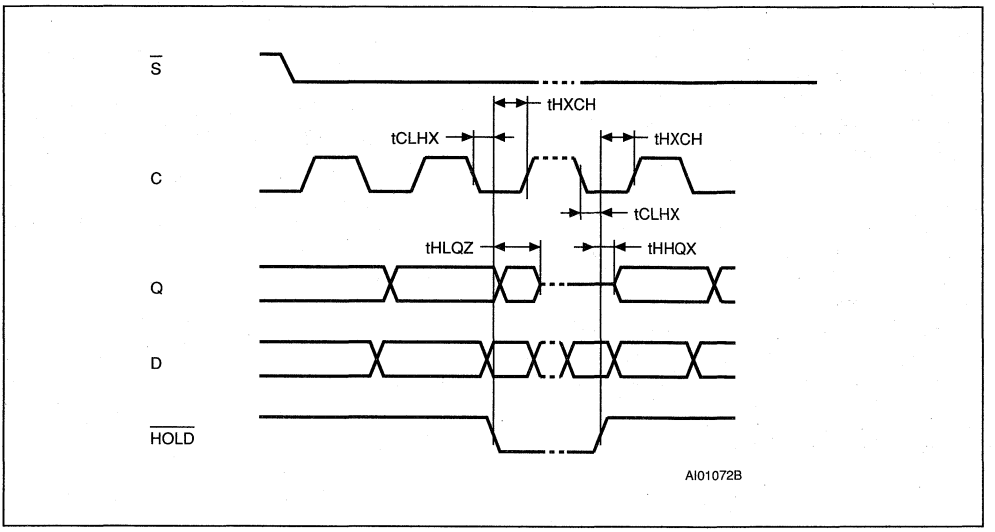


Figure 8. Hold Timing



Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95P02 are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95P02 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95P02 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 7 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 7), the chip is automatically deselected.

Write Enable (WREN) and Write Disable (WRDI)

The ST95P02 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95P02, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95P02 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and Write bits
WEL, WIP: Read only bits.

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95P02 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset.

The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95P02 is divided into four 512 bit blocks. The user may read the blocks but will be unable to write within the selected blocks.

The blocks and respective WRSR control bits are shown in Table 6.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out.

Table 6. Array Addresses Protect

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	none
0	1	C0h - FFh
1	0	80h - FFh
1	1	00h - FFh

Table 7. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

OPERATIONS (cont'd)

When the highest address is reached (FFh), the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95P02 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing a one byte address (A7-A0), and one byte of data. $\overline{S}$ must remain low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur at the clock low pulse just after the eigth bit of data of a word is received.

Figure 9. Read Operation Sequence

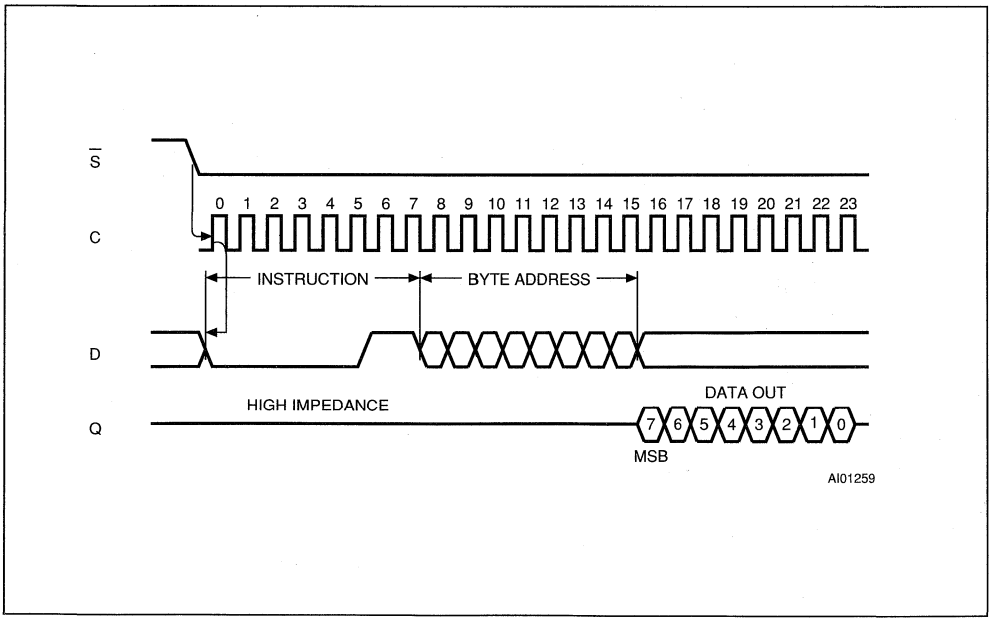


Figure 10. Write Enable Latch Sequence

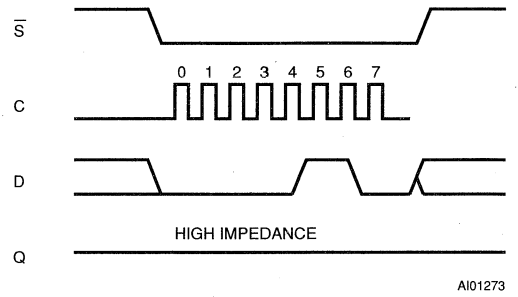


Figure 11. Write Operation Sequence

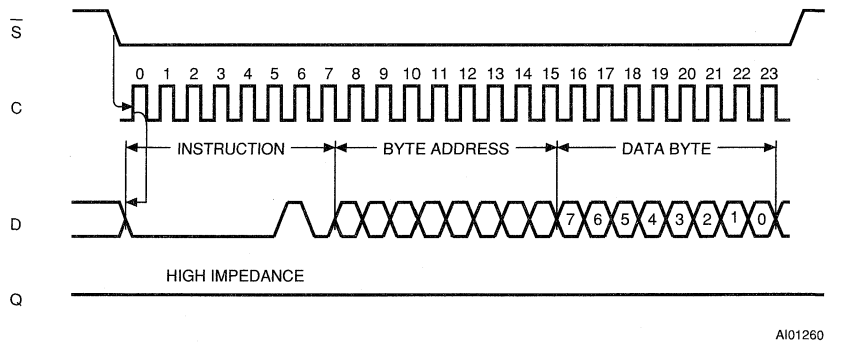


Figure 12. Page Write Operation Sequence

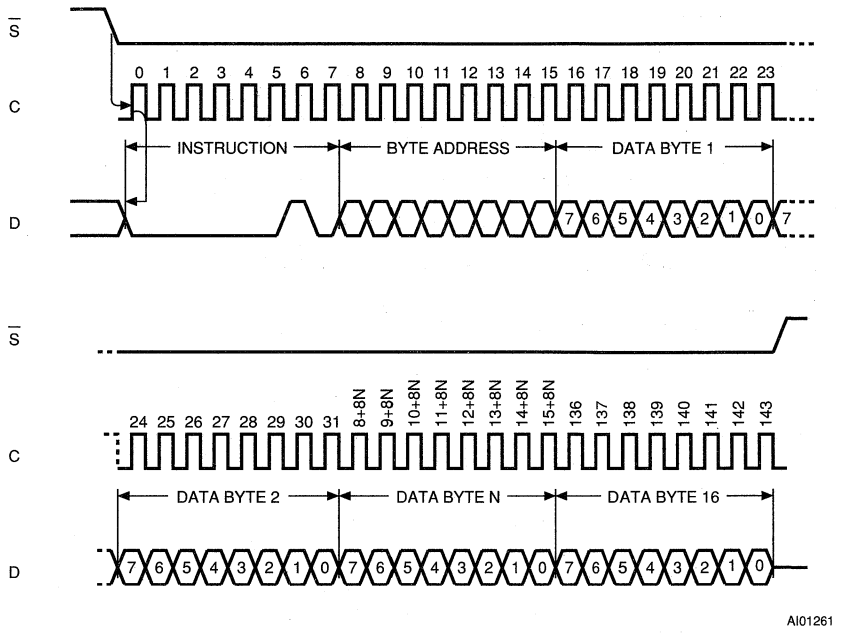


Figure 13. RDSR: Read Status Register Sequence

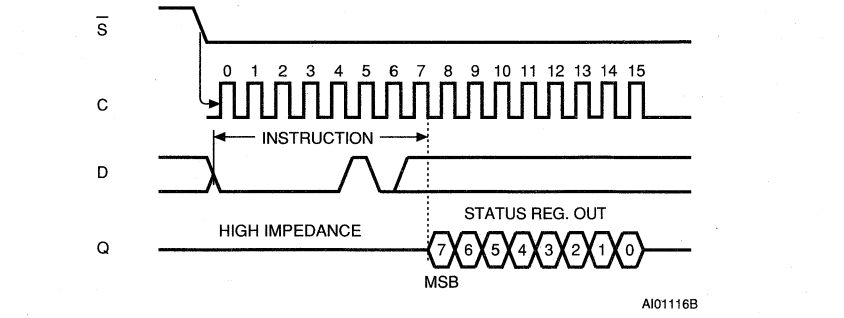
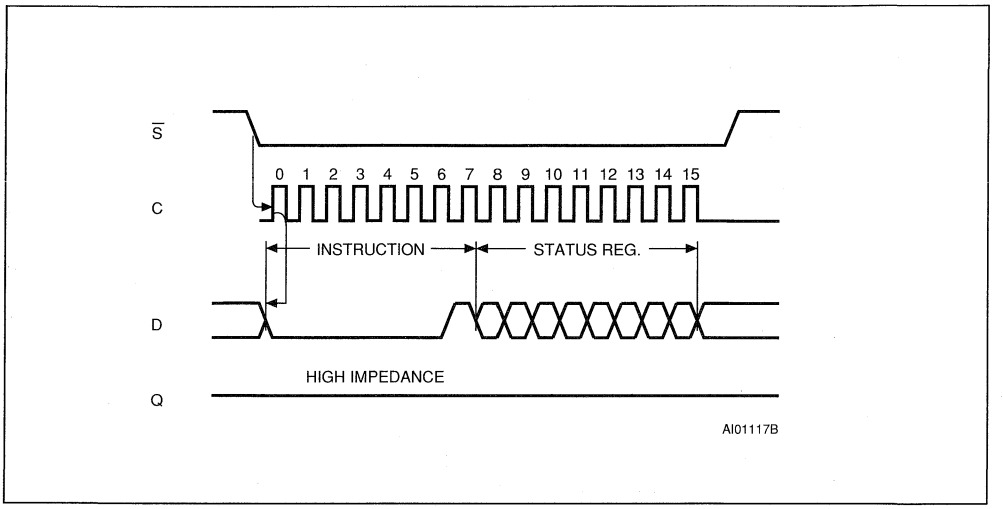


Figure 14. WRSR: Write Status Register Sequence



POWER ON STATE

After a Power up the ST95P02 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

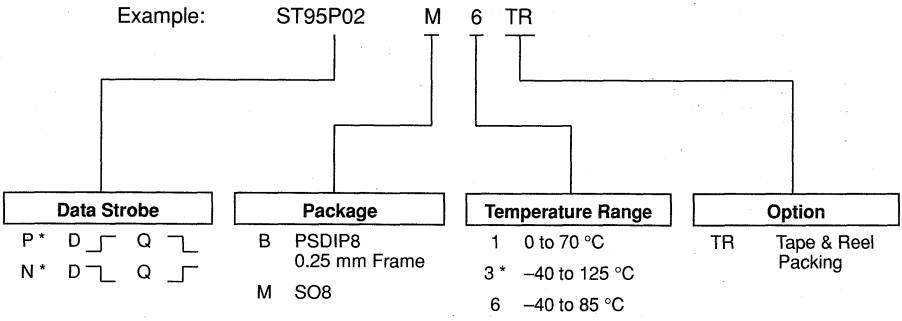
DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register). The Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

ORDERING INFORMATION SCHEME



Notes: P * Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
N * **On Request Only.** Data In strobed on the falling edge of the clock and Data Out synchronized on the rising edge of the clock.
3 * Temperature range on special request only.

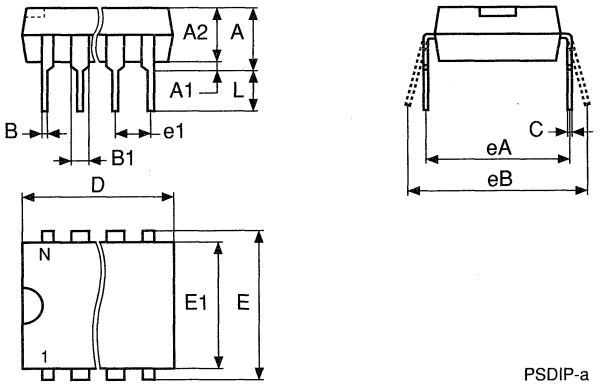
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	
CP			0.10			0.004

PSDIP8



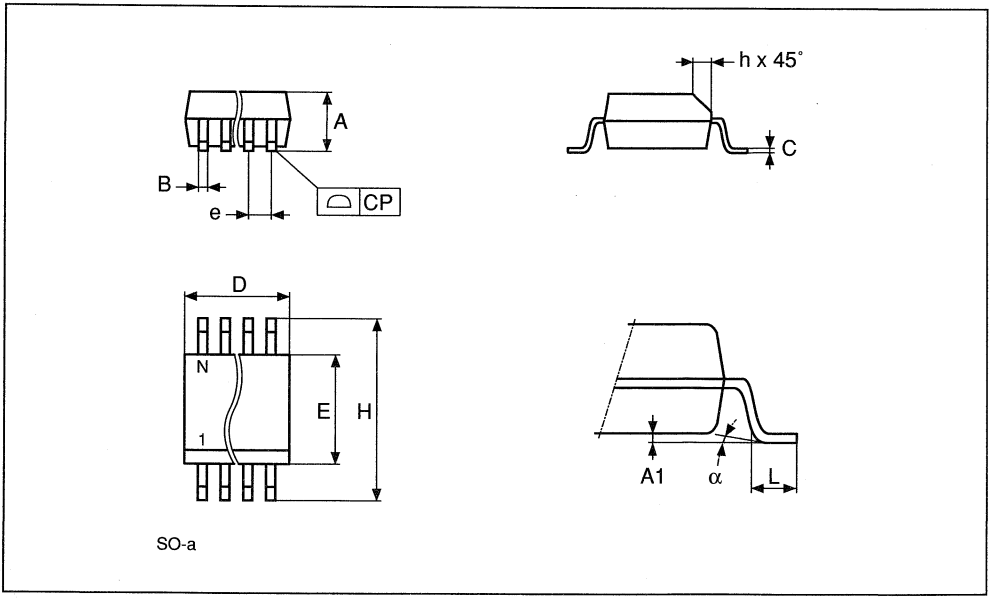
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



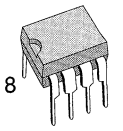
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 4K (512 x 8) EEPROM

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 1 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- ***The ST95P04 will be replaced shortly by the updated version ST95040***



PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

The ST95P04 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 4K bit memory is organised as 32 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

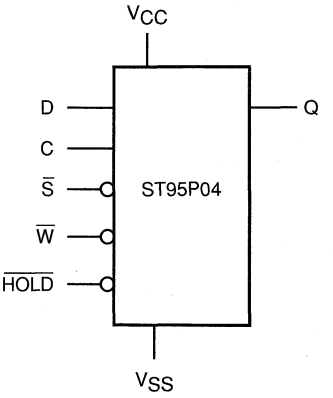


Figure 2A. DIP Pin Connections

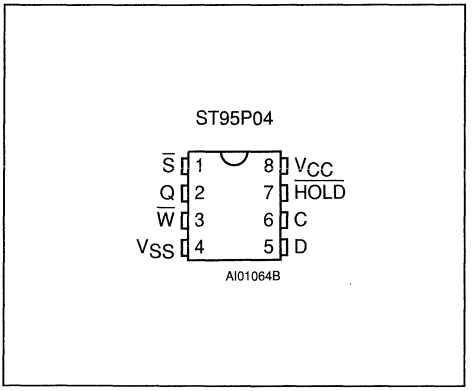


Figure 2B. SO Pin Connections

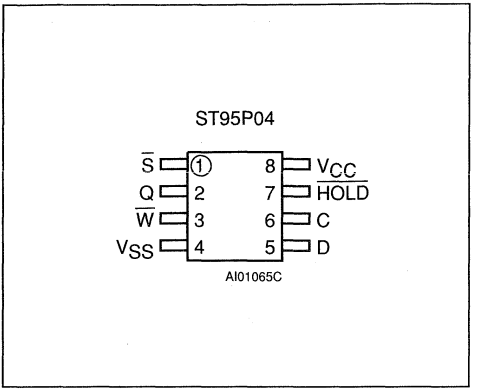


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

SIGNALS DESCRIPTION

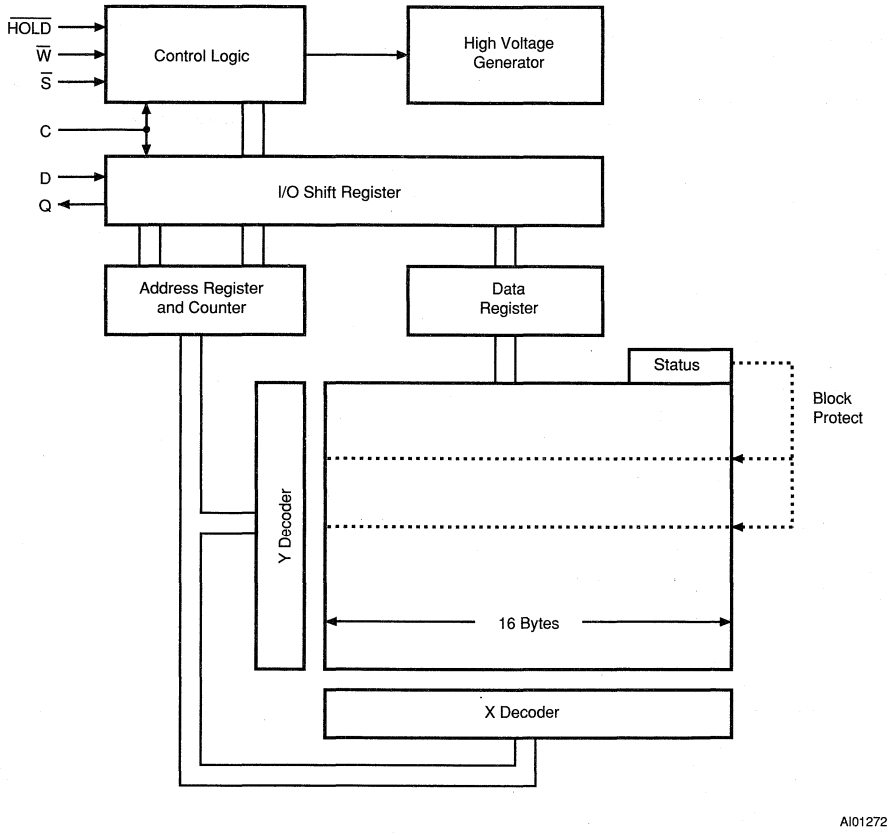
Serial Output (Q). The output pin is used to transfer data serially out of the ST95P04. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). This input is used to select the ST95P04. The chip is selected by a high to low transition on the $\overline{S}$ pin when C is at '0' state. At any time, the chip is deselected by a low to high transition on the $\overline{S}$ pin when C is at '0' state. As soon as the chip is deselected, the Q pin is at high impedance state. This pin allows multiple ST95P04 to share the same SPI bus. After power up, the chip is at the deselect state. Transitions of $\overline{S}$ are ignored when C is at '1' state.

Figure 3. Block Diagram



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Input Output Waveforms

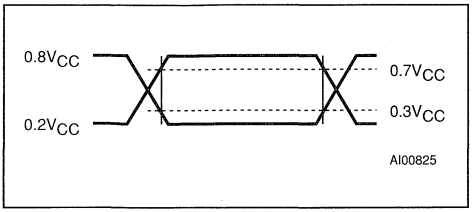


Figure 5. AC Testing Load Circuit

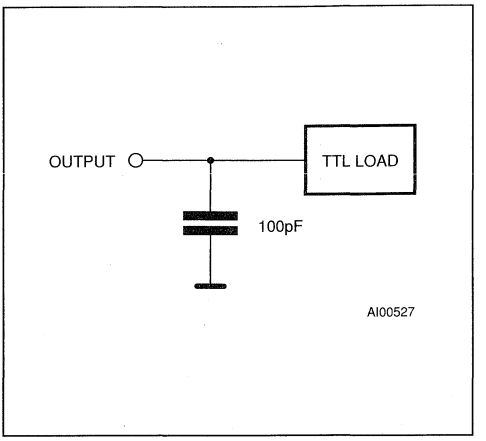


Table 3. Input Parameters (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width		10	ns

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 1 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V		50	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 2mA	0.8 V_{CC}		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	1	MHz
t_{SLCH}	t_{SU}	$\overline{S}$ Setup Time		100		ns
t_{CLSH}	t_{SH}	$\overline{S}$ Hold Time		100		ns
t_{CH}	t_{WH}	Clock High Time		400		ns
t_{CL}	t_{WL}	Clock Low Time		400		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		100		ns
t_{CHDX}	t_{DH}	Data In Hold Time		100		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HXCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{CLHX}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time		400		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			300	ns
t_{QVCL}	t_V	Output Valid from Clock Low			400	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			150	ns
t_{QHQL}	t_{FO}	Output Fall Time			150	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			300	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			300	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data is available.

Figure 6. Output Timing

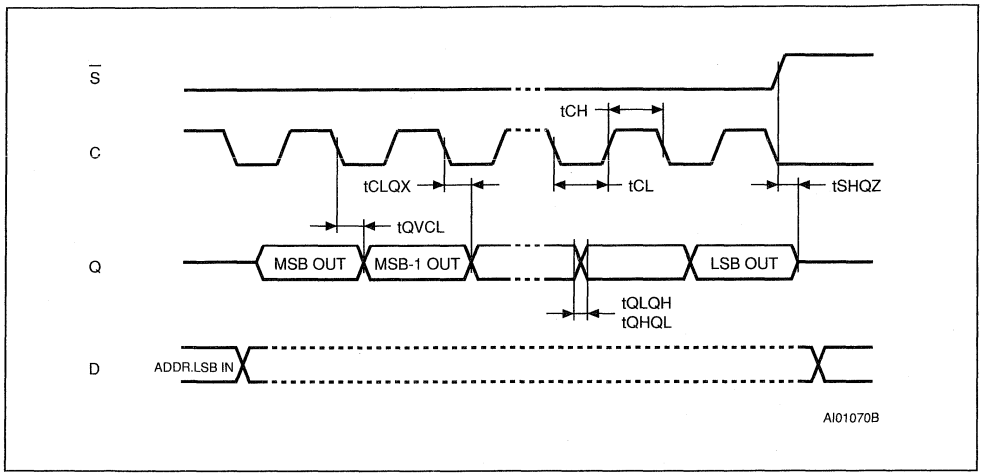


Figure 7. Serial Input Timing

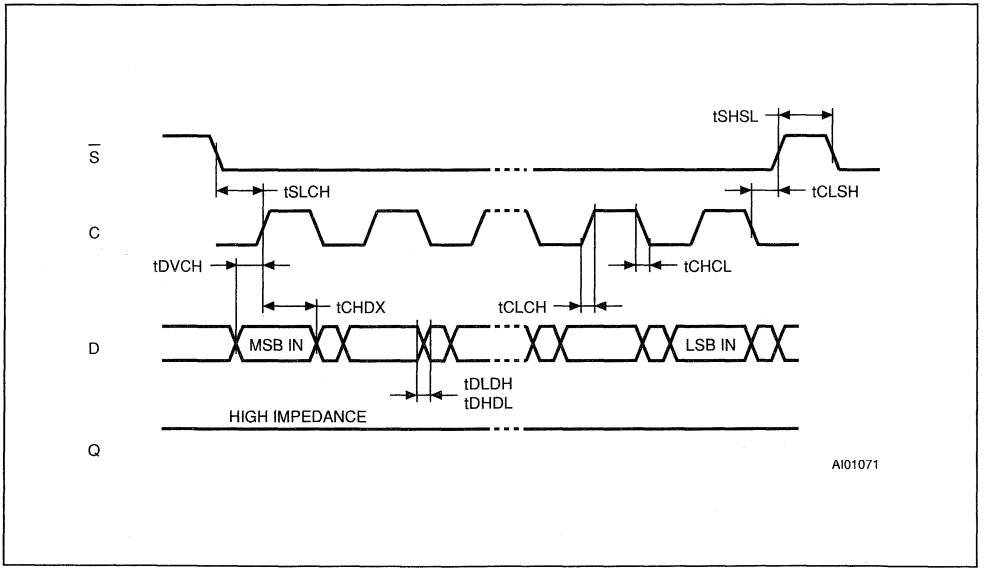
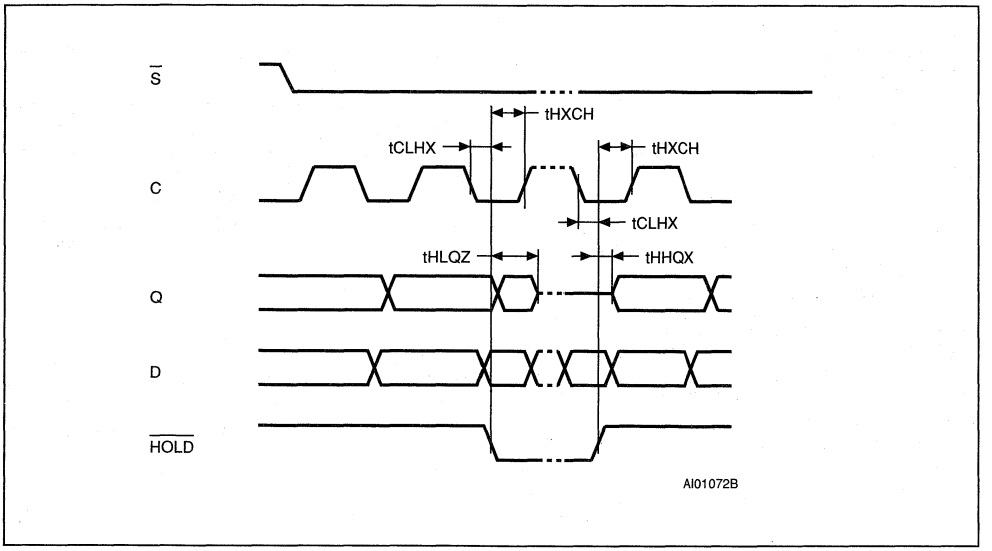


Figure 8. Hold Timing



Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95P04 are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95P04 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95P04 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 7 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 7), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95P04 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95P04, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95P04 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and Write bits
WEL, WIP: Read only bits.

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95P04 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset.

The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95P04 is divided into four 1024 bit blocks. The user may read the blocks but will be unable to write within the selected blocks.

The blocks and respective WRSR control bits are shown in Table 6.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 3 of the read instruction contains address A8 (most significant address bit). This bit is used to select the first or second page of the device. Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock

Table 6. Array Addresses Protect

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	none
0	1	180h - 1FFh
1	0	100h - 1FFh
1	1	000h - 1FFh

Table 7. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 X110
WRDI	Reset Write Enable Latch	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read Data from Memory Array	0000 A011
WRITE	Write Data to Memory Array	0000 A010

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFh), the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95P04 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing a one byte address (A7-A0), and one byte of data. Bit 3 of the write instruction contains address A8 (most significant address bit). $\overline{S}$ must remain low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur at the clock low pulse just after the eigth bit of data of a word is received.

Figure 9. Read Operation Sequence

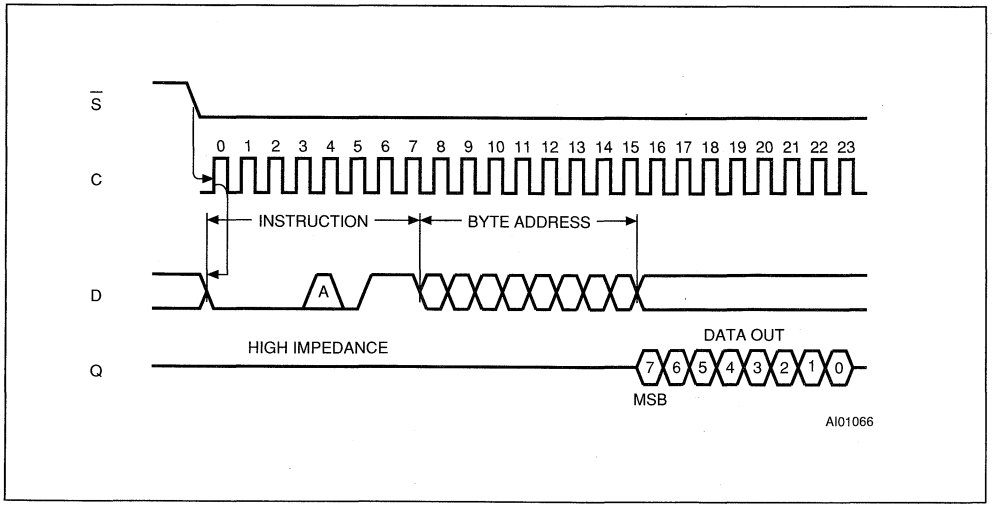


Figure 10. Write Enable Latch Sequence

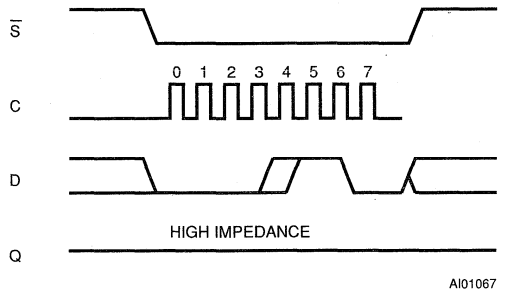


Figure 11. Write Operation Sequence

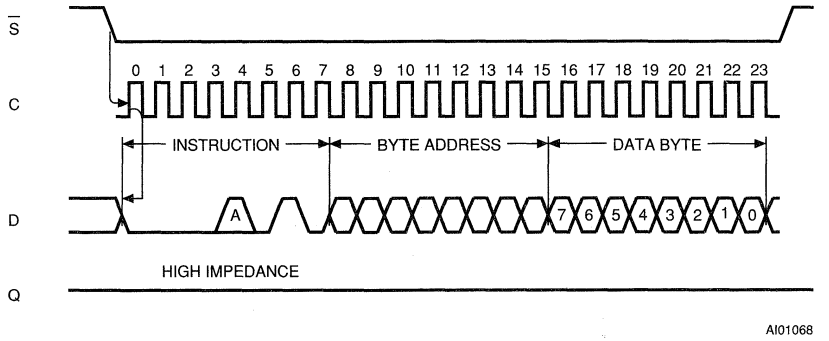


Figure 12. Page Write Operation Sequence

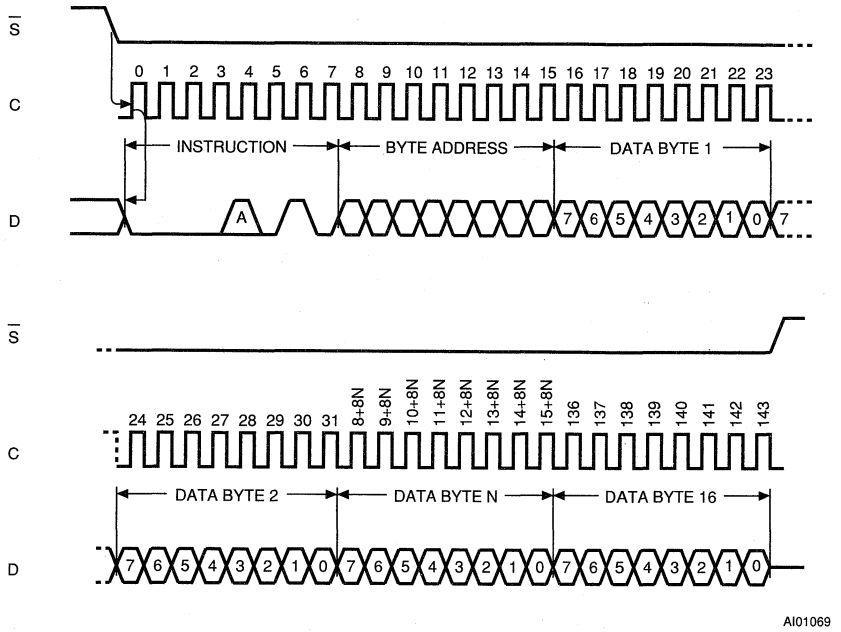


Figure 13. RDSR: Read Status Register Sequence

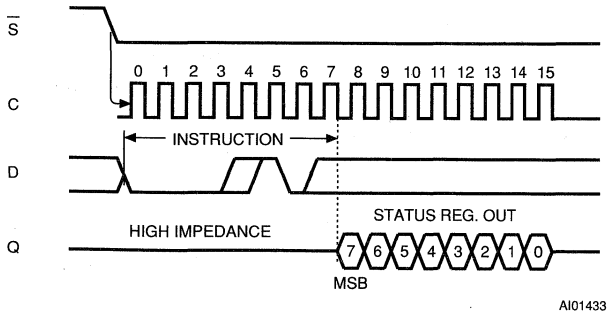
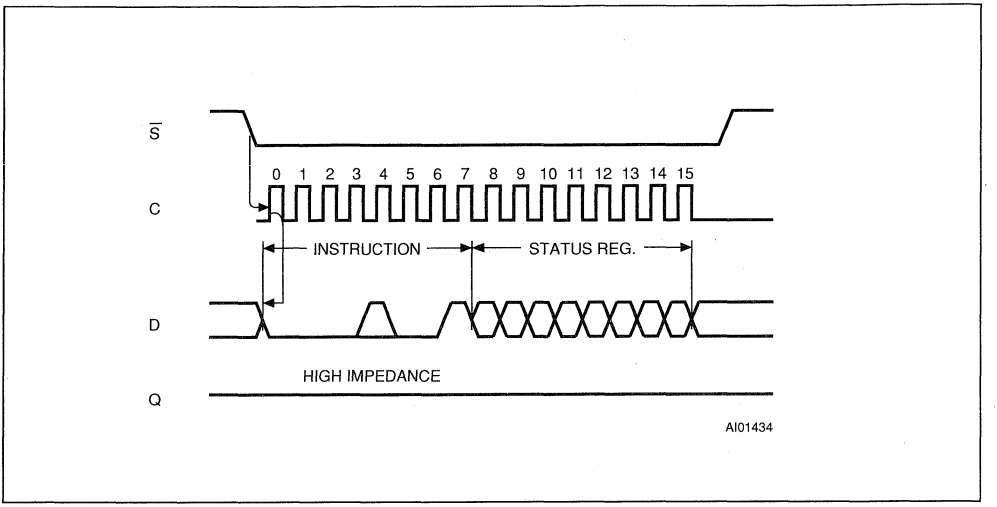


Figure 14. WRSR: Write Status Register Sequence



POWER ON STATE

After a Power up the ST95P04 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

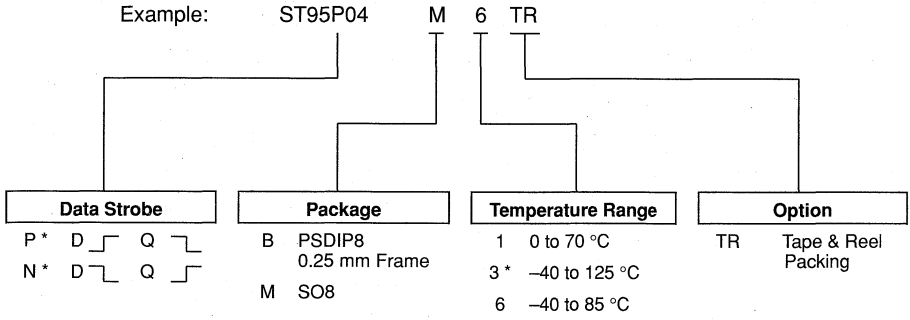
DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register). The Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

ORDERING INFORMATION SCHEME



Notes: P * Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
N * **On Request Only.** Data In strobed on the falling edge of the clock and Data Out synchronized on the rising edge of the clock.
3 * Temperature range on special request only.

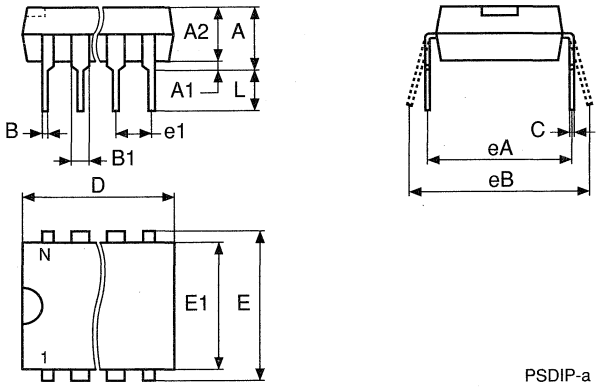
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	
CP			0.10			0.004

PSDIP8



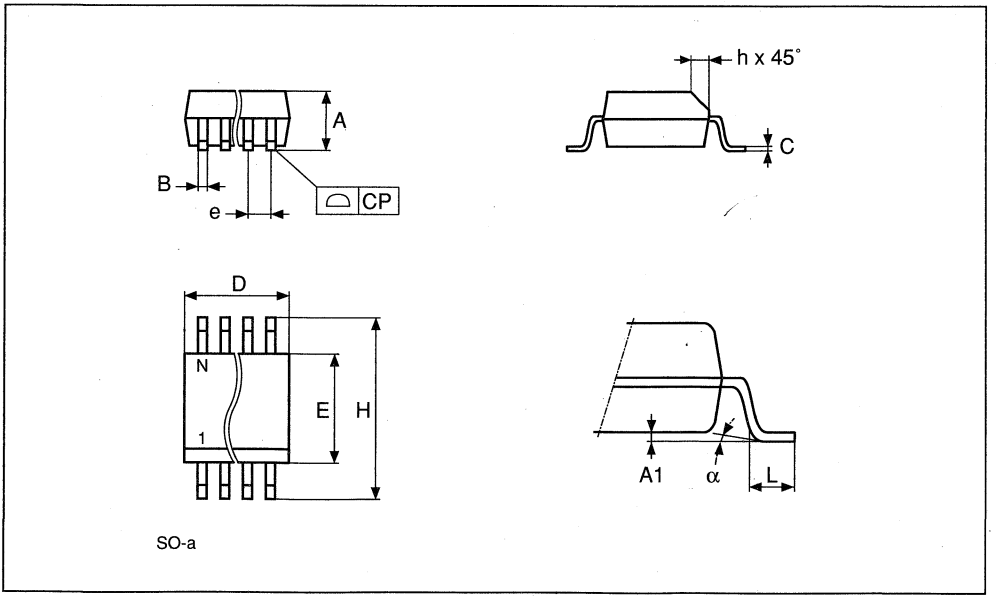
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



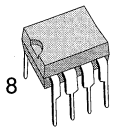
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 8K (1K x 8) EEPROM

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- ***The ST95P08 will be replaced shortly by the updated version ST95080***



PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

The ST95P08 is a 8K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 8K bit memory is organised as 64 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

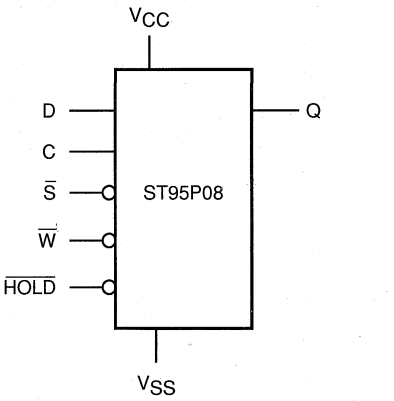


Figure 2A. DIP Pin Connections

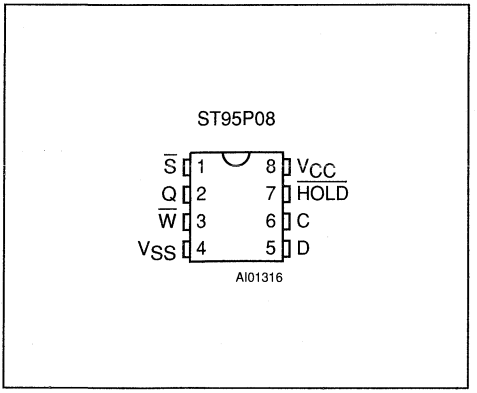


Figure 2B. SO Pin Connections

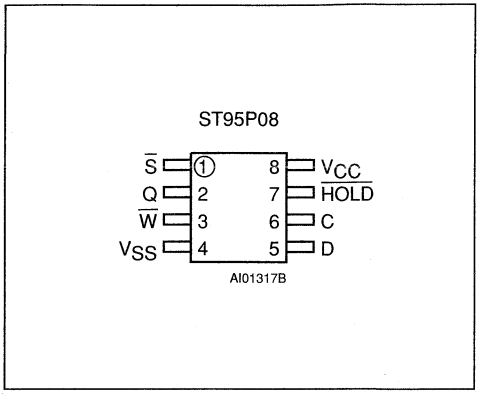


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

SIGNALS DESCRIPTION

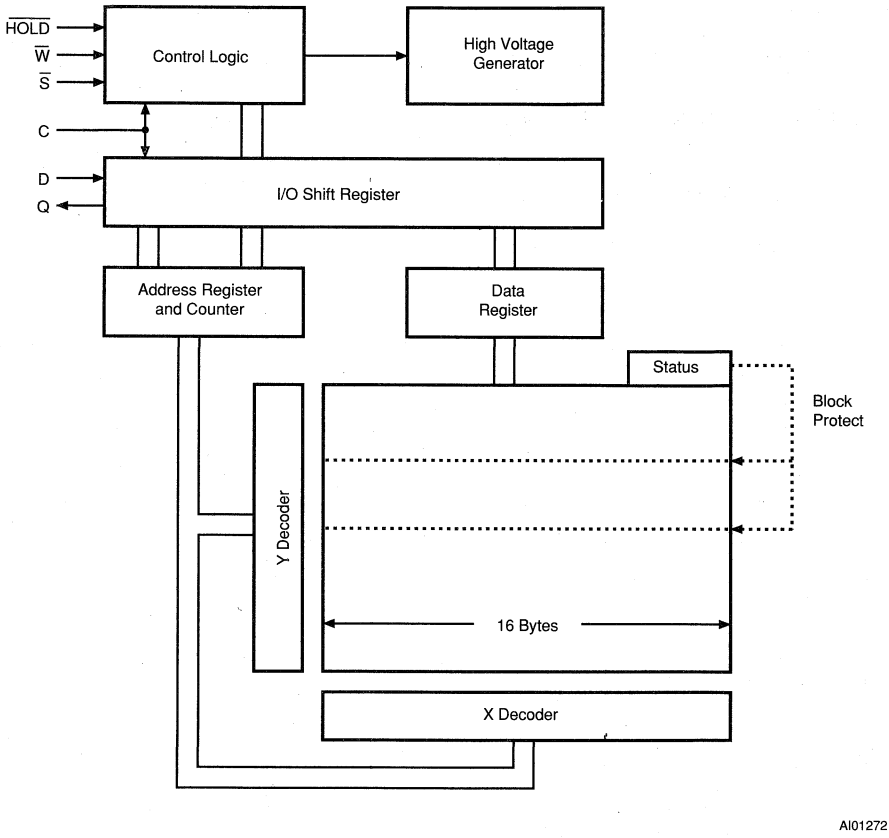
Serial Output (Q). The output pin is used to transfer data serially out of the ST95P08. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). This input is used to select the ST95P08. The chip is selected by a high to low transition on the $\overline{S}$ pin when C is at '0' state. At any time, the chip is deselected by a low to high transition on the $\overline{S}$ pin when C is at '0' state. As soon as the chip is deselected, the Q pin is at high impedance state. This pin allows multiple ST95P08 to share the same SPI bus. After power up, the chip is at the deselect state. Transition of $\overline{S}$ are ignored when C is at '1' state.

Figure 3. Block Diagram



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Input Output Waveforms

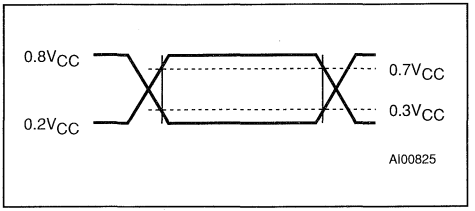


Figure 5. AC Testing Load Circuit

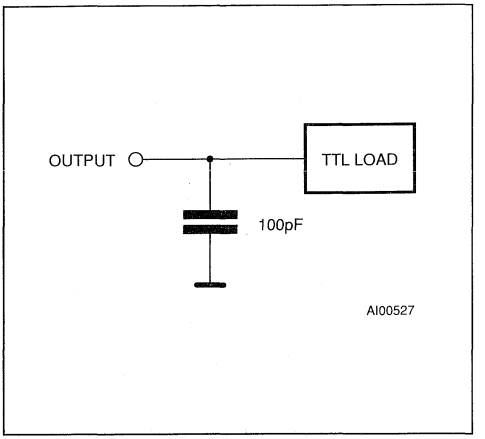


Table 3. Input Parameters (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width		10	ns

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V		50	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 2mA	0.8 V_{CC}		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCH}	t_{SU}	$\overline{S}$ Setup Time		50		ns
t_{CLSH}	t_{SH}	$\overline{S}$ Hold Time		50		ns
t_{CH}	t_{WH}	Clock High Time		200		ns
t_{CL}	t_{WL}	Clock Low Time		300		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HXCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		50		ns
t_{CLHX}	t_{HH}	$\overline{HOLD}$ Hold Time		50		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	4.5V < V_{CC} < 5.5V	200		ns
			3V < V_{CC} < 4.5V	250		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			150	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			150	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			150	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data is available.

Figure 6. Output Timing

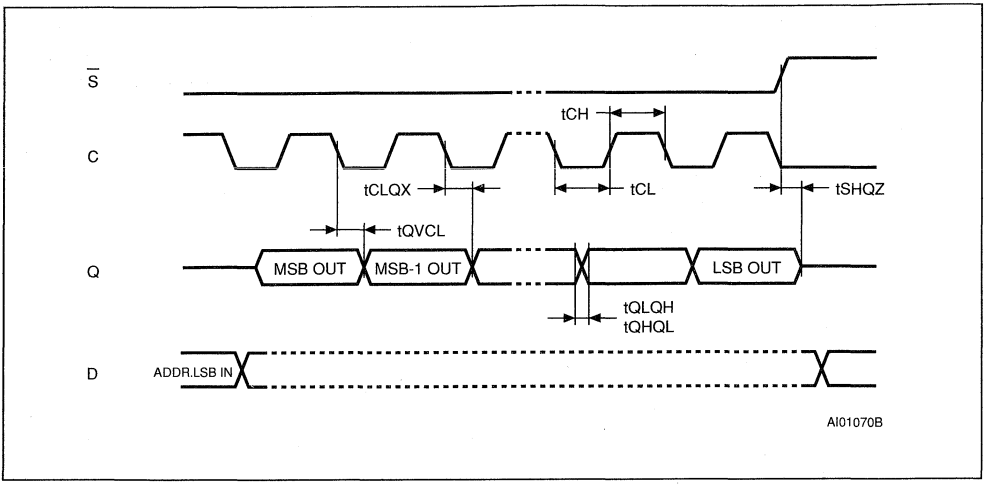


Figure 7. Serial Input Timing

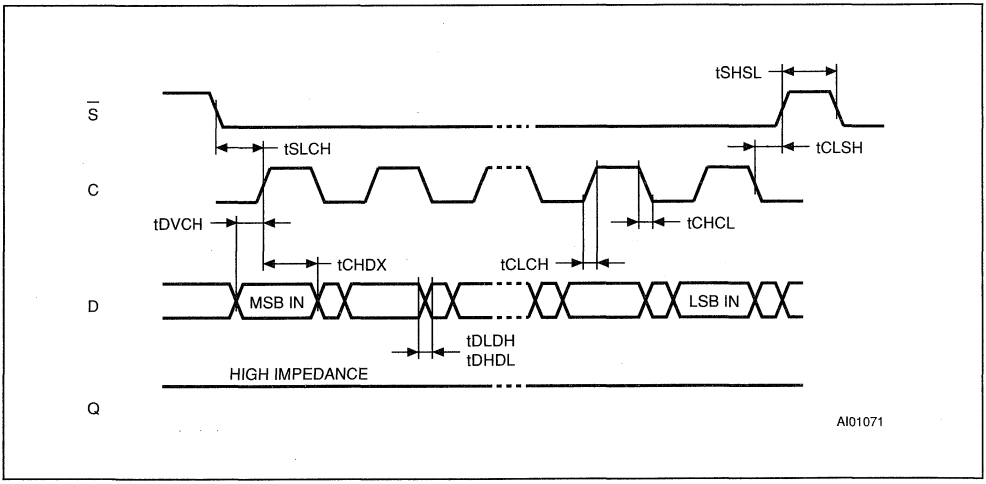
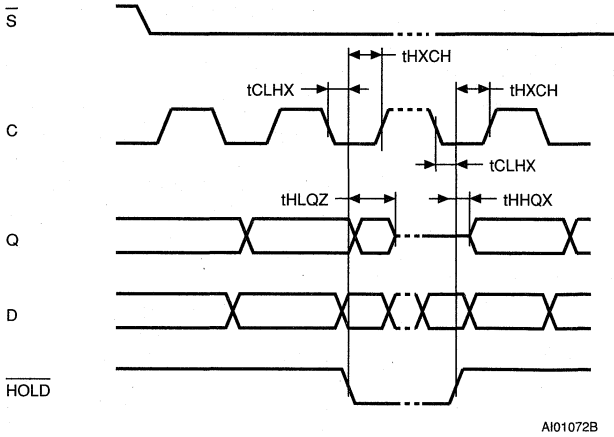


Figure 8. Hold Timing



Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95P08 are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95P08 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95P08 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 7 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 7), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95P04 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95P08, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95P08 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95P08 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset.

The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95P08 is divided into four 2048 bit blocks. The user may read the blocks but will be unable to write within the selected blocks.

The blocks and respective WRSR control bits are shown in Table 6.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 3 and 4 of the read instruction contain address bits A9 and A8 (most significant address bits). These bits are used to select the first or second page of the device. Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next

Table 6. Array Addresses Protect

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	none
0	1	300h - 3FFh
1	0	200h - 3FFh
1	1	000h - 3FFh

Table 7. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	000X X110
WRDI	Reset Write Enable Latch	000X X100
RDSR	Read Status Register	000X X101
WRSR	Write Status Register	000X X001
READ	Read Data from Memory Array	000A A011
WRITE	Write Data to Memory Array	000A A010

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

OPERATIONS (cont'd)

address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFh), the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95P08 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing a one byte address (A7-A0), and one byte of data. Bits 3 and 4 of the write instruction contain address bits A9 and A8 (most significant address bits). $\overline{S}$ must remain low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur at the clock low pulse just after the eigth bit of data of a word is received.

Figure 9. Read Operation Sequence

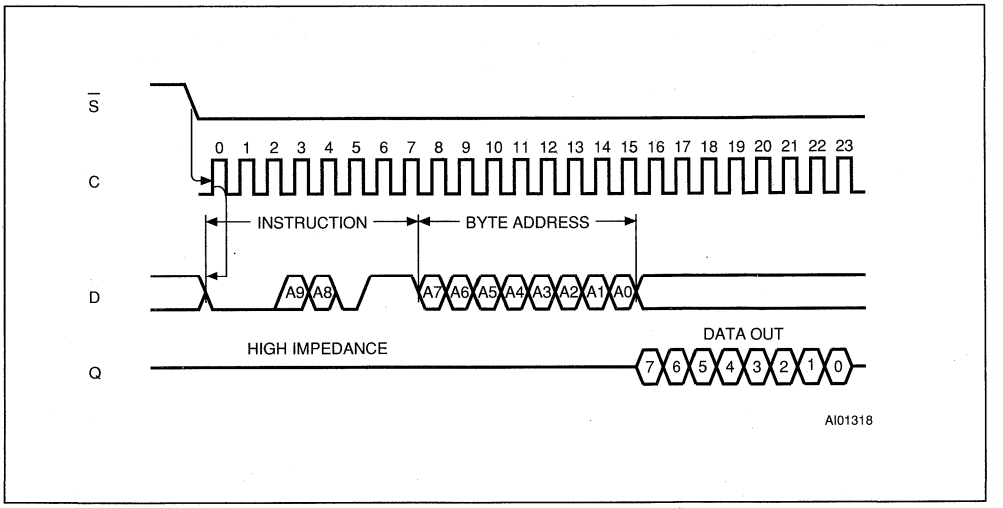


Figure 10. Write Enable Latch Sequence

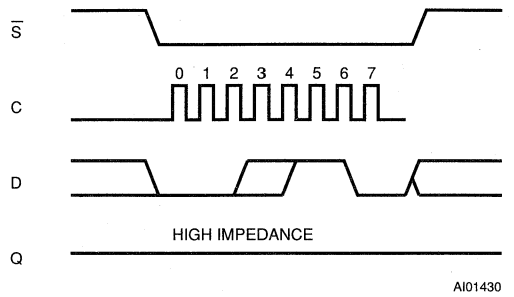


Figure 11. Write Operation Sequence

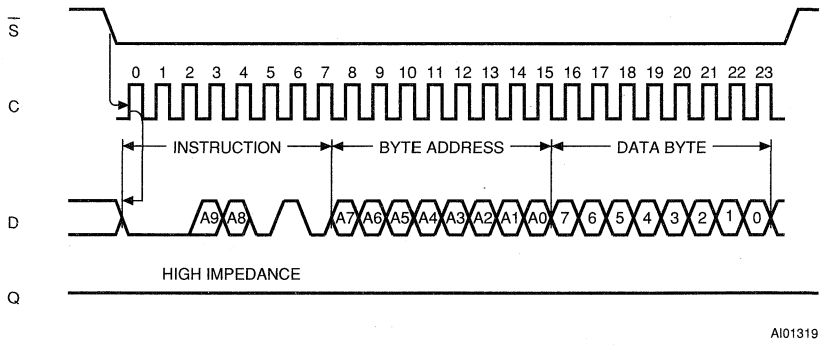


Figure 12. Page Write Operation Sequence

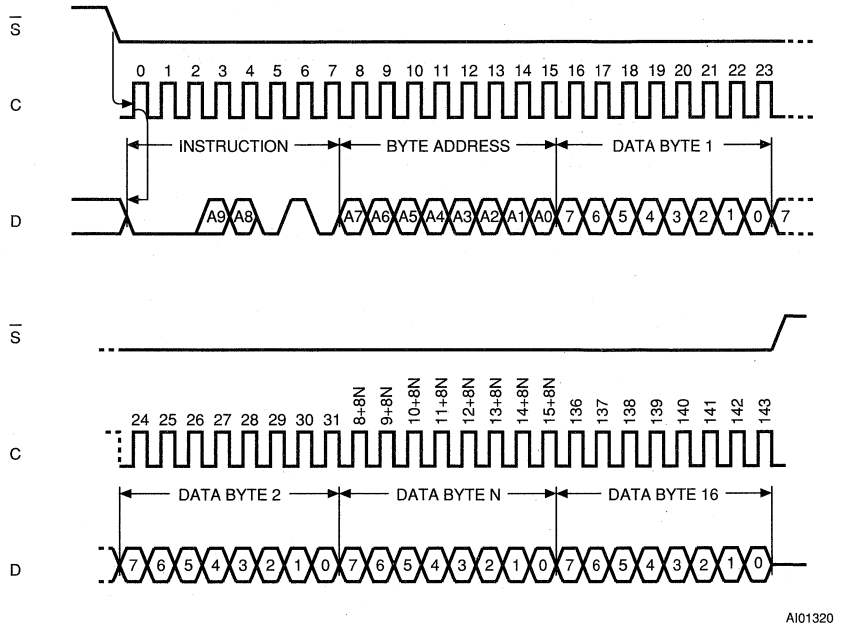


Figure 13. RDSR: Read Status Register Sequence

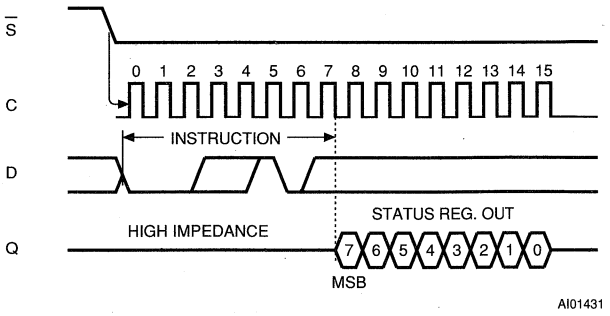
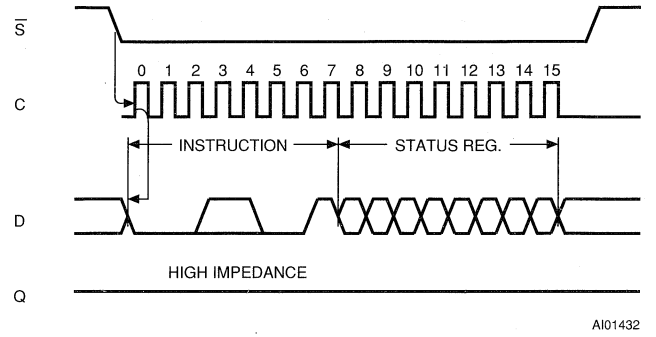


Figure 14. WRSR: Write Status Register Sequence



POWER ON STATE

After a Power up the ST95P08 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

DATA PROTECTION AND PROTOCOL SAFETY

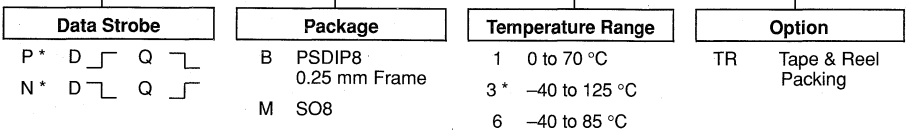
- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register). The Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

ORDERING INFORMATION SCHEME

Example: ST95P08 M 6 TR



Notes: P * Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
N * **On Request Only.** Data In strobed on the falling edge of the clock and Data Out synchronized on the rising edge of the clock.
3 * Temperature range on special request only.

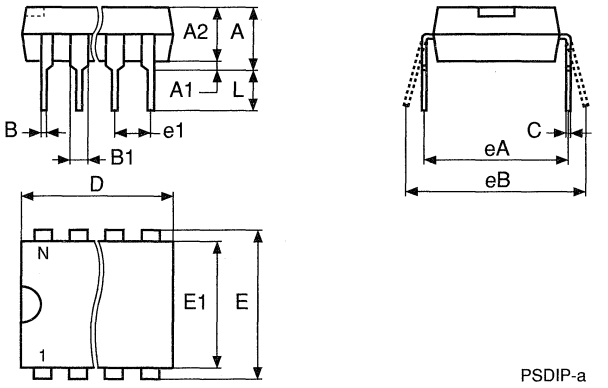
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	
CP			0.10			0.004

PSDIP8



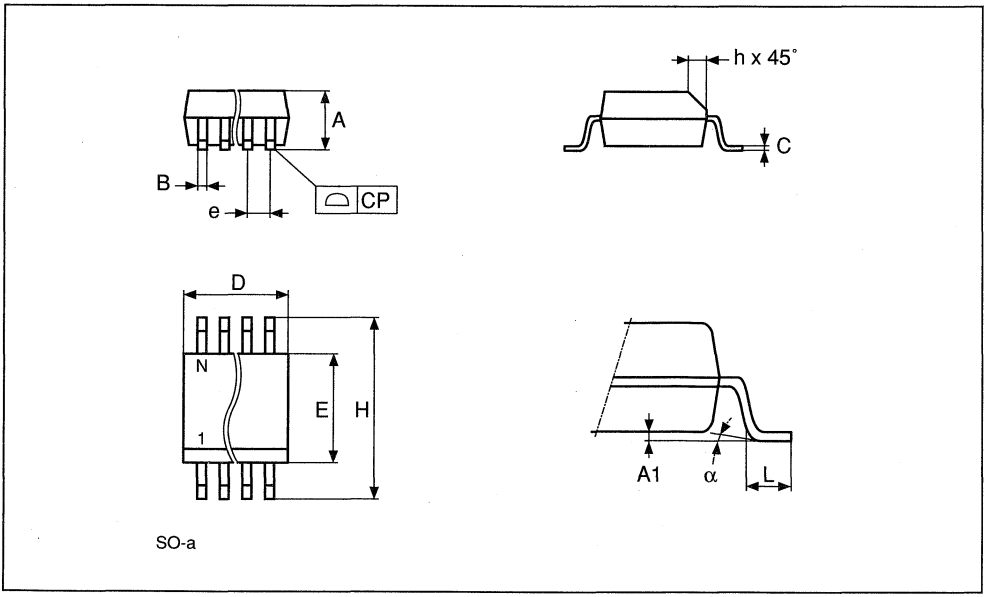
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



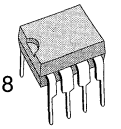
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 2K (256 x 8) EEPROM

PRODUCT PREVIEW

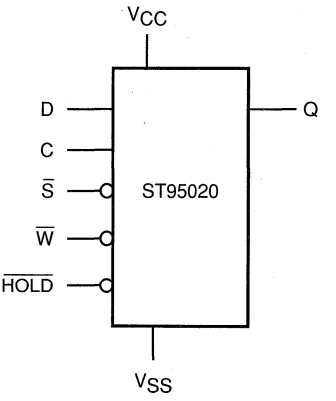
- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST95020 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

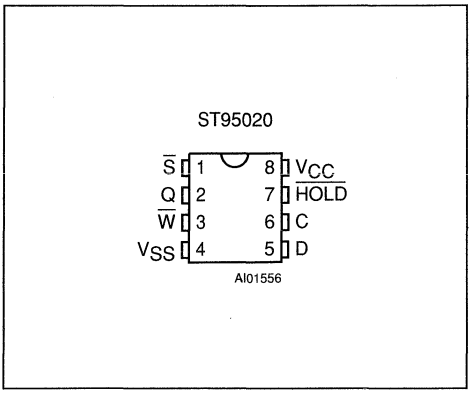


Figure 2B. SO Pin Connections

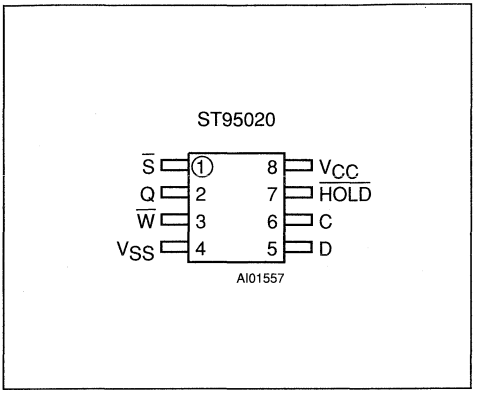


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data are clocked in during the low to high transition of clock C, data are clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Figure 3. Data and Clock Timing

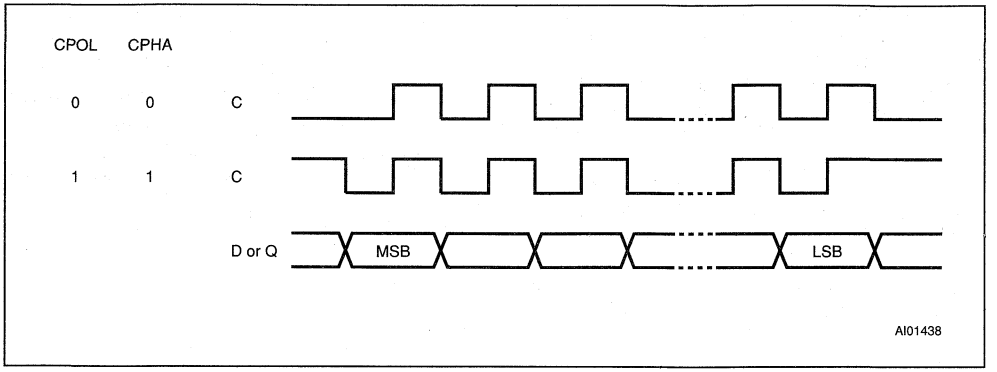
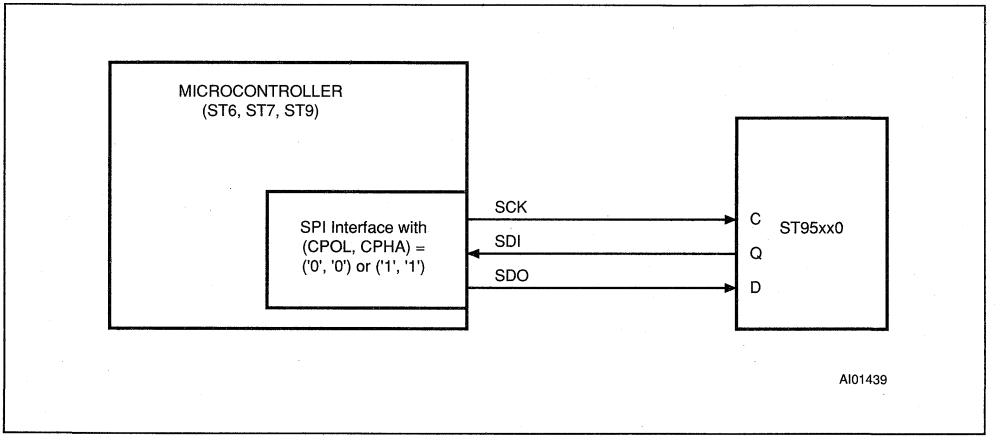


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the ST95020 is deselected and the D output pin is at high impedance and unless an internal write operation is underway the S95020 will be in the standby power mode. $\overline{S}$ low enables the ST95020, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95020 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The ST95020 can be driven by a microcontroller with its SPI peripheral running in either two of the following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data are latched in by the low to high transition of clock C, and output data are available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains to '0' for (CPOL, CPHA) = (0, 0) and C remains to 1 for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95020 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95020, the circuit executes the instruction and enters a wait mode until it is deselected.

Table 3. Write Protected Block Size

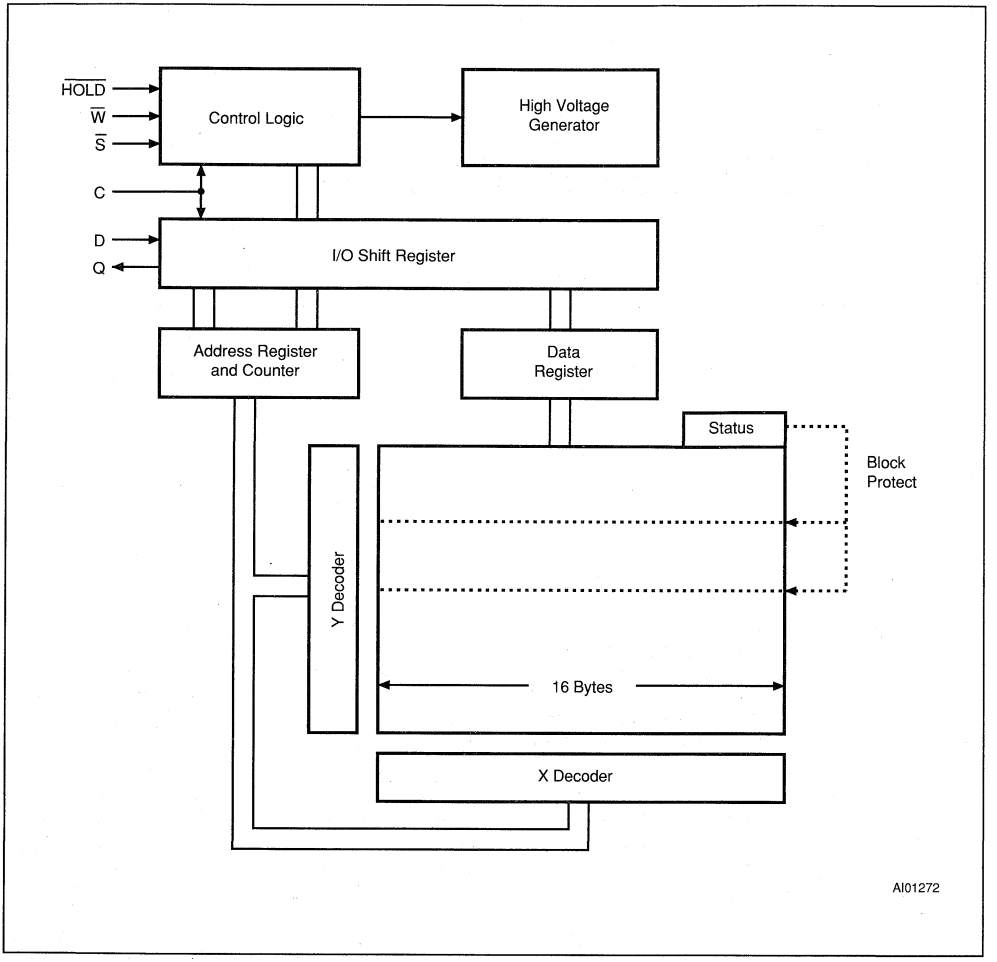
Status Register Bits		Array Addresses Protected	Protected Block
BP1	BP0		
0	0	none	none
0	1	C0h - FFh	Upper quart
1	0	80h - FFh	Upper half
1	1	00h - FFh	Whole memory

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Notes: A = 1, Upper page selected
A = 0, Lower page selected

Figure 5. Block Diagram



Read Status Register (RDSR)

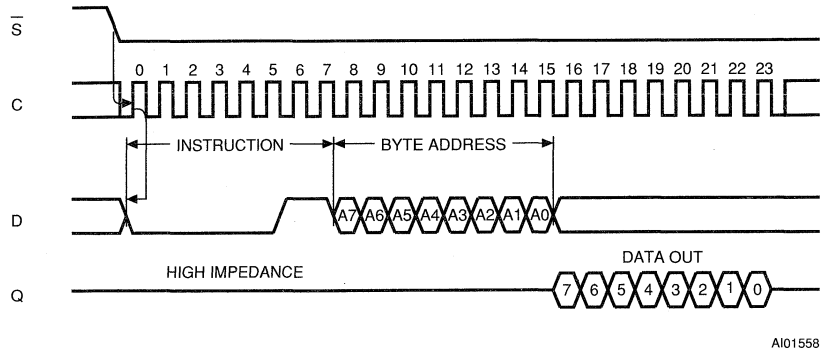
The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95020 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

Figure 6. Read Operation Sequence



OPERATIONS (cont'd)

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95020 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95020 is divided into four 512 bit blocks. The user may read the blocks but will be unable to write within the selected blocks. The blocks and respective WRSR control bits are shown in Table 3.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 4 of the read instruction contain address bit A8 (most significant address bit). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

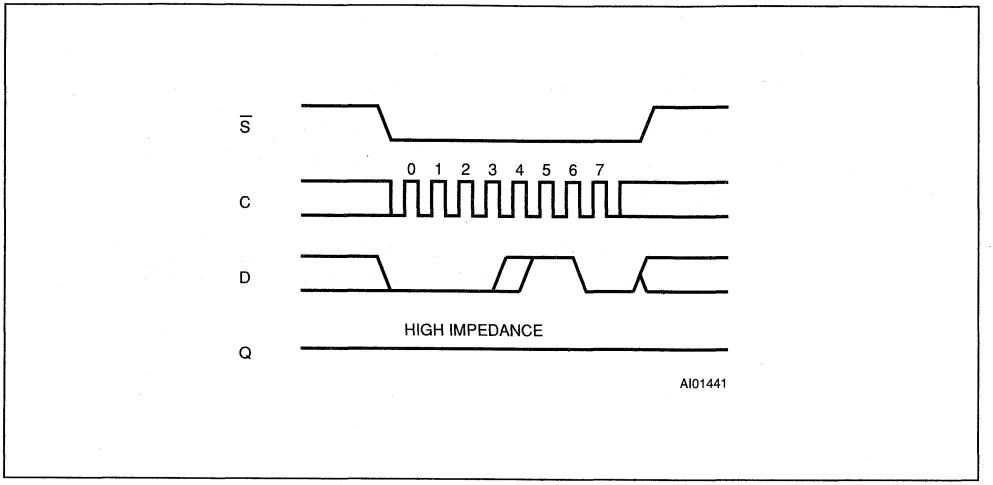


Figure 8. Write Operation Sequence

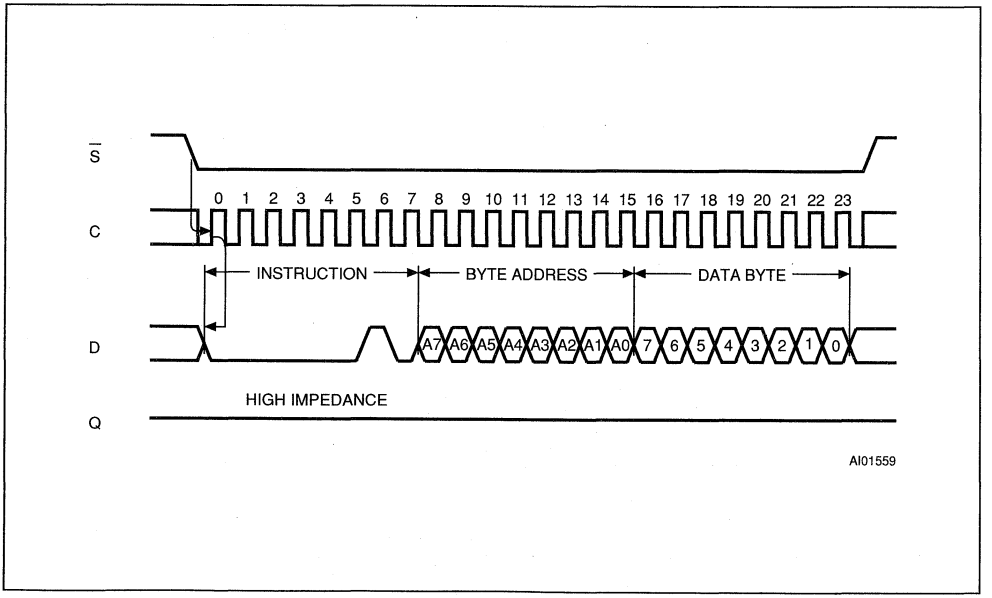


Figure 9. Page Write Operation Sequence

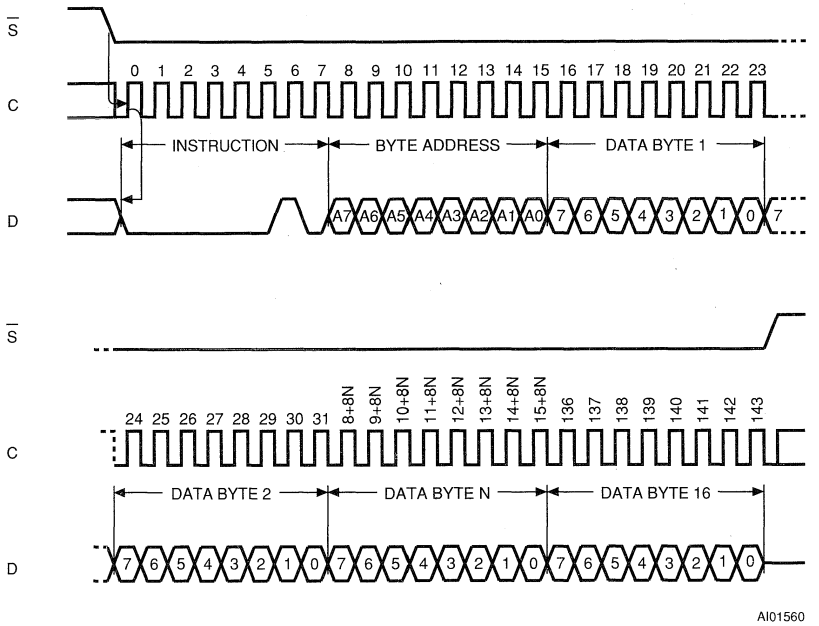


Figure 10. RDSR: Read Status Register Sequence

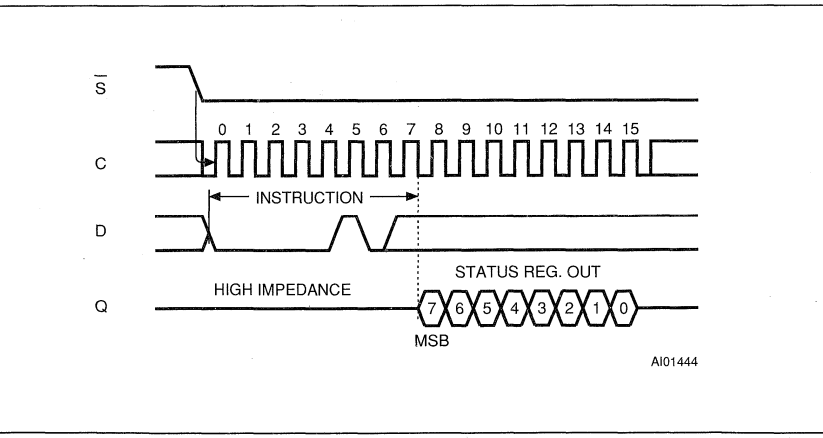
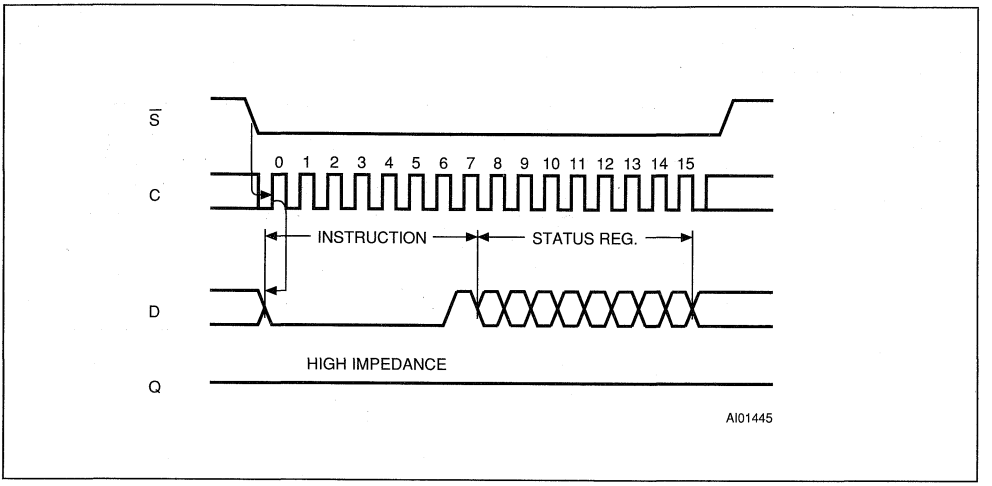


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95020 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remains low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

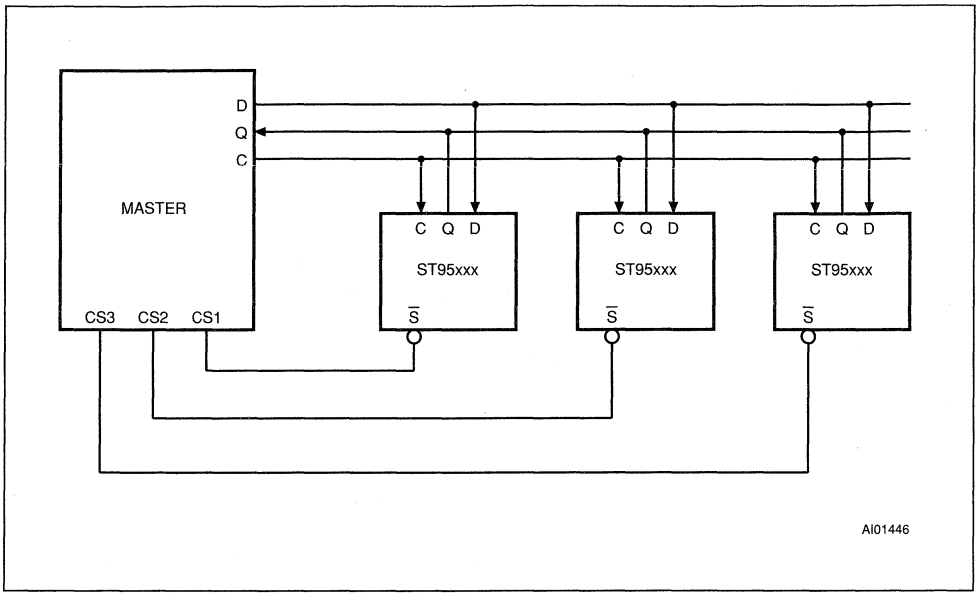
A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur just after the eigth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95020 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

Figure 12. EEPROM and SPI Bus



DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register), i.e. the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Waveforms

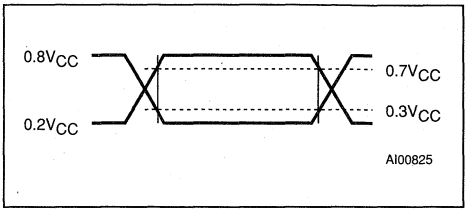


Table 5. Input Parameters (1) (T_A = 25 °C, f = 2 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = 2mA	V_{CC} –0.6		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.

Table 7. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time		100		ns
t_{CHSL}		$\overline{S}$ Active after Rising Edge of C		100		ns
t_{CH}	t_{WH}	Clock High Time		200		ns
t_{CL}	t_{WL}	Clock Low Time		300		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HHCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active		100		ns
t_{CLHL}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ Inactive		100		ns
t_{CHSH}		$\overline{S}$ not Active after Rising Edge of C		200		ns
t_{SHCH}		$\overline{S}$ not Active before next C Pulse		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			200	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			200	ns

Figure 14. Serial Input Timing

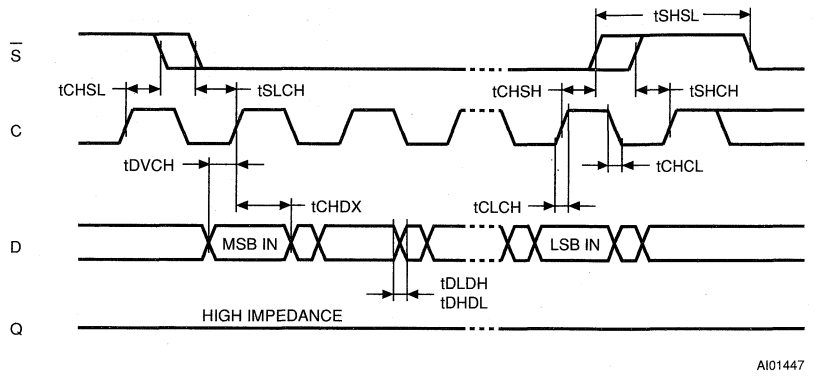


Figure 15. Hold Timing

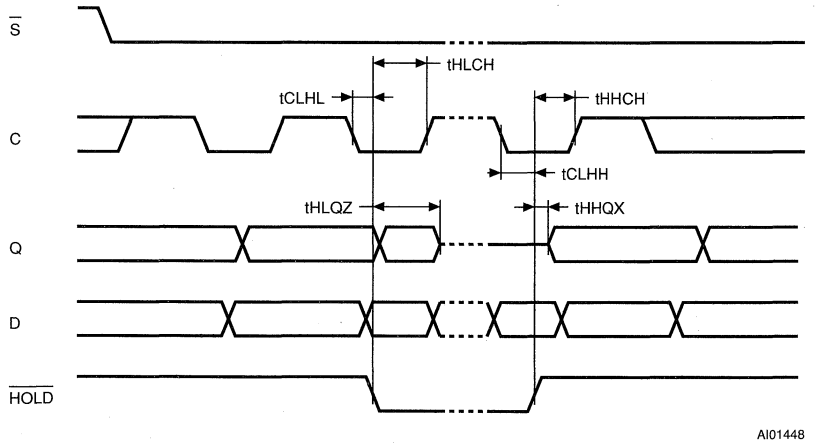
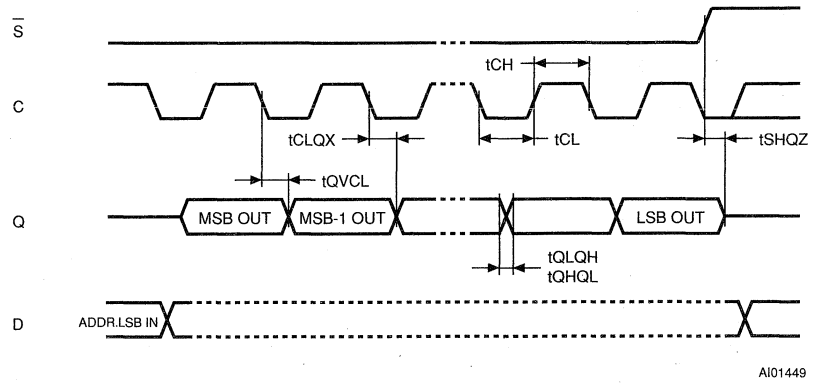
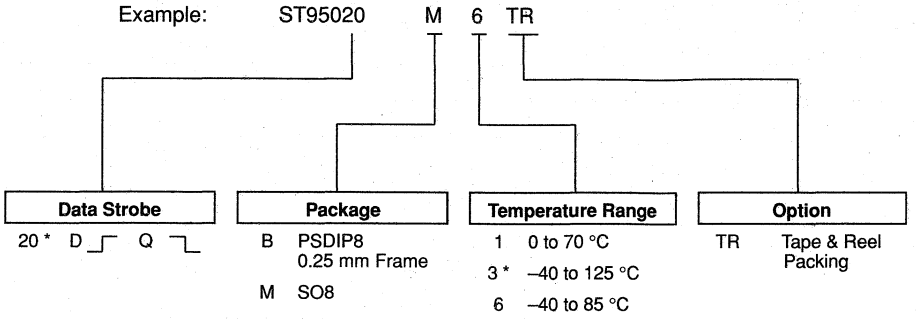


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



Notes: 20 * Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
3 * Temperature range on special request only.

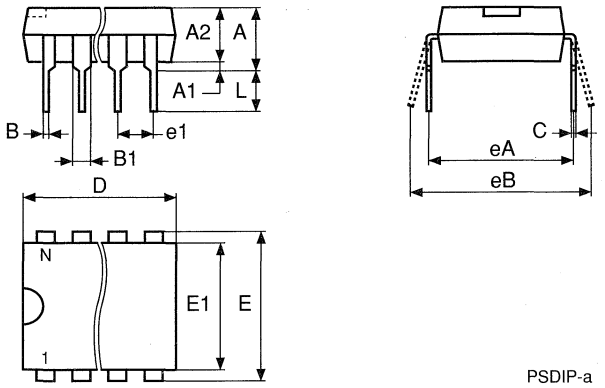
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



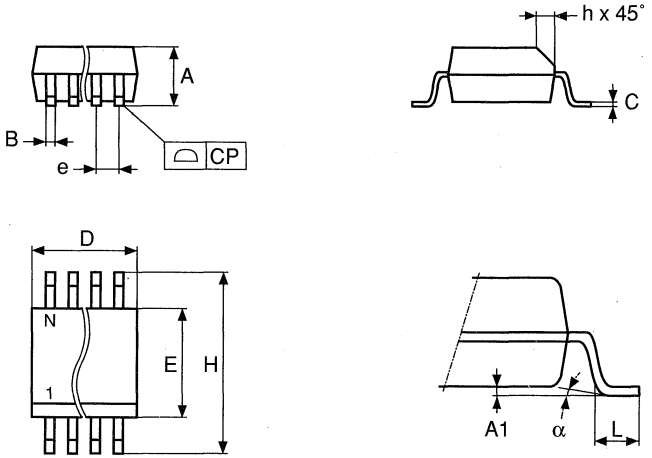
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



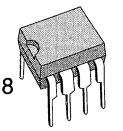
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 2K (256 x 8) EEPROM

PRODUCT PREVIEW

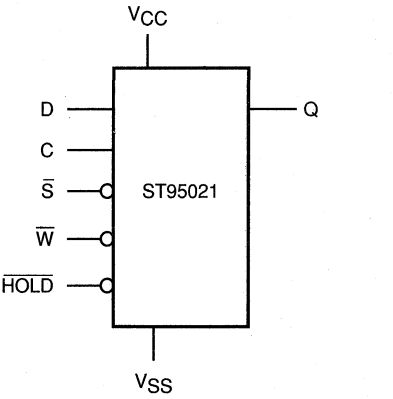
- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS NEGATIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST95021 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

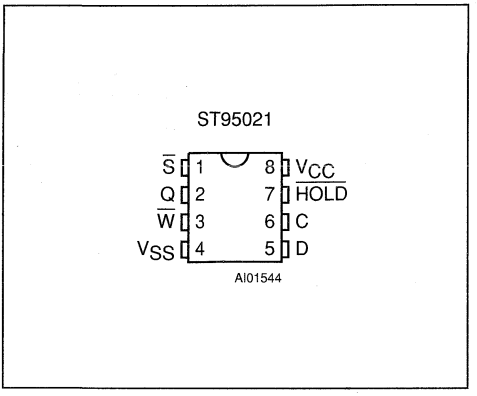


Figure 2B. SO Pin Connections

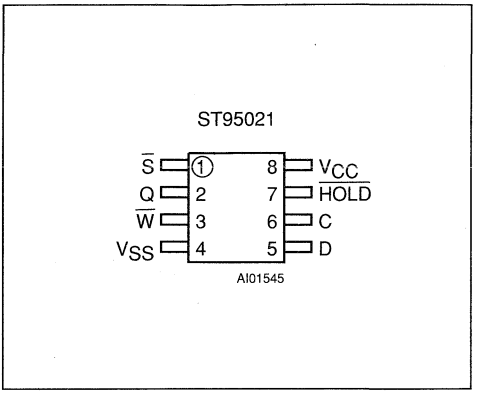


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data are clocked in during the high to low transition of clock C, data are clocked out during the low to high transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out. Data is shifted out on the rising edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the falling edge of the serial clock.

Figure 3. Data and Clock Timing

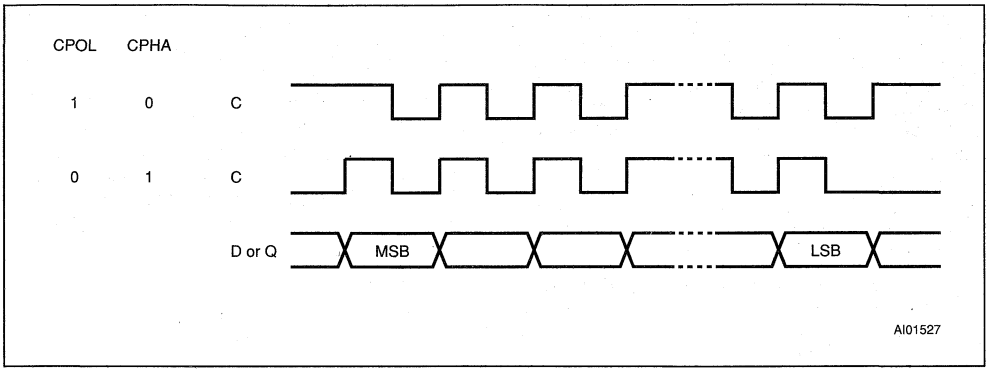
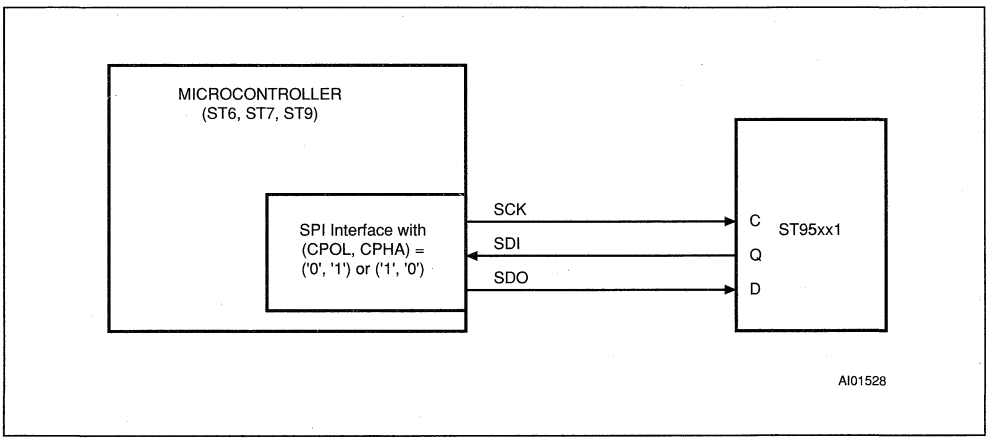


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the falling edge of the clock input, while data on the Q pin changes after the rising edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the ST95021 is deselected and the D output pin is at high impedance and unless an internal write operation is underway the S95021 will be in the standby power mode. $\overline{S}$ low enables the ST95021, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold (HOLD). The HOLD pin is used to pause serial communications without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on HOLD when C is low. To resume the communications, HOLD is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95021 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The ST95021 can be driven by a microcontroller with its SPI peripheral running in either two of the following modes: (CPOL, CPHA) = ('1', '0') or (CPOL, CPHA) = ('0', '1').

For these two modes, input data are latched in by the high to low transition of clock C, and output data are available from the low to high transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 1) and (CPOL, CPHA) = (1, 0) is the stand-by polarity: C remains to '0' for (CPOL, CPHA) = (0, 1) and C remains to 1 for (CPOL, CPHA) = (1, 0) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first falling edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the falling edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95021 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95021, the circuit executes the instruction and enters a wait mode until it is deselected.

Table 3. Write Protected Block Size

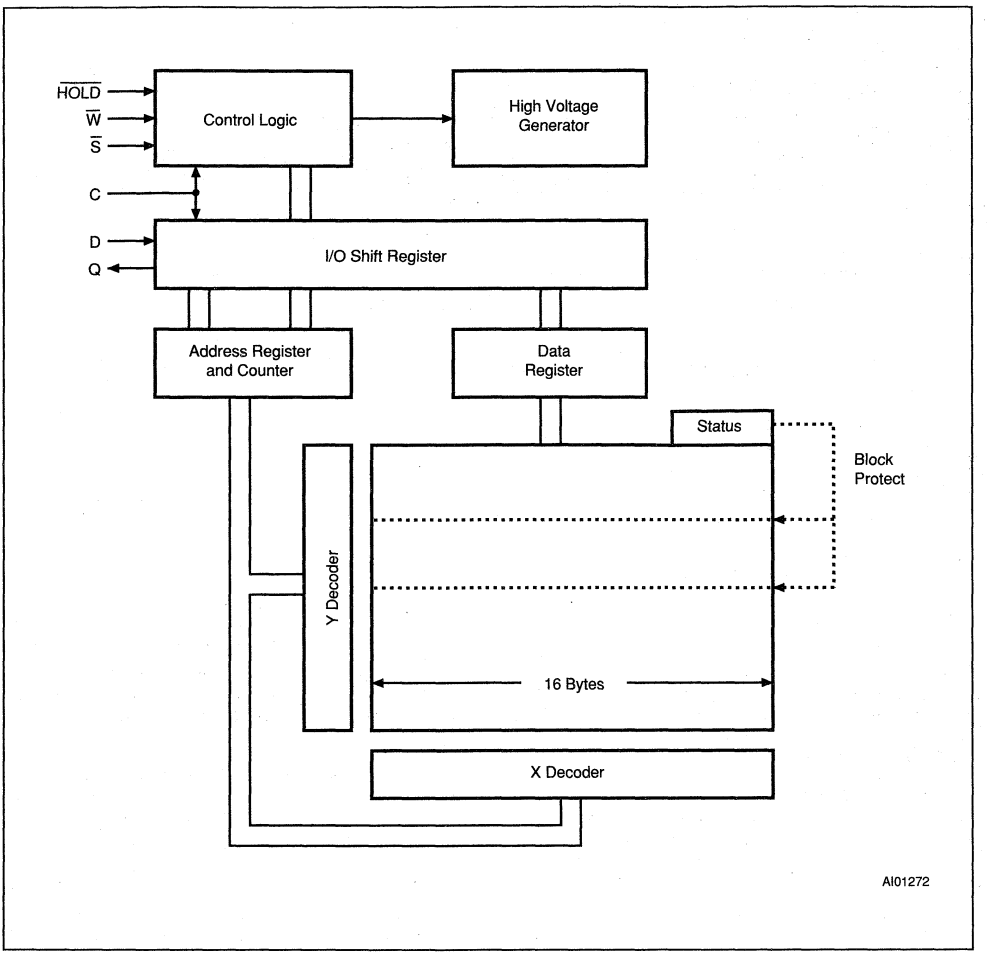
Status Register Bits		Array Addresses Protected	Protected Block
BP1	BP0		
0	0	none	none
0	1	C0h - FFh	Upper quart
1	0	80h - FFh	Upper half
1	1	00h - FFh	Whole memory

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Notes: A = 1, Upper page selected
A = 0, Lower page selected

Figure 5. Block Diagram



Read Status Register (RDSR)

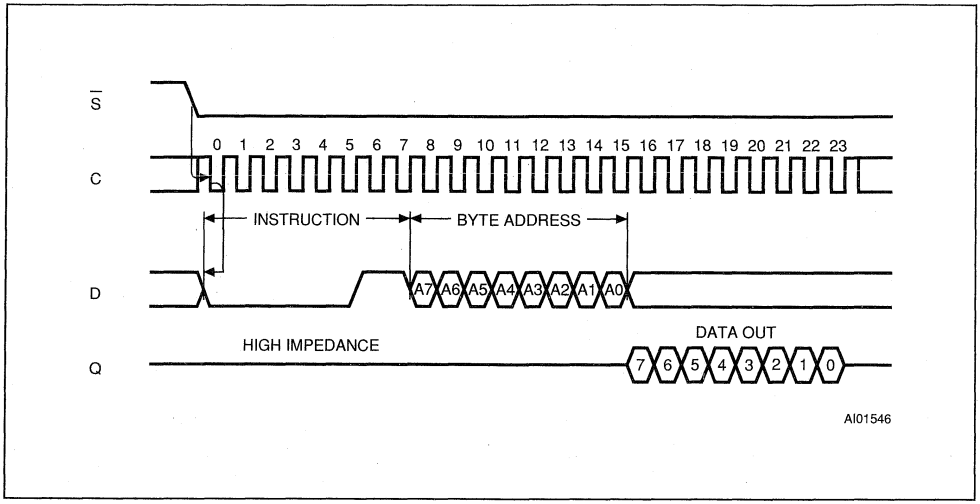
The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95021 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

Figure 6. Read Operation Sequence



OPERATIONS (cont'd)

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95021 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95021 is divided into four 512 bit blocks. The user may read the blocks but will be unable to write within the selected blocks. The blocks and respective WRSR control bits are shown in Table 3.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the falling edge of the clock (C). Bit 4 of the read instruction contain address bit A8 (most significant address bit). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the rising edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

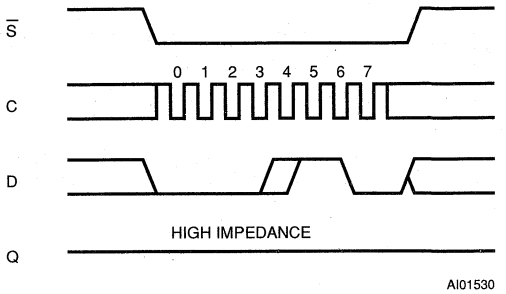


Figure 8. Write Operation Sequence

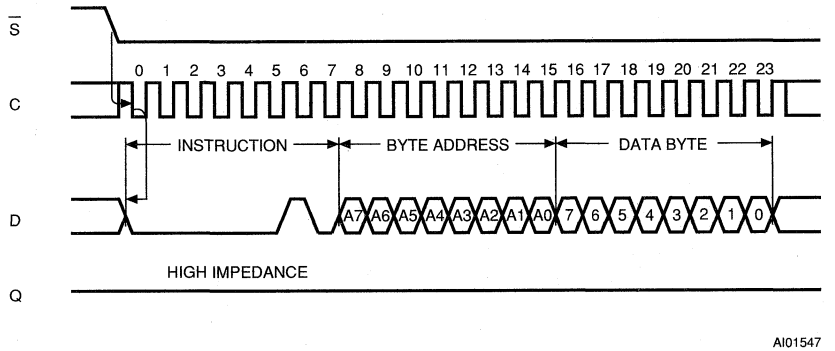


Figure 9. Page Write Operation Sequence

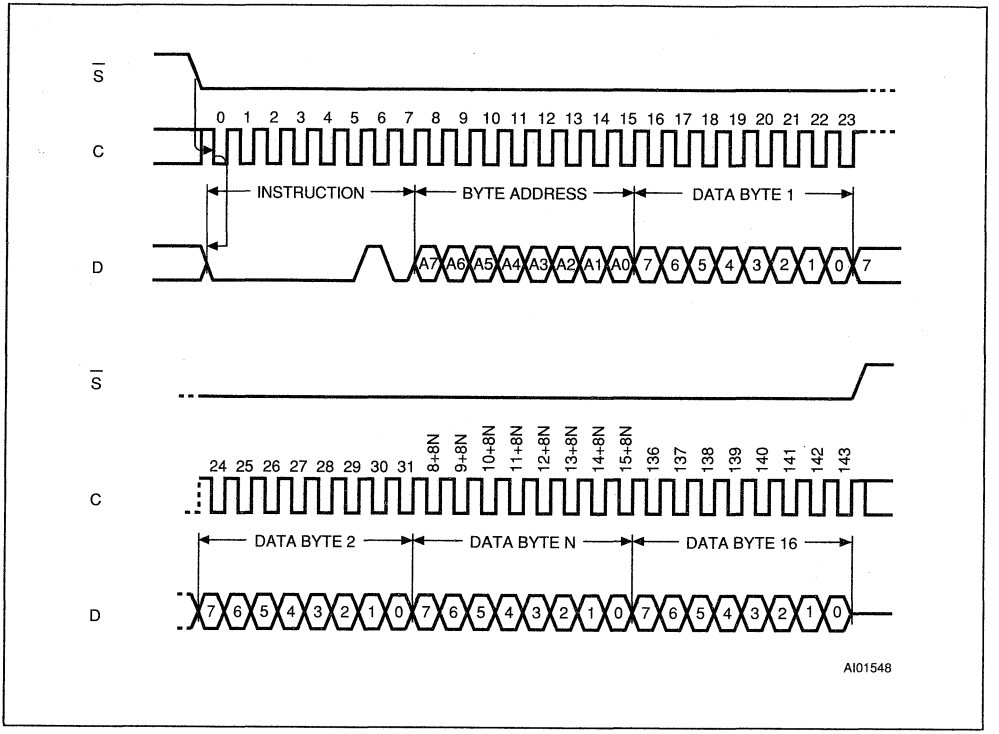


Figure 10. RDSR: Read Status Register Sequence

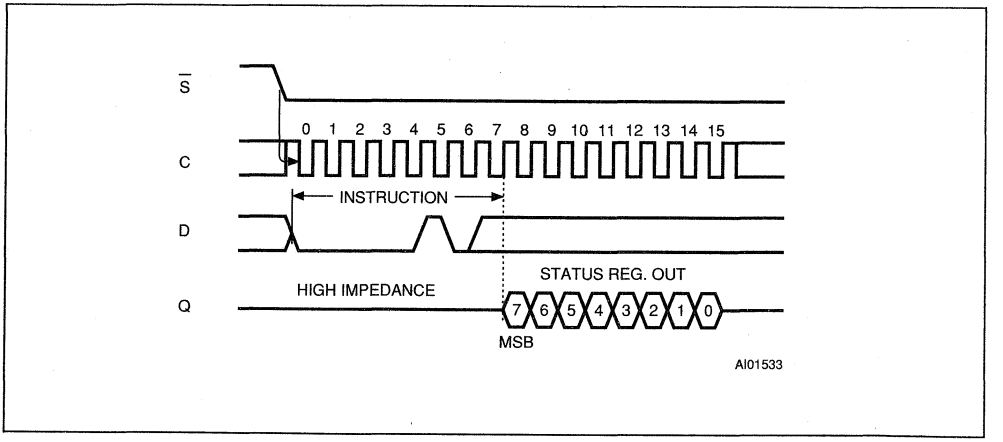
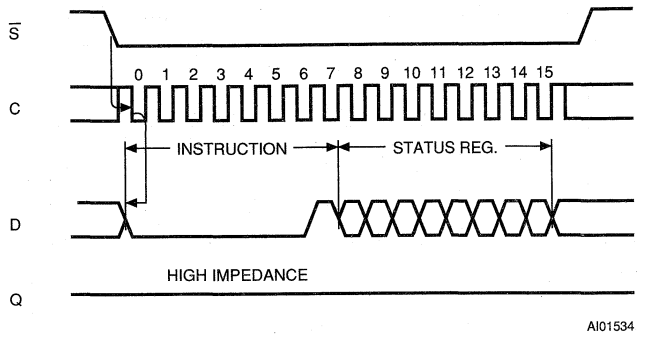


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95021 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remains low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

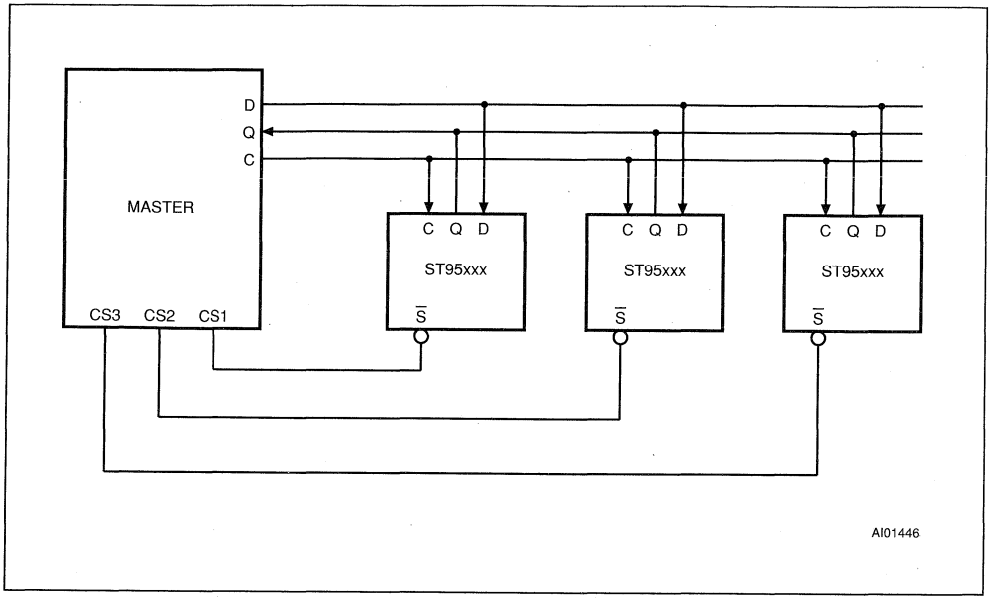
A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur just after the eigth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95021 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

Figure 12. EEPROM and SPI Bus



DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register), i.e. the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Waveforms

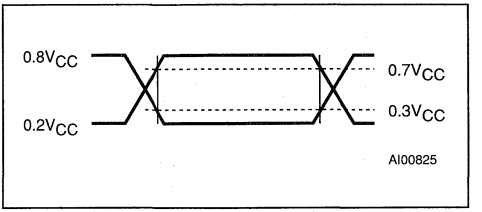


Table 5. Input Parameters (1) (T_A = 25 °C, f = 2 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = 2mA	V_{CC} –0.6		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.

Table 7. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCL}	t_{CSS}	$\overline{S}$ Active Setup Time		100		ns
t_{CLSL}		$\overline{S}$ Active after Falling Edge of C		100		ns
t_{CH}	t_{WH}	Clock High Time		300		ns
t_{CL}	t_{WL}	Clock Low Time		200		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CLDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HHCL}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{HLCL}		Clock High Hold Time after $\overline{HOLD}$ Active		100		ns
t_{CHHL}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ Inactive		100		ns
t_{CLSH}		$\overline{S}$ not Active after Falling Edge of C		200		ns
t_{SHCL}		$\overline{S}$ not Active before next C Pulse		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			200	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CHQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			200	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			200	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data are available.

Figure 14. Serial Input Timing

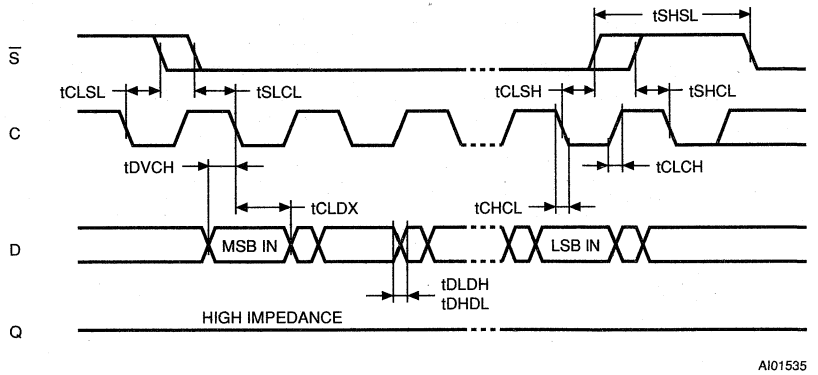


Figure 15. Hold Timing

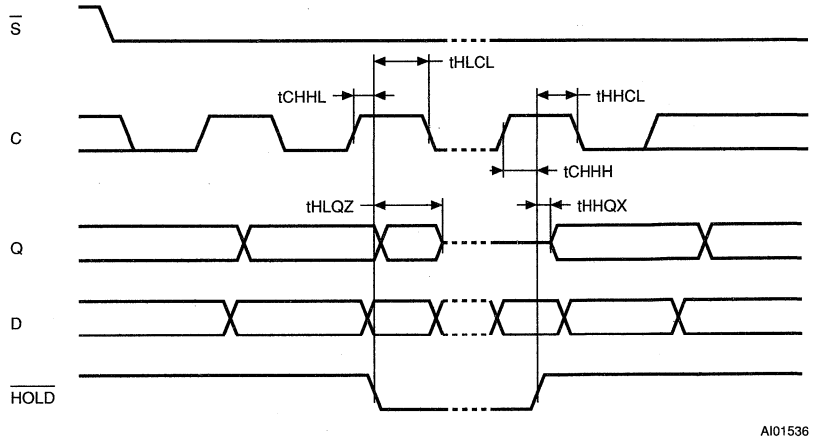
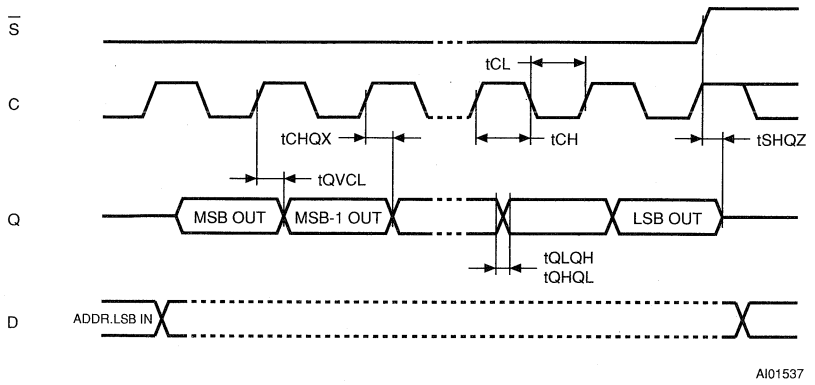
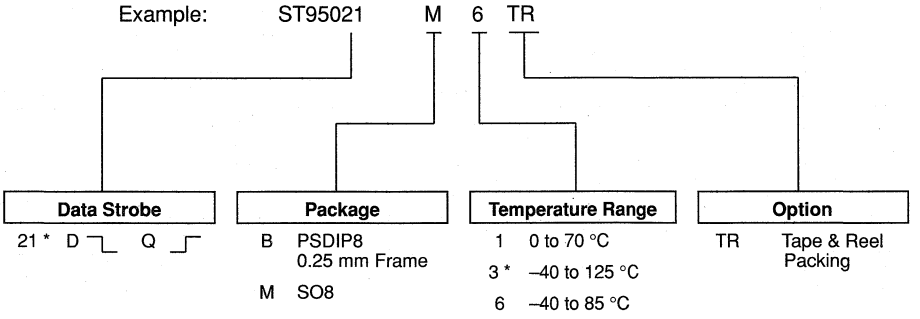


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



Notes: 21 * Data In strobed on falling edge of the clock (C) and Data Out synchronized from the rising edge of the clock.
3 * Temperature range on special request only.

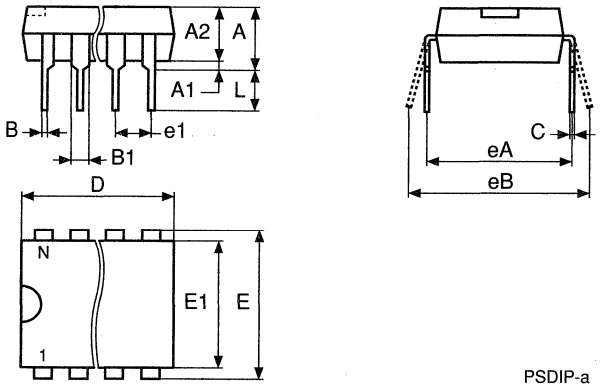
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	
CP			0.10			0.004

PSDIP8



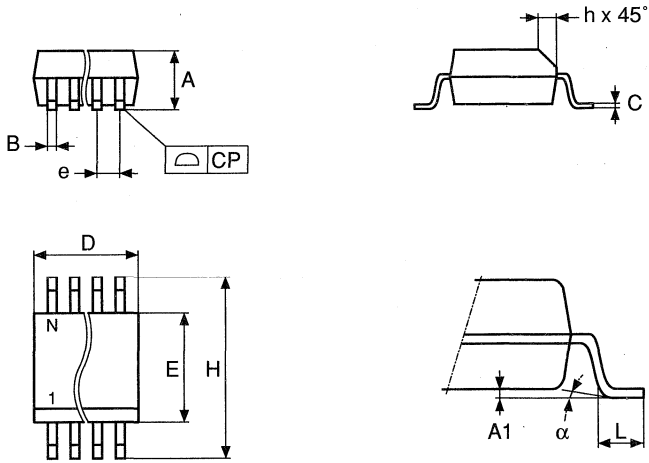
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



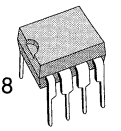
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 4K (512 x 8) EEPROM

PRELIMINARY DATA

- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

The ST95040 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

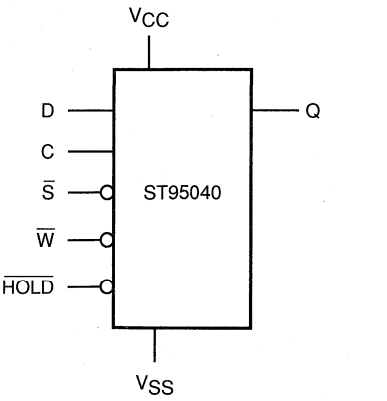


Figure 2A. DIP Pin Connections

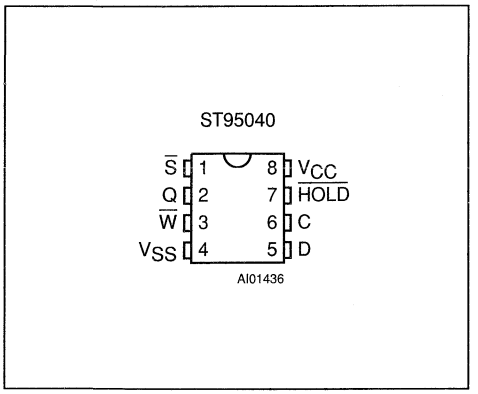


Figure 2B. SO Pin Connections

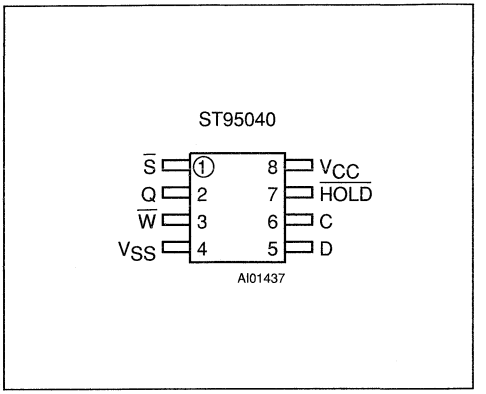


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data are clocked in during the low to high transition of clock C, data are clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the ST95040. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Figure 3. Data and Clock Timing

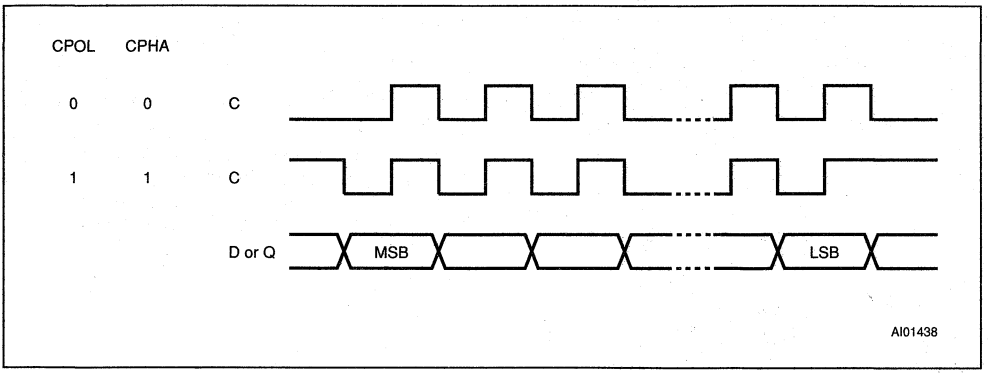
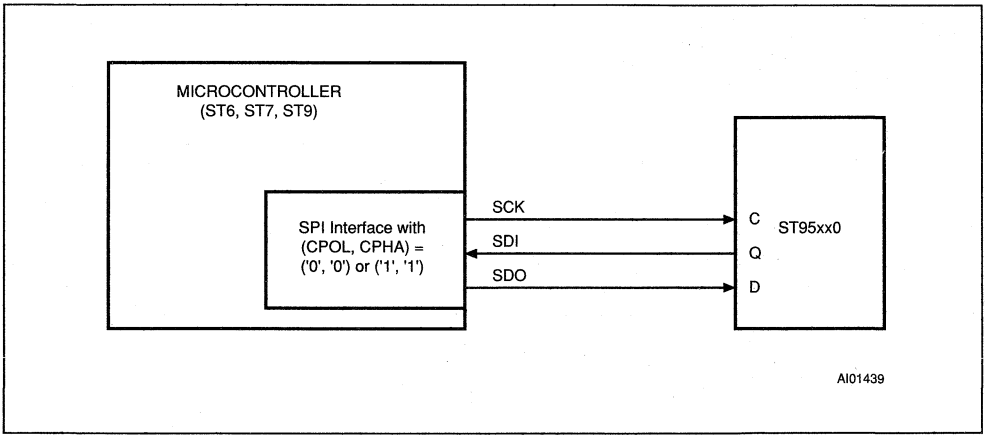


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the ST95040 is deselected and the D output pin is at high impedance and unless an internal write operation is underway the S95040 will be in the standby power mode. $\overline{S}$ low enables the ST95040, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95040 are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95040 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95040 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The ST95040 can be driven by a microcontroller with its SPI peripheral running in either two of the following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data are latched in by the low to high transition of clock C, and output data are available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains to '0' for (CPOL, CPHA) = (0, 0) and C remains to 1 for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95040 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95040, the circuit executes the instruction and enters a wait mode until it is deselected.

Table 3. Write Protected Block Size

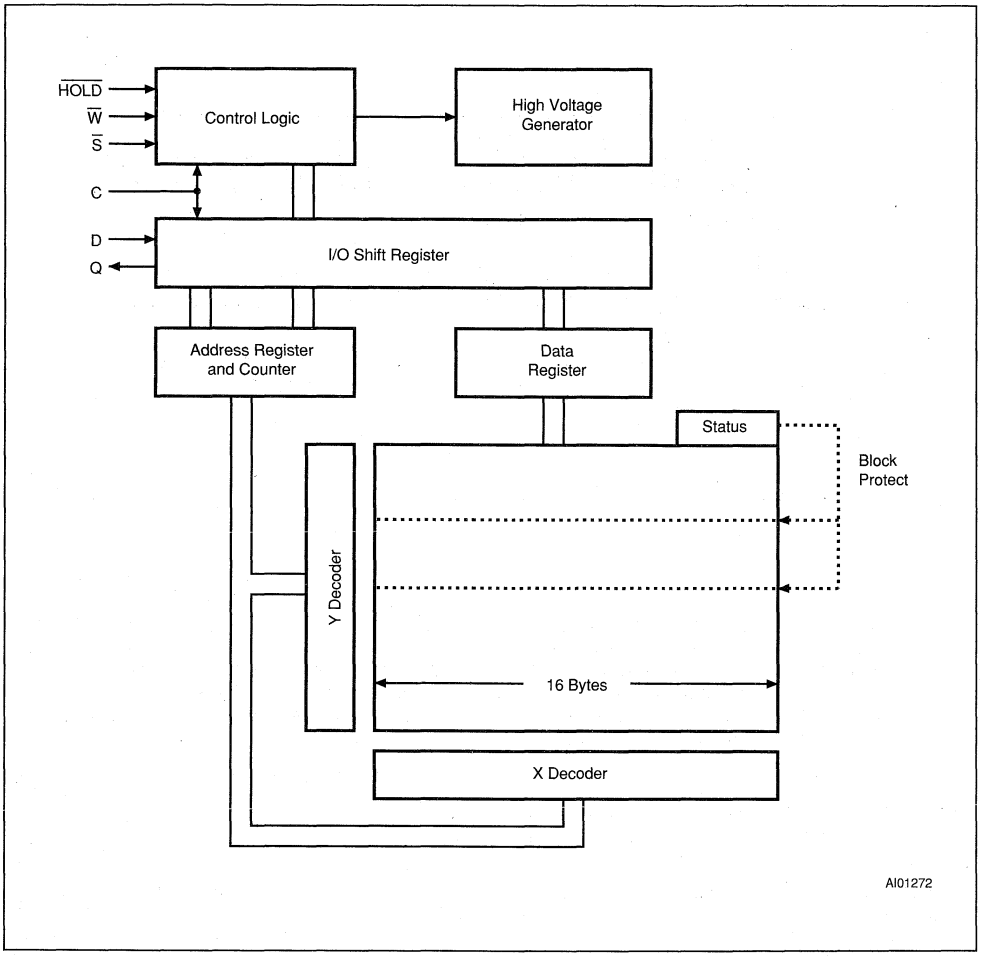
Status Register Bits		Array Addresses Protected	Protected Block
BP1	BP0		
0	0	none	none
0	1	180h - 1FFh	Upper quart
1	0	100h - 1FFh	Upper half
1	1	000h - 1FFh	Whole memory

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 X110
WRDI	Reset Write Enable Latch	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read Data from Memory Array	0000 A010
WRITE	Write Data to Memory Array	0000 A011

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

Figure 5. Block Diagram



Read Status Register (RDSR)

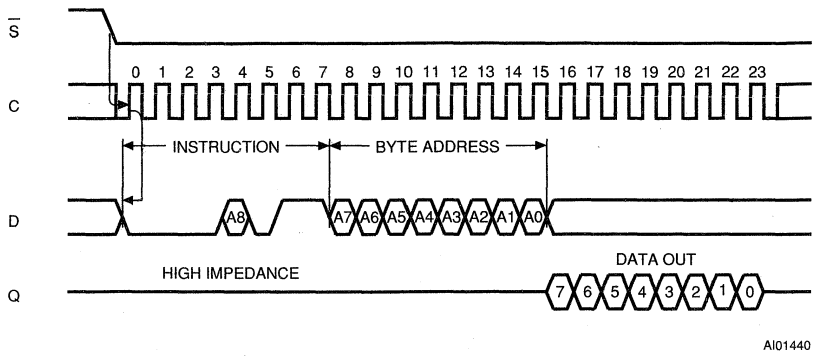
The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95040 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

Figure 6. Read Operation Sequence



OPERATIONS (cont'd)

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95040 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95040 is divided into four 1024 bit blocks. The user may read the blocks but will be unable to write within the selected blocks. The blocks and respective WRSR control bits are shown in Table 3.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 4 of the read instruction contain address bit A8 (most significant address bit). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

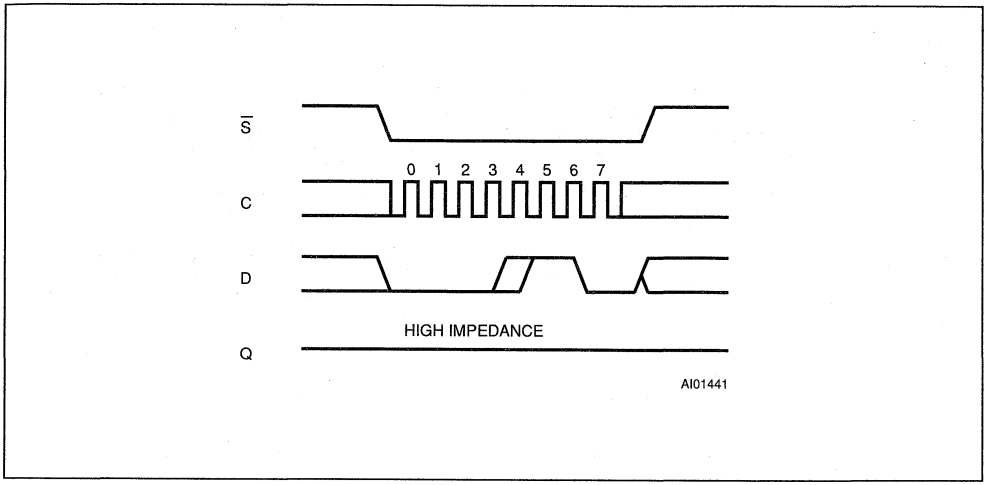


Figure 8. Write Operation Sequence

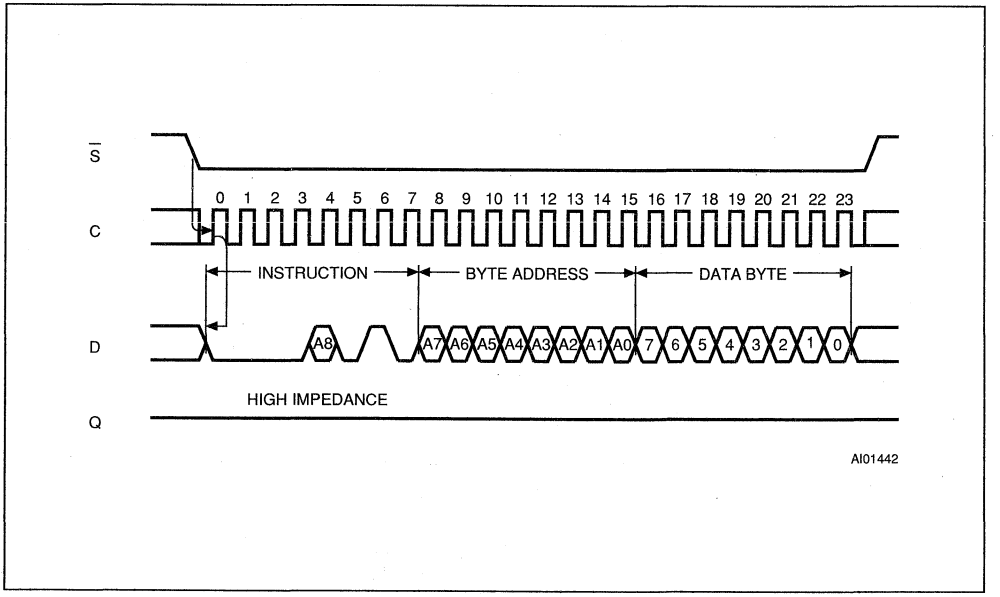


Figure 9. Page Write Operation Sequence

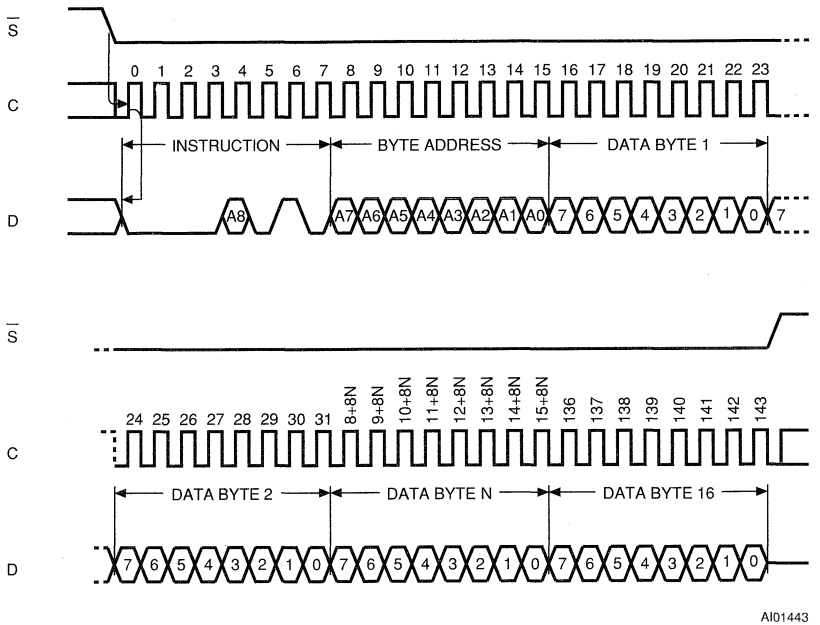


Figure 10. RDSR: Read Status Register Sequence

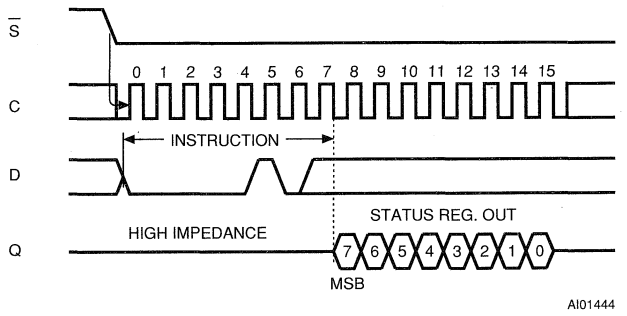
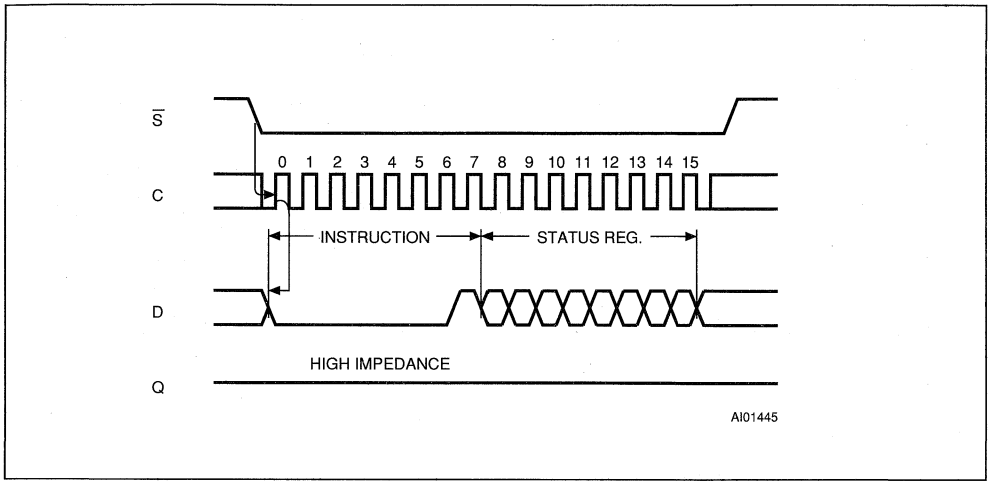


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95040 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remains low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

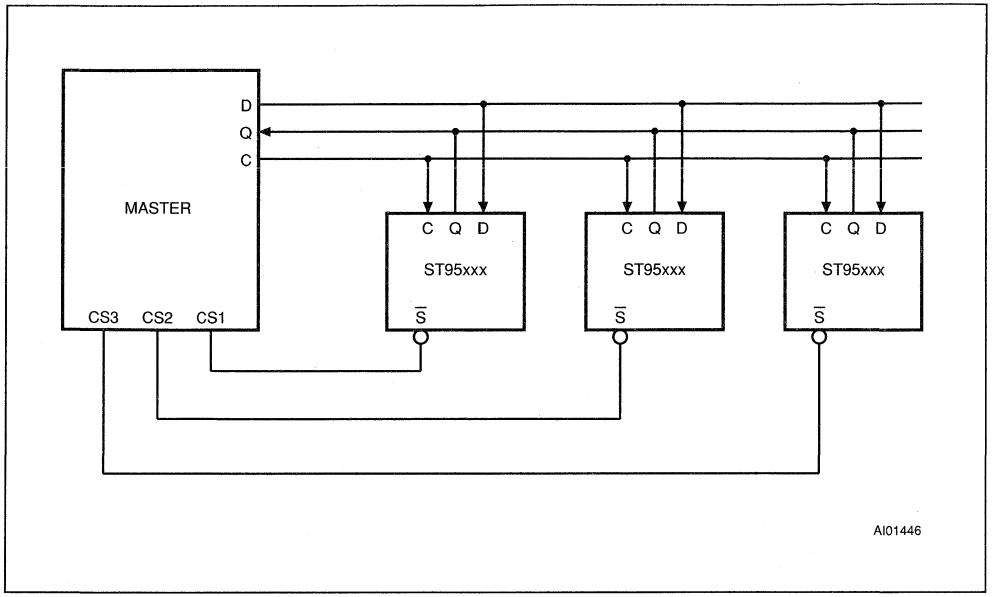
A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur just after the eigth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95040 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

Figure 12. EEPROM and SPI Bus



DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register), i.e. the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Waveforms

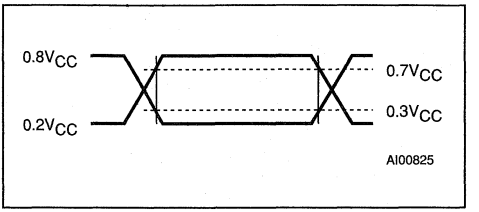


Table 5. Input Parameters (1) (T_A = 25 °C, f = 2 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC}, @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = 2mA	V_{CC} –0.6		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.

Table 7. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time		100		ns
t_{CHSL}		$\overline{S}$ Active after Rising Edge of C		100		ns
t_{CH}	t_{WH}	Clock High Time		200		ns
t_{CL}	t_{WL}	Clock Low Time		300		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HHCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active		100		ns
t_{CLHL}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ Inactive		100		ns
t_{CHSH}		$\overline{S}$ not Active after Rising Edge of C		200		ns
t_{SHCH}		$\overline{S}$ not Active before next C Pulse		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			200	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			200	ns

Figure 14. Serial Input Timing

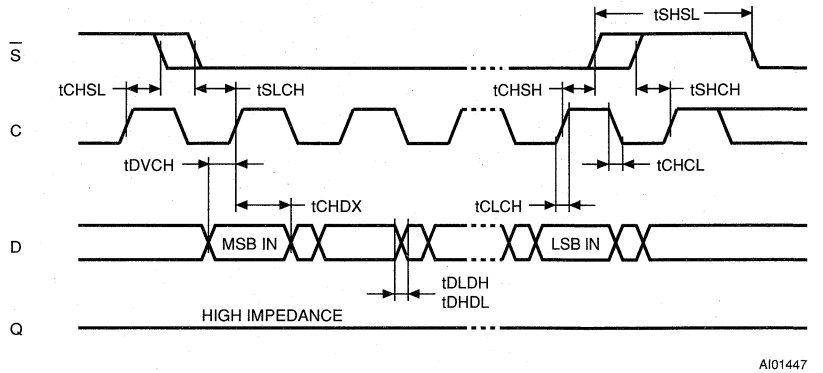


Figure 15. Hold Timing

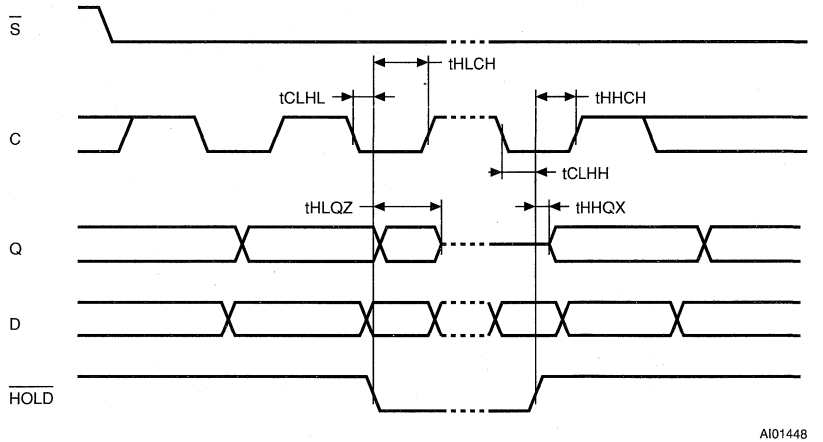
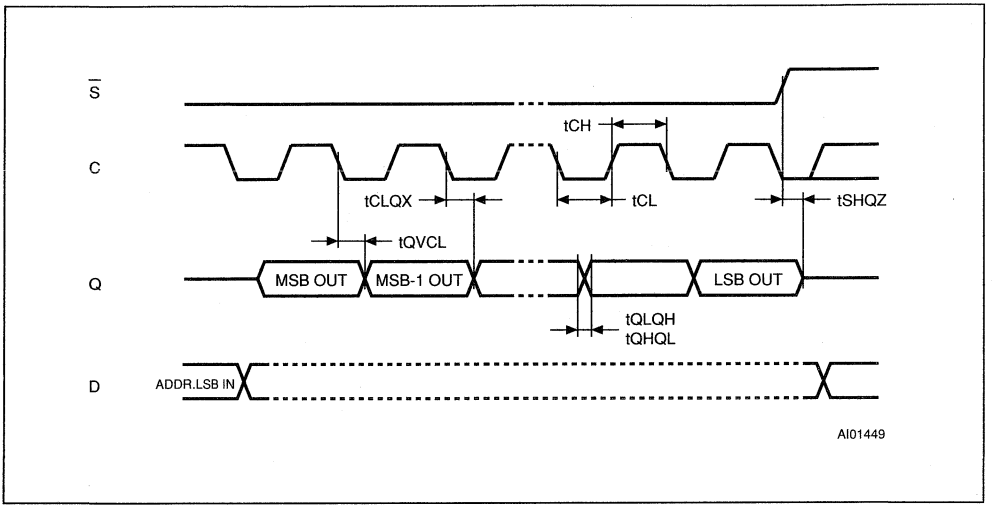
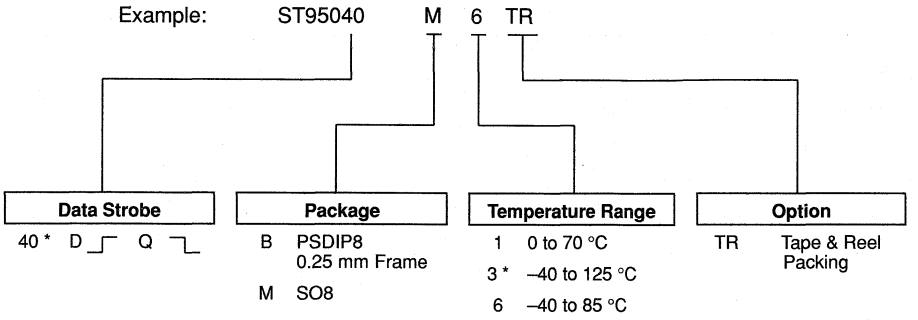


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



Notes: 40 * Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
3 * Temperature range on special request only.

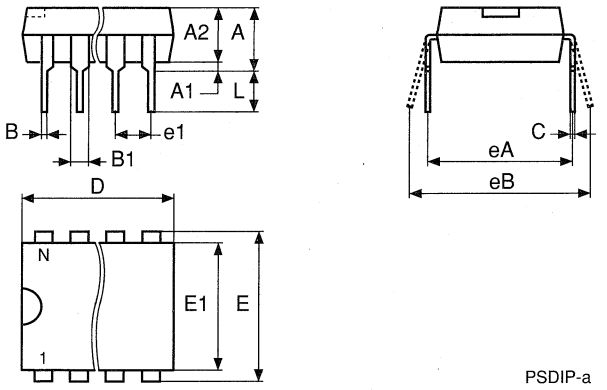
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	
CP			0.10			0.004

PSDIP8



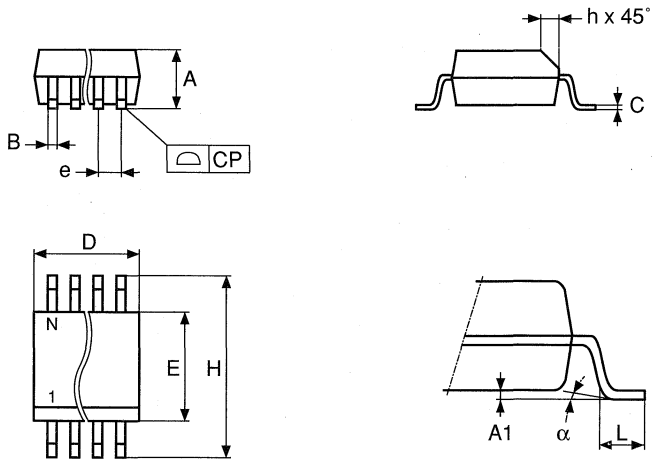
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



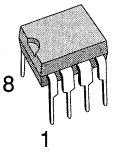
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 4K (512 x 8) EEPROM

PRELIMINARY DATA

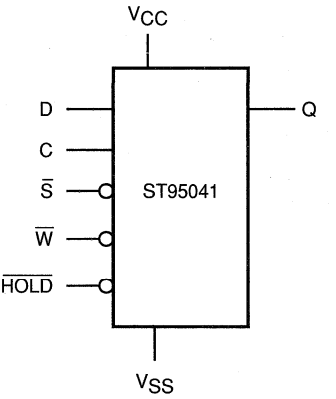
- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS NEGATIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST95041 is a 4K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

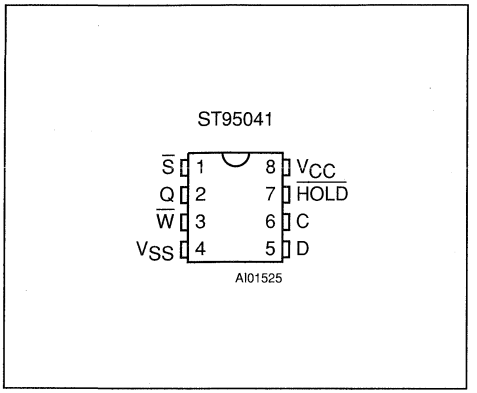


Figure 2B. SO Pin Connections

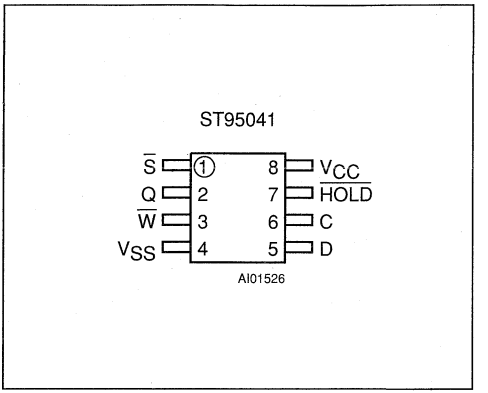


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data are clocked in during the high to low transition of clock C, data are clocked out during the low to high transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the ST95041. Data is shifted out on the rising edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the falling edge of the serial clock.

Figure 3. Data and Clock Timing

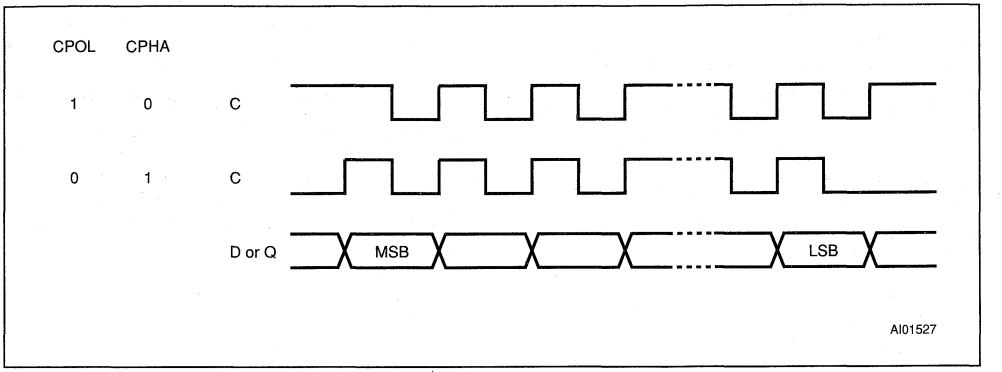
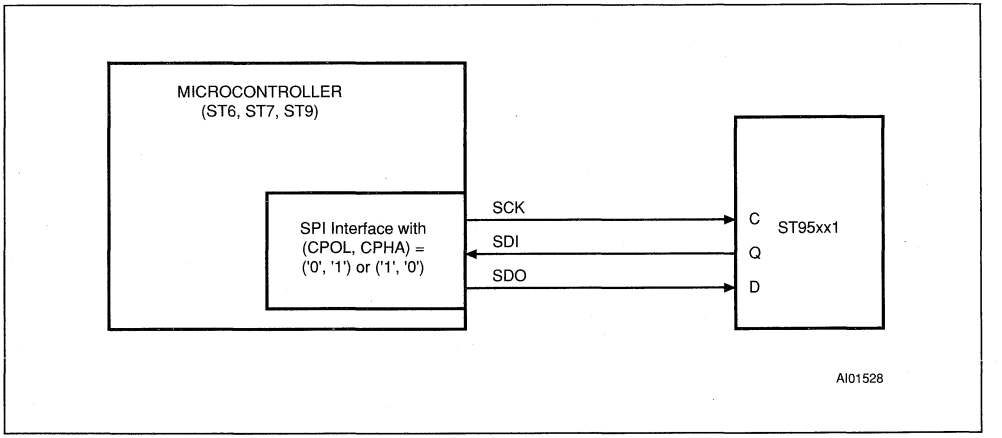


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the falling edge of the clock input, while data on the Q pin changes after the rising edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the ST95041 is deselected and the D output pin is at high impedance and unless an internal write operation is underway the S95041 will be in the standby power mode. $\overline{S}$ low enables the ST95041, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95041 are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95041 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95041 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The ST95041 can be driven by a microcontroller with its SPI peripheral running in either two of the following modes: (CPOL, CPHA) = ('1', '0') or (CPOL, CPHA) = ('0', '1').

For these two modes, input data are latched in by the high to low transition of clock C, and output data are available from the low to high transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 1) and (CPOL, CPHA) = (1, 0) is the stand-by polarity: C remains to '0' for (CPOL, CPHA) = (0, 1) and C remains to 1 for (CPOL, CPHA) = (1, 0) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first falling edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the falling edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95041 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95041, the circuit executes the instruction and enters a wait mode until it is deselected.

Table 3. Write Protected Block Size

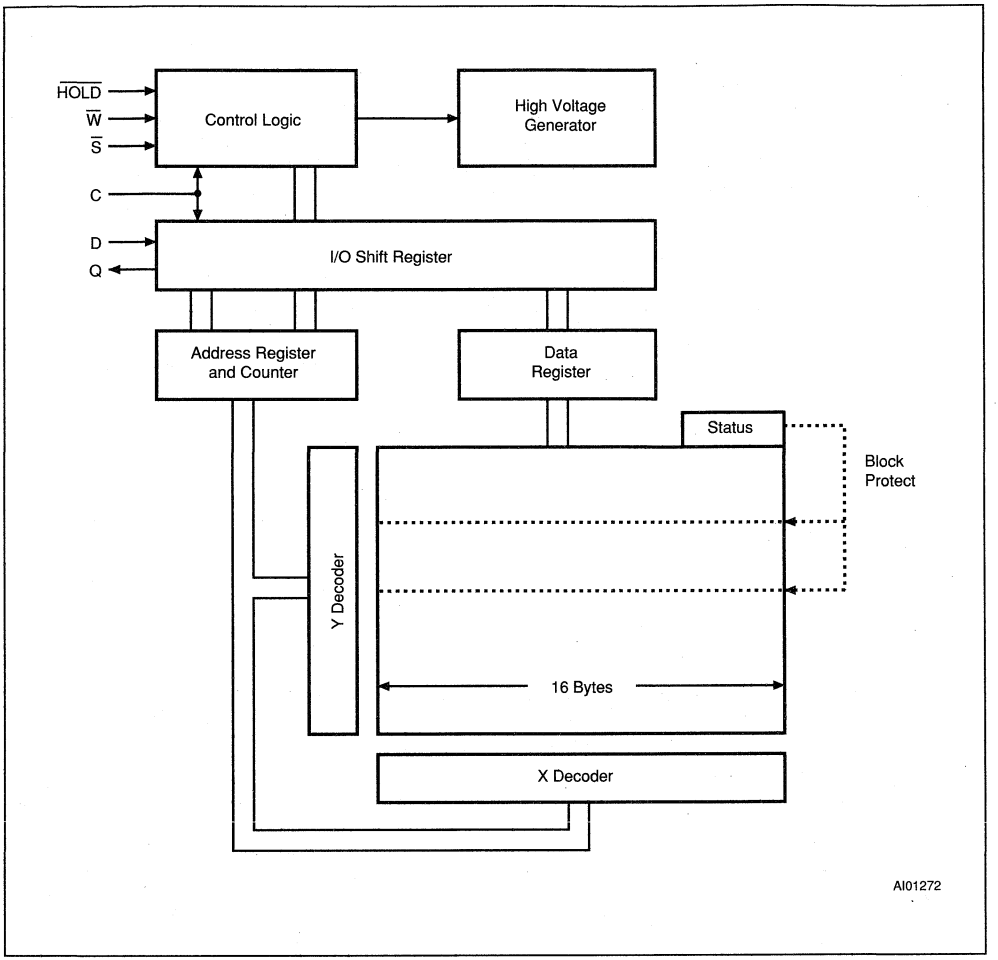
Status Register Bits		Array Addresses Protected	Protected Block
BP1	BP0		
0	0	none	none
0	1	180h - 1FFh	Upper quart
1	0	100h - 1FFh	Upper half
1	1	000h - 1FFh	Whole memory

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 X110
WRDI	Reset Write Enable Latch	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read Data from Memory Array	0000 A010
WRITE	Write Data to Memory Array	0000 A011

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

Figure 5. Block Diagram



Read Status Register (RDSR)

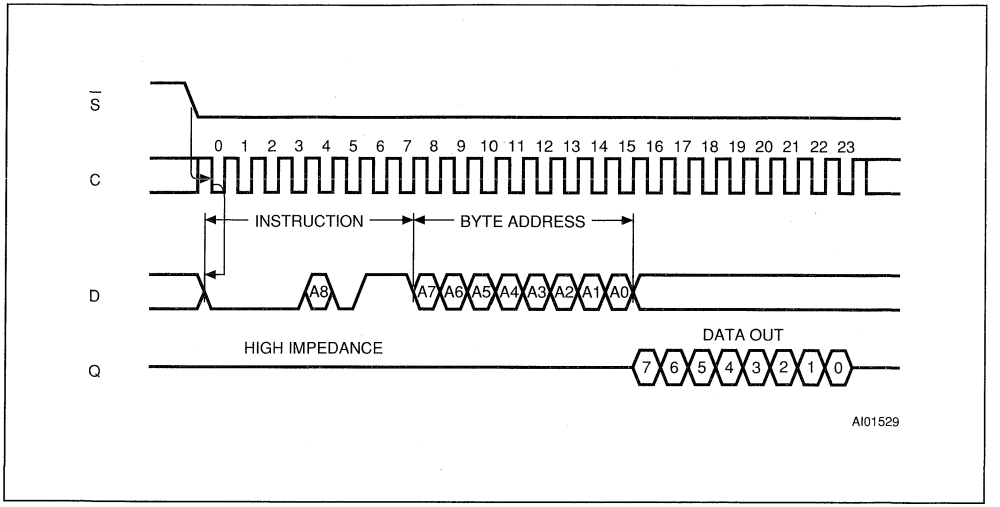
The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95041 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

Figure 6. Read Operation Sequence



OPERATIONS (cont'd)

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95041 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95041 is divided into four 1024 bit blocks. The user may read the blocks but will be unable to write within the selected blocks. The blocks and respective WRSR control bits are shown in Table 3.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the falling edge of the clock (C). Bit 4 of the read instruction contain address bit A8 (most significant address bit). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the rising edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

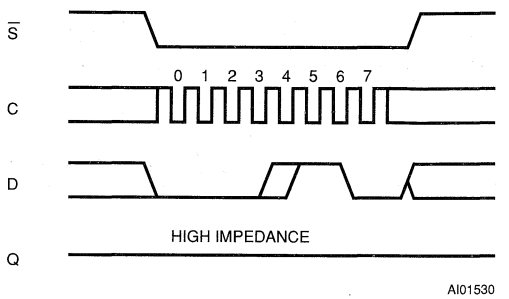


Figure 8. Write Operation Sequence

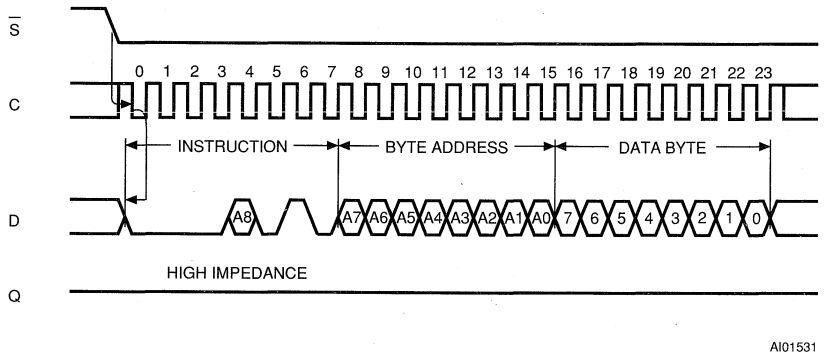


Figure 9. Page Write Operation Sequence

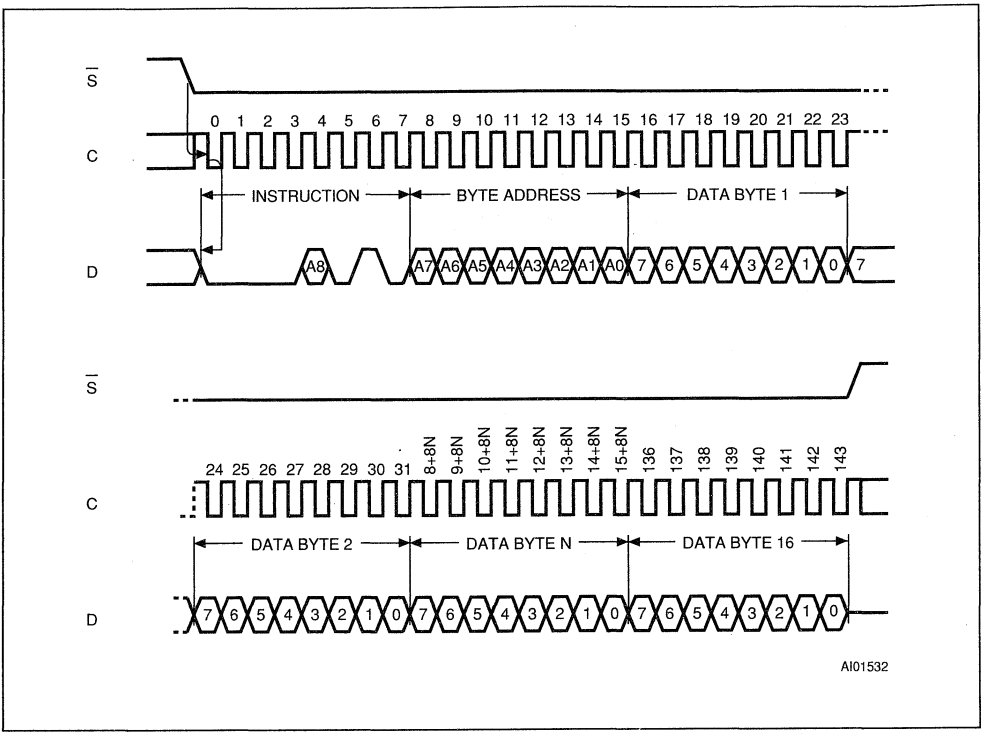


Figure 10. RDSR: Read Status Register Sequence

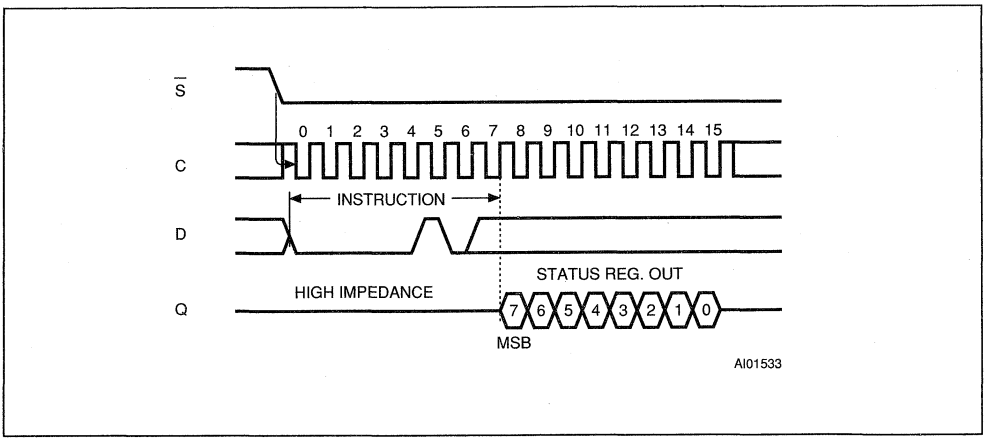
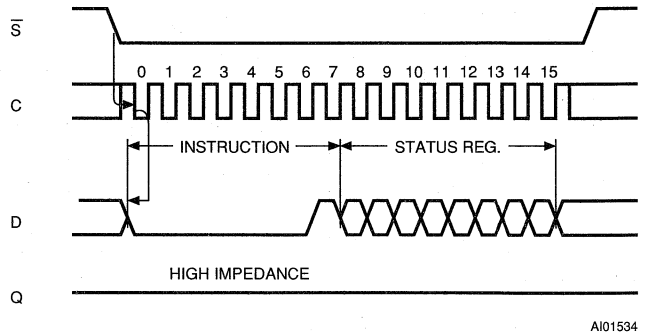


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95041 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remains low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

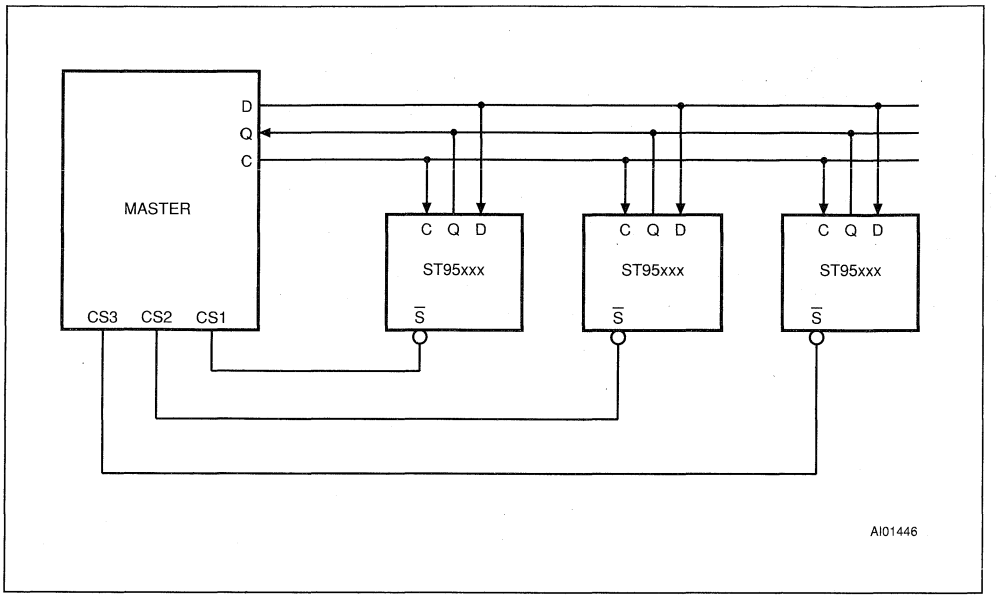
A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur just after the eigth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95041 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

Figure 12. EEPROM and SPI Bus



DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register), i.e. the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Waveforms

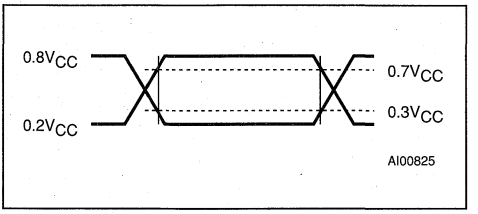


Table 5. Input Parameters (1) (T_A = 25 °C, f = 2 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = 2mA	V_{CC} –0.6		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.

Table 7. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCL}	t_{CSS}	$\overline{S}$ Active Setup Time		100		ns
t_{CLSL}		$\overline{S}$ Active after Falling Edge of C		100		ns
t_{CH}	t_{WH}	Clock High Time		300		ns
t_{CL}	t_{WL}	Clock Low Time		200		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CLDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HHCL}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{HLCL}		Clock High Hold Time after $\overline{HOLD}$ Active		100		ns
t_{CHHL}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ Inactive		100		ns
t_{CLSH}		$\overline{S}$ not Active after Falling Edge of C		200		ns
t_{SHCL}		$\overline{S}$ not Active before next C Pulse		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			200	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CHQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			200	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			200	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data are available.

Figure 14. Serial Input Timing

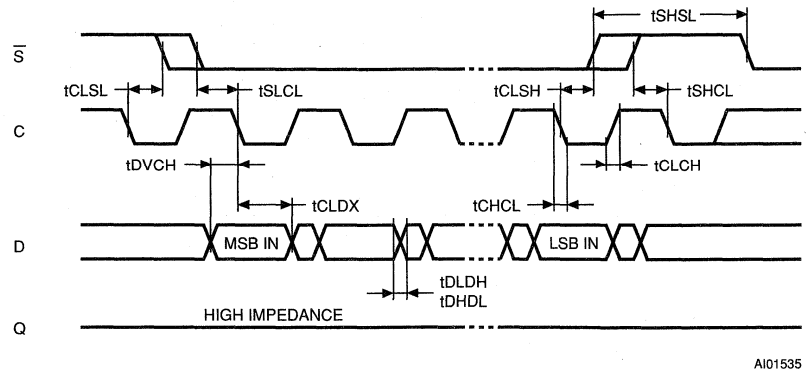


Figure 15. Hold Timing

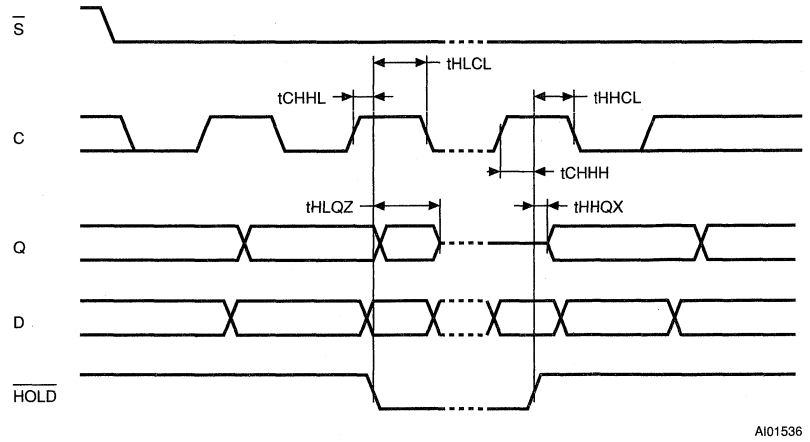
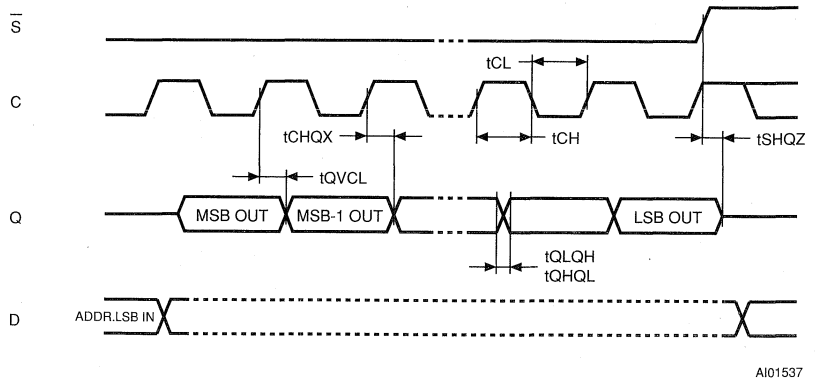
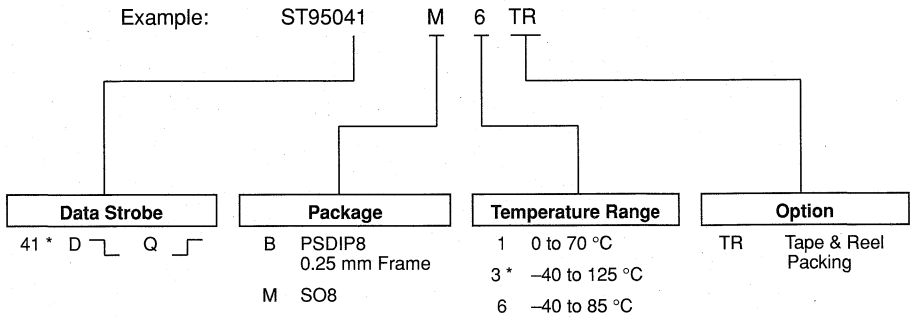


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



Notes: 41 * Data In strobed on falling edge of the clock (C) and Data Out synchronized from the rising edge of the clock.
3 * Temperature range on special request only.

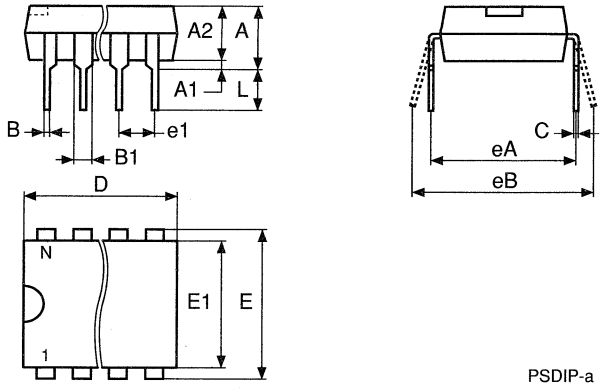
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



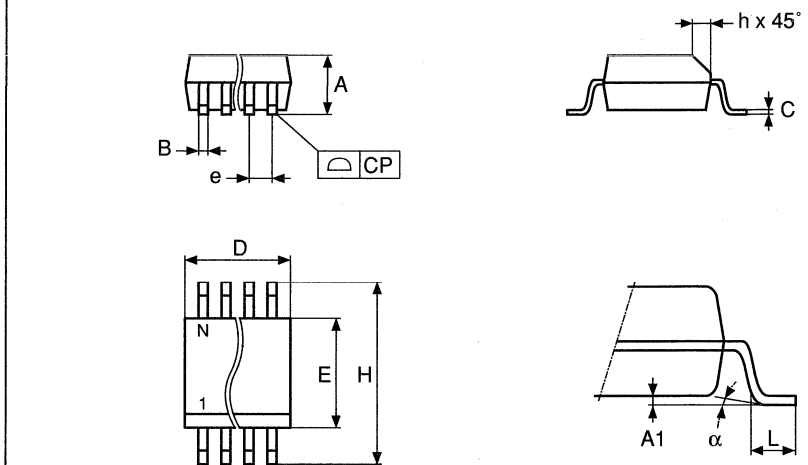
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



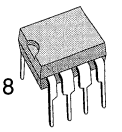
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 8K (1K x 8) EEPROM

PRODUCT PREVIEW

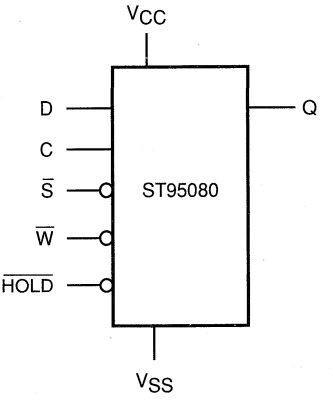
- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST95080 is an 8K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

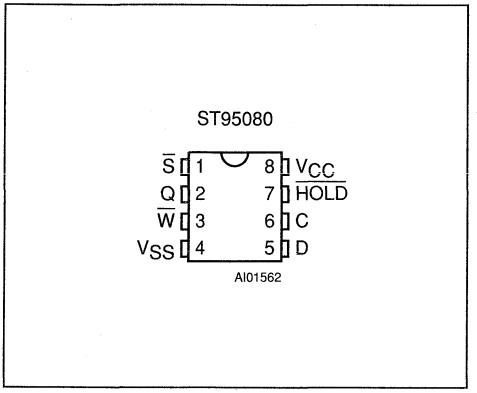


Figure 2B. SO Pin Connections

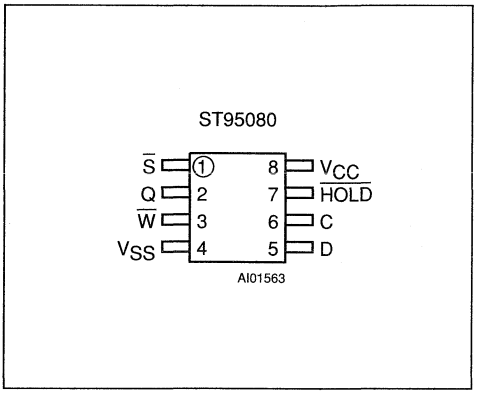


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data are clocked in during the low to high transition of clock C, data are clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Figure 3. Data and Clock Timing

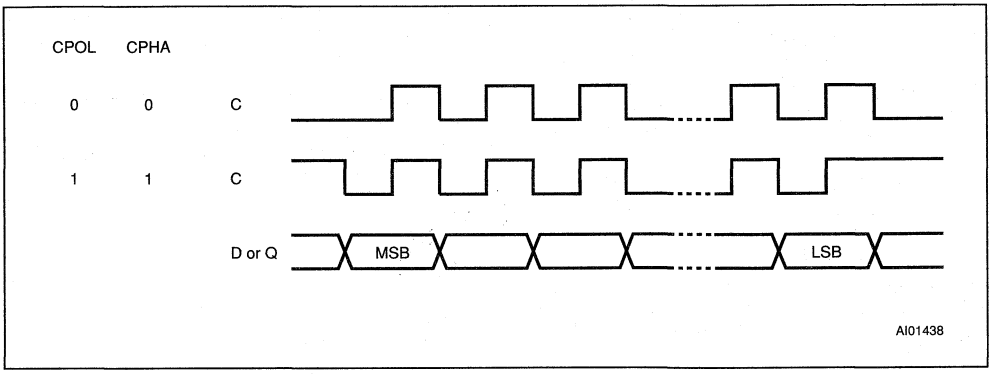
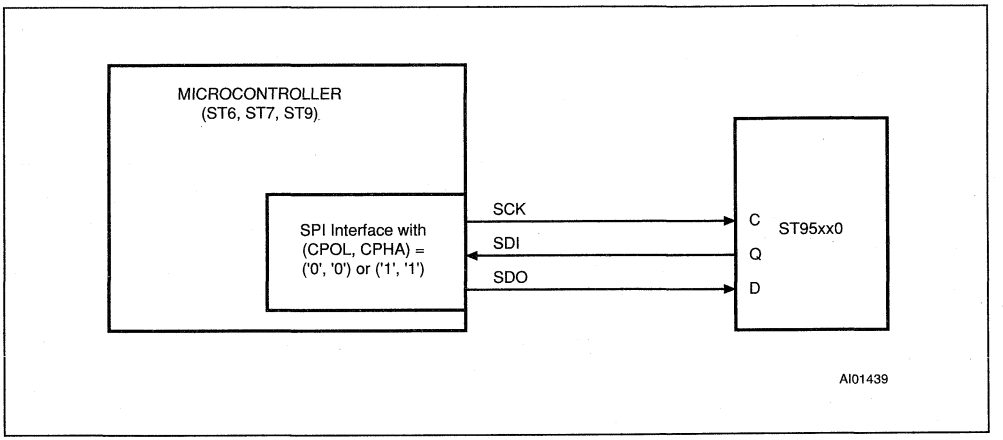


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the ST95080 is deselected and the D output pin is at high impedance and unless an internal write operation is underway the S95080 will be in the standby power mode. $\overline{S}$ low enables the ST95080, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95080 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The ST95080 can be driven by a microcontroller with its SPI peripheral running in either two of the following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data are latched in by the low to high transition of clock C, and output data are available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains to '0' for (CPOL, CPHA) = (0, 0) and C remains to 1 for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95080 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95080, the circuit executes the instruction and enters a wait mode until it is deselected.

Table 3. Write Protected Block Size

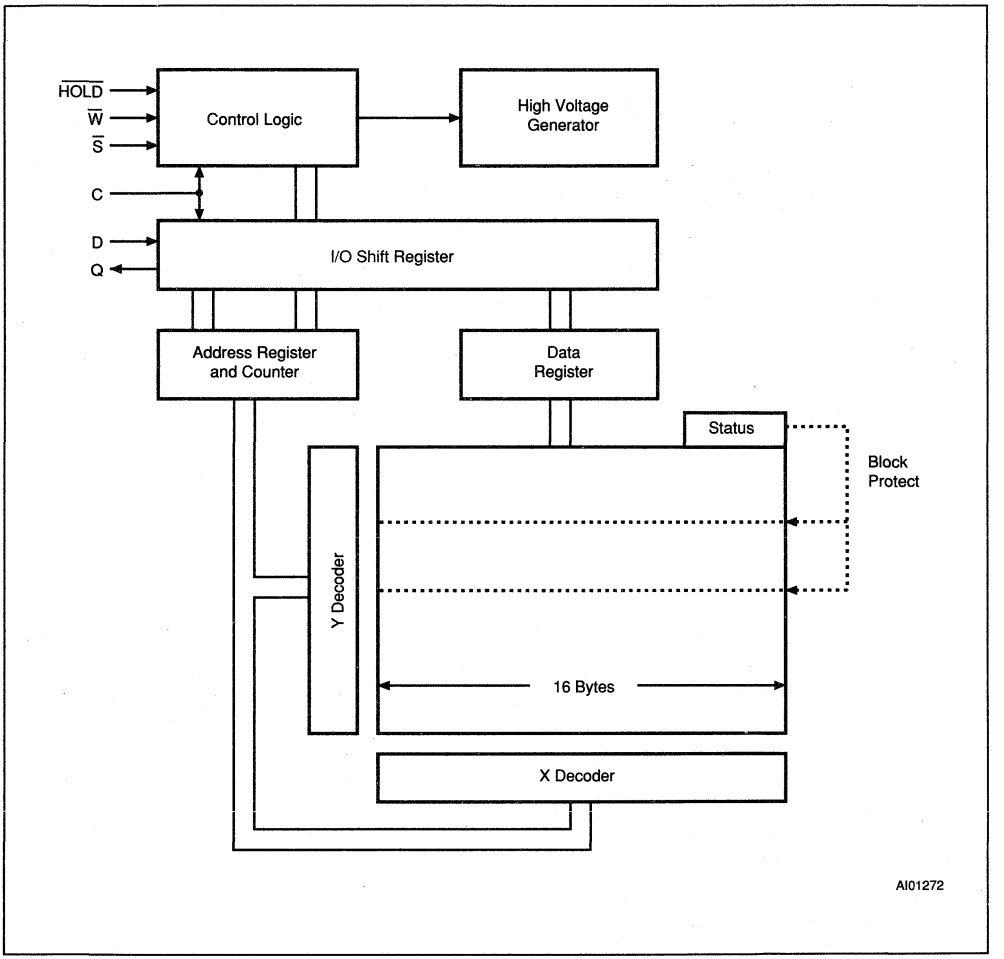
Status Register Bits		Array Addresses Protected	Protected Block
BP1	BP0		
0	0	none	none
0	1	300h - 3FFh	Upper quart
1	0	200h - 3FFh	Upper half
1	1	000h - 3FFh	Whole memory

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	000X X110
WRDI	Reset Write Enable Latch	000X X100
RDSR	Read Status Register	000X X101
WRSR	Write Status Register	000X X001
READ	Read Data from Memory Array	000A A011
WRITE	Write Data to Memory Array	000A A010

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

Figure 5. Block Diagram



Read Status Register (RDSR)

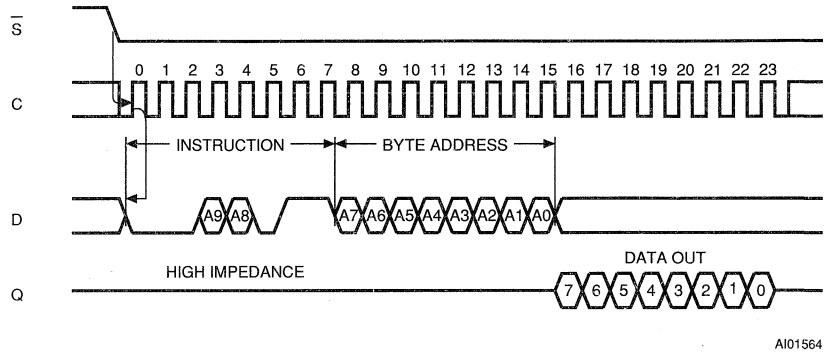
The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95080 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

Figure 6. Read Operation Sequence



OPERATIONS (cont'd)

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95080 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95080 is divided into four 2048 bit blocks. The user may read the blocks but will be unable to write within the selected blocks. The blocks and respective WRSR control bits are shown in Table 3.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 4 of the read instruction contain address bit A8 (most significant address bit). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

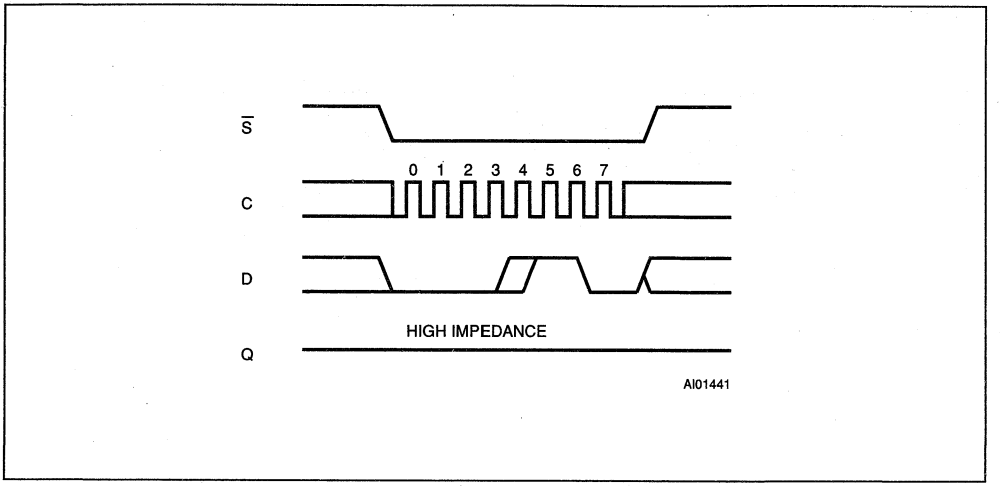


Figure 8. Write Operation Sequence

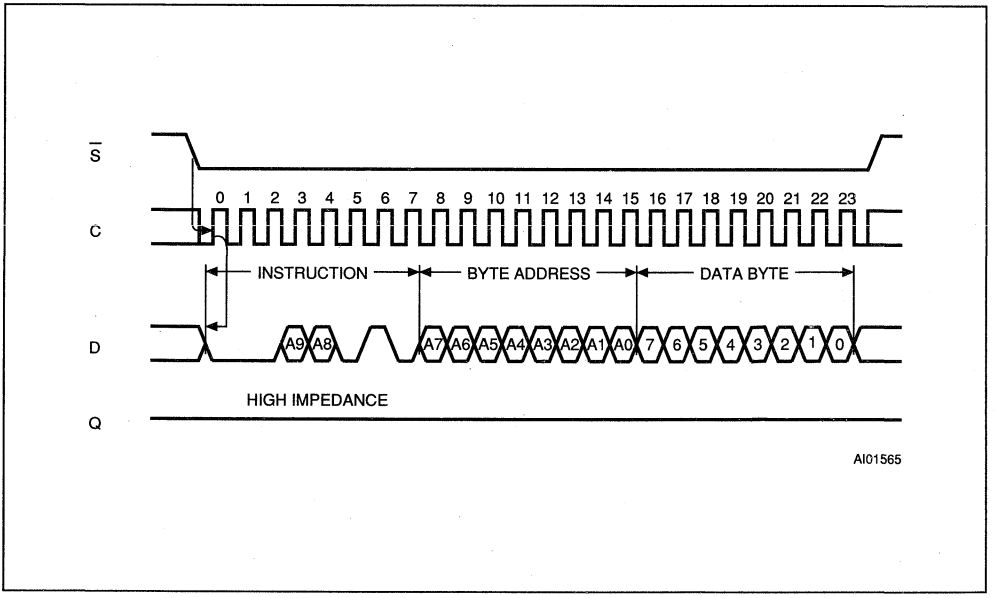


Figure 9. Page Write Operation Sequence

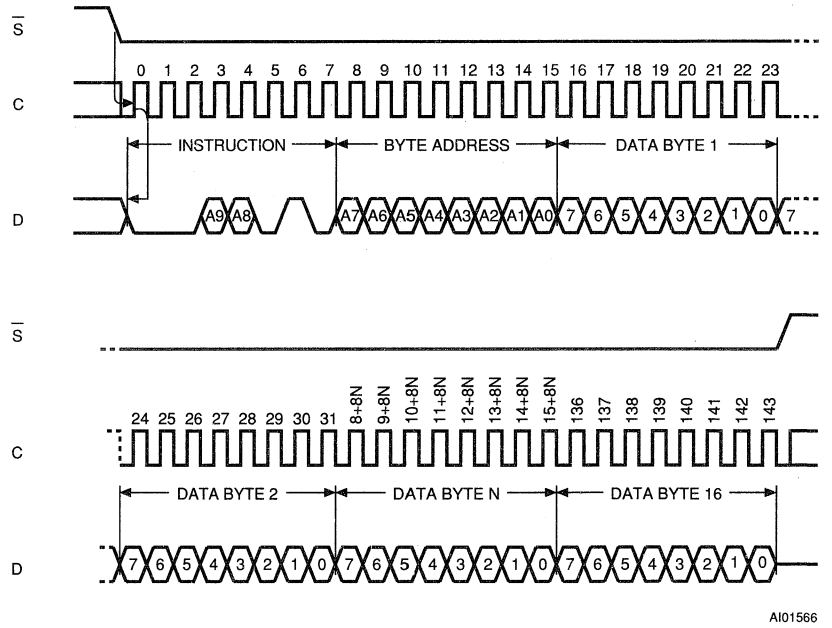


Figure 10. RDSR: Read Status Register Sequence

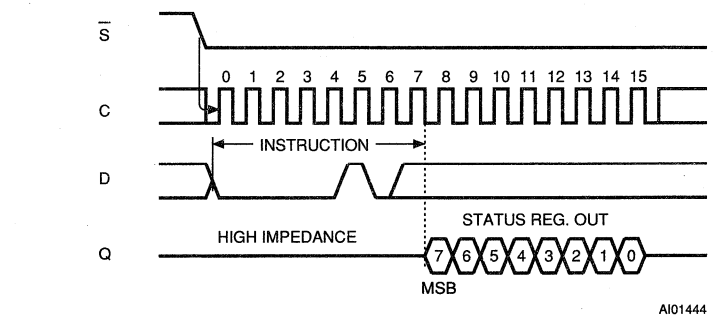
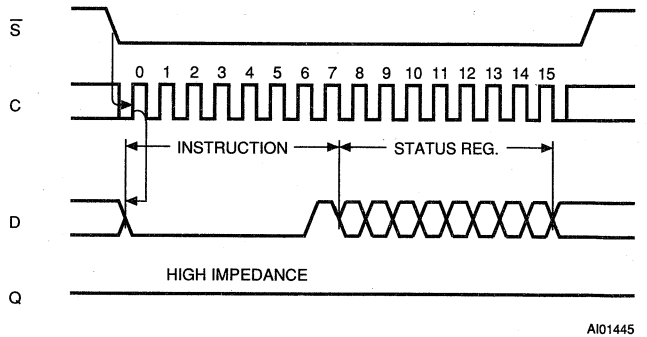


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95080 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remains low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

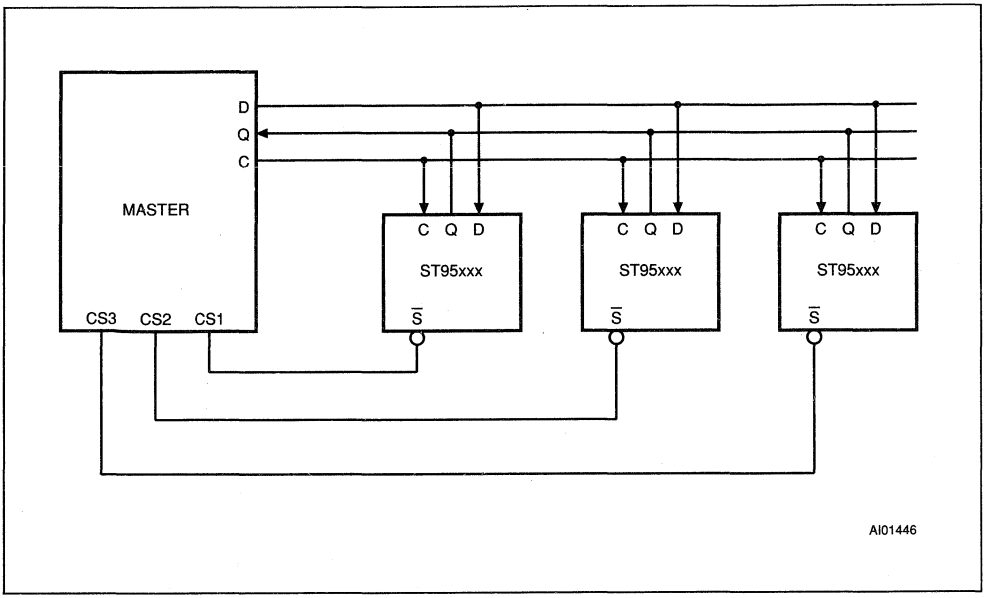
A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur just after the eigth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95080 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

Figure 12. EEPROM and SPI Bus



DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register), i.e. the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Waveforms

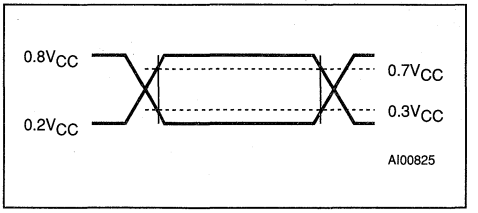


Table 5. Input Parameters (1) (T_A = 25 °C, f = 2 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = 2mA	V_{CC} –0.6		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.

Table 7. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time		100		ns
t_{CHSL}		$\overline{S}$ Active after Rising Edge of C		100		ns
t_{CH}	t_{WH}	Clock High Time		200		ns
t_{CL}	t_{WL}	Clock Low Time		300		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HHCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active		100		ns
t_{CLHL}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ Inactive		100		ns
t_{CHSH}		$\overline{S}$ not Active after Rising Edge of C		200		ns
t_{SHCH}		$\overline{S}$ not Active before next C Pulse		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			200	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			200	ns

Figure 14. Serial Input Timing

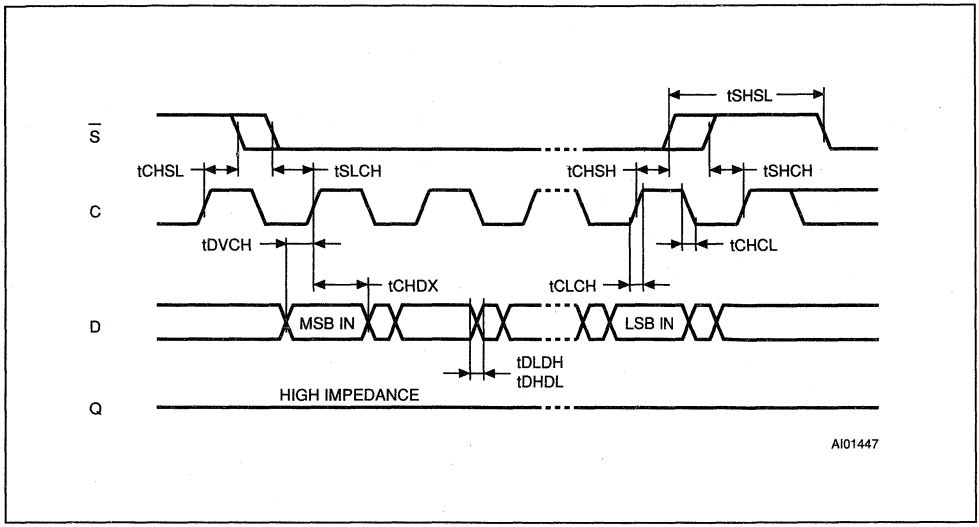


Figure 15. Hold Timing

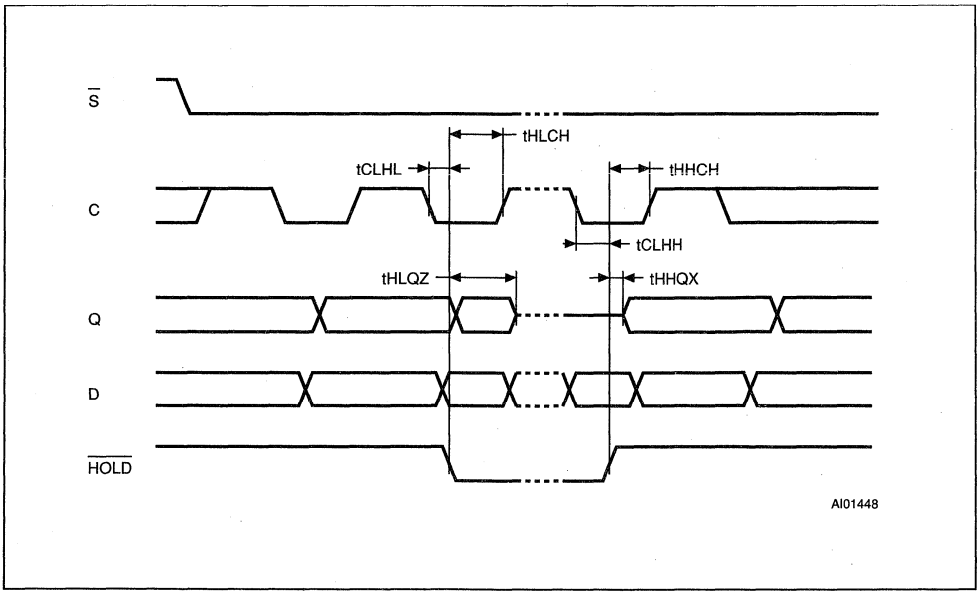
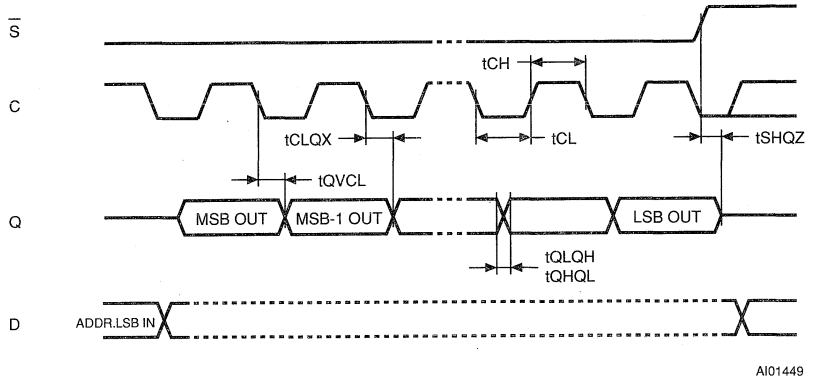
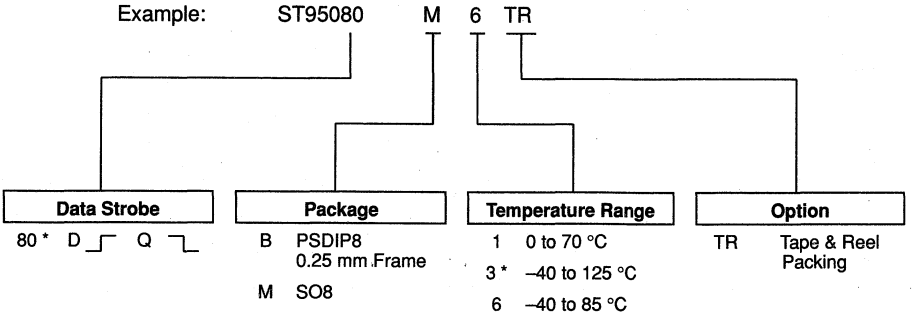


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



Notes: 80 * Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.
3 * Temperature range on special request only.

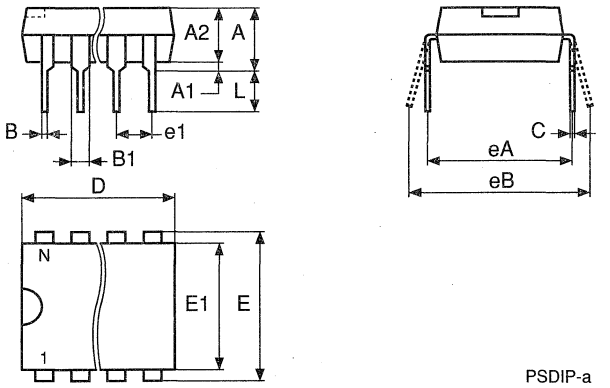
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8



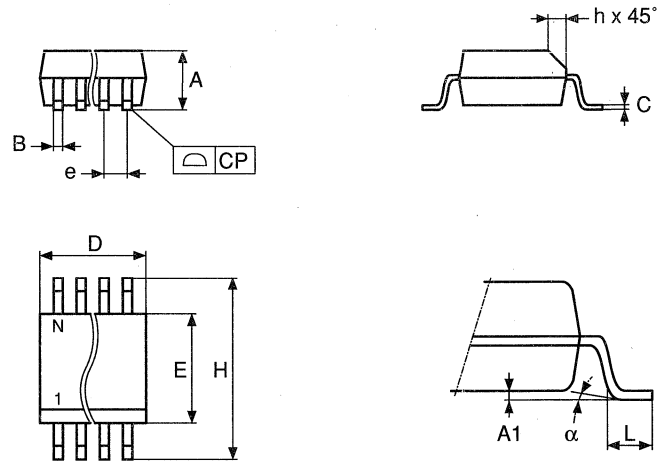
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



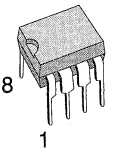
SO-a

Drawing is out of scale

SERIAL ACCESS SPI BUS 8K (1K x 8) EEPROM

PRODUCT PREVIEW

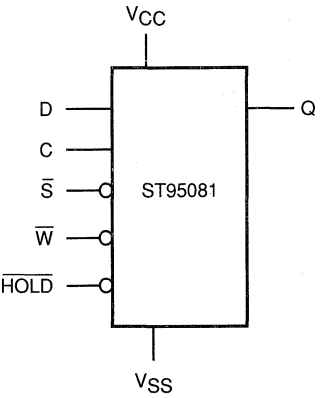
- 1 MILLION ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED 10ms (max) PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS NEGATIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST95081 is an 8K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

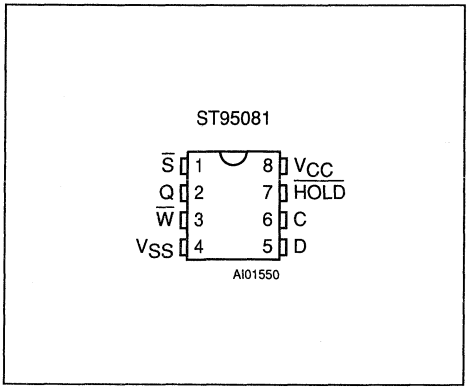


Figure 2B. SO Pin Connections

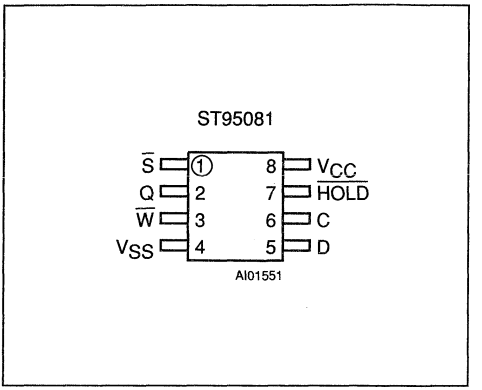


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data are clocked in during the high to low transition of clock C, data are clocked out during the low to high transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out. Data is shifted out on the rising edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the falling edge of the serial clock.

Figure 3. Data and Clock Timing

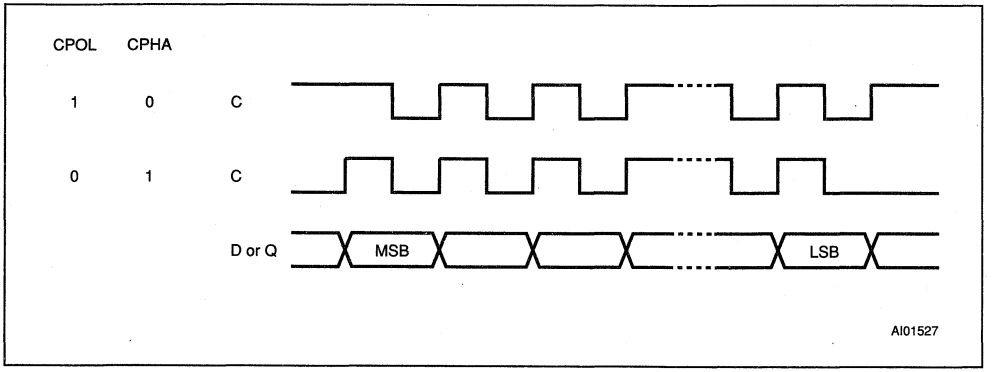
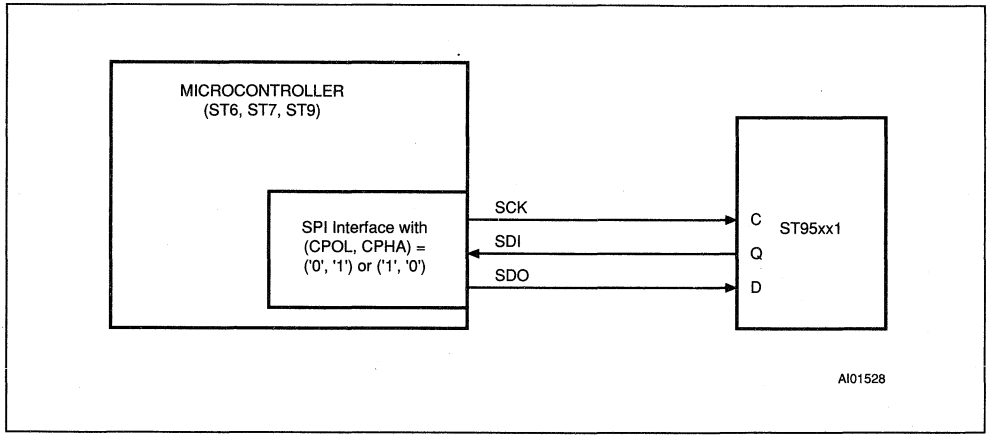


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the falling edge of the clock input, while data on the Q pin changes after the rising edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the ST95081 is deselected and the D output pin is at high impedance and unless an internal write operation is underway the S95081 will be in the standby power mode. $\overline{S}$ low enables the ST95081, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95081 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The ST95081 can be driven by a microcontroller with its SPI peripheral running in either two of the following modes: (CPOL, CPHA) = ('1', '0') or (CPOL, CPHA) = ('0', '1').

For these two modes, input data are latched in by the high to low transition of clock C, and output data are available from the low to high transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 1) and (CPOL, CPHA) = (1, 0) is the stand-by polarity: C remains to '0' for (CPOL, CPHA) = (0, 1) and C remains to 1 for (CPOL, CPHA) = (1, 0) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first falling edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the falling edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95081 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95081, the circuit executes the instruction and enters a wait mode until it is deselected.

Table 3. Write Protected Block Size

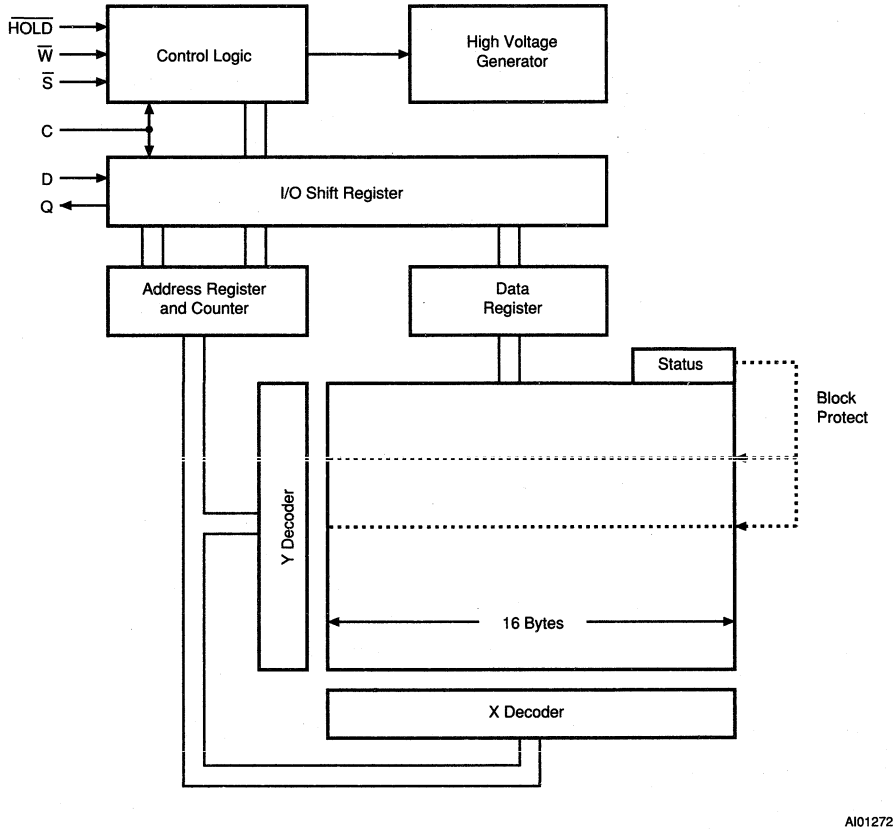
Status Register Bits		Array Addresses Protected	Protected Block
BP1	BP0		
0	0	none	none
0	1	300h - 3FFh	Upper quart
1	0	200h - 3FFh	Upper half
1	1	000h - 3FFh	Whole memory

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	000X X110
WRDI	Reset Write Enable Latch	000X X100
RDSR	Read Status Register	000X X101
WRSR	Write Status Register	000X X001
READ	Read Data from Memory Array	000A A011
WRITE	Write Data to Memory Array	000A A010

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

Figure 5. Block Diagram



Read Status Register (RDSR)

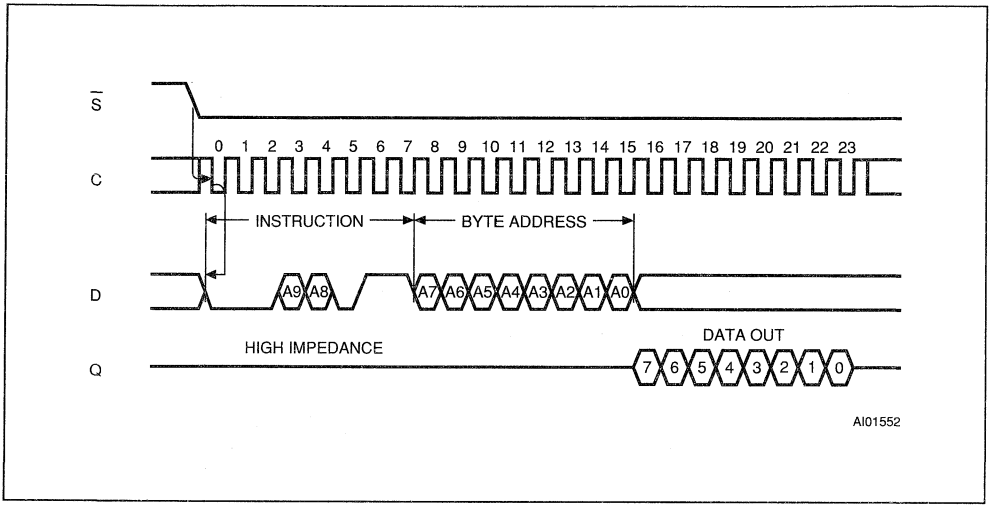
The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95081 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

Figure 6. Read Operation Sequence



OPERATIONS (cont'd)

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95081 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95081 is divided into four 2048 bit blocks. The user may read the blocks but will be unable to write within the selected blocks. The blocks and respective WRSR control bits are shown in Table 3.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the falling edge of the clock (C). Bit 4 of the read instruction contain address bit A8 (most significant address bit). Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the rising edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

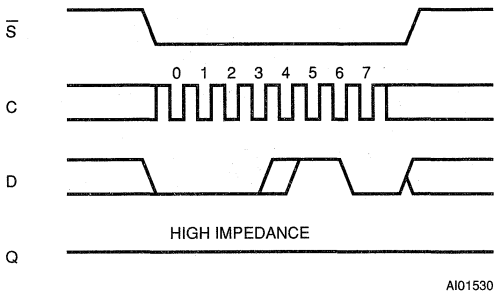


Figure 8. Write Operation Sequence

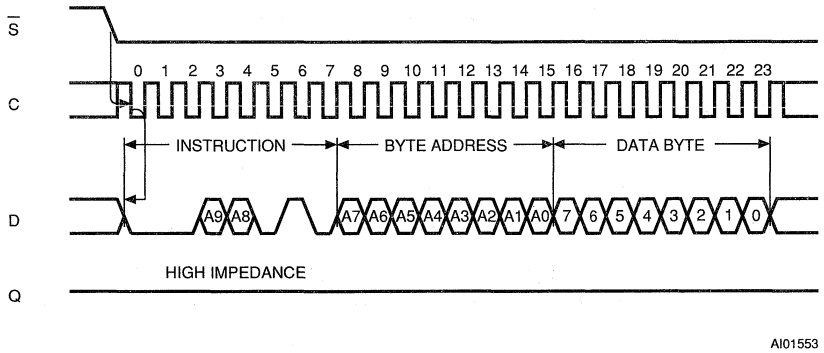


Figure 9. Page Write Operation Sequence

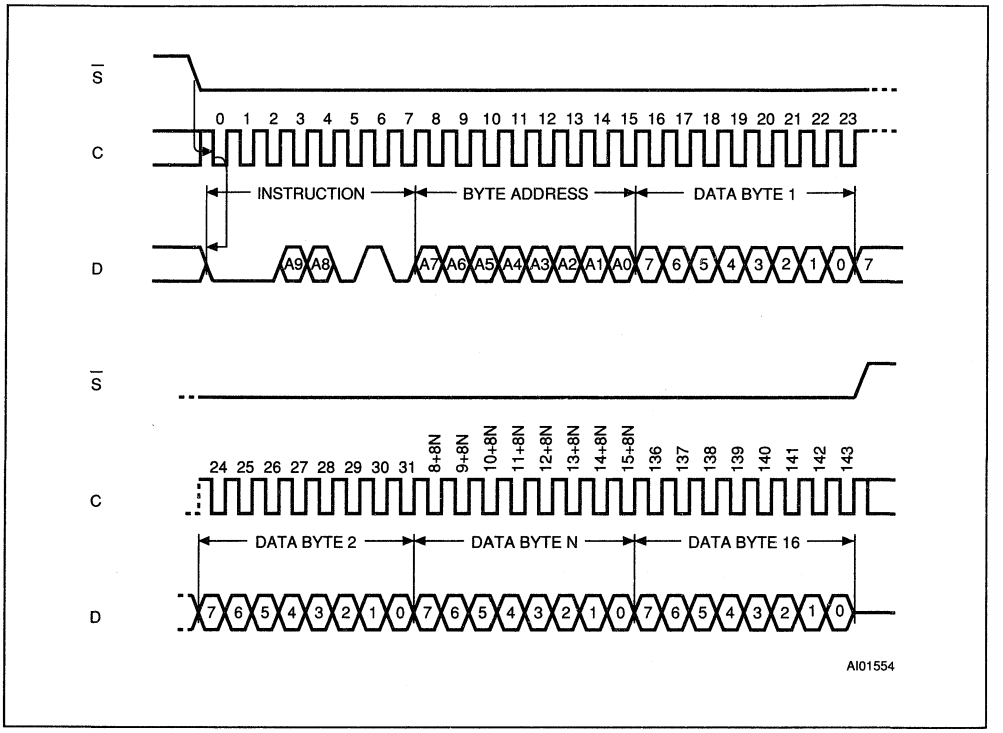


Figure 10. RDSR: Read Status Register Sequence

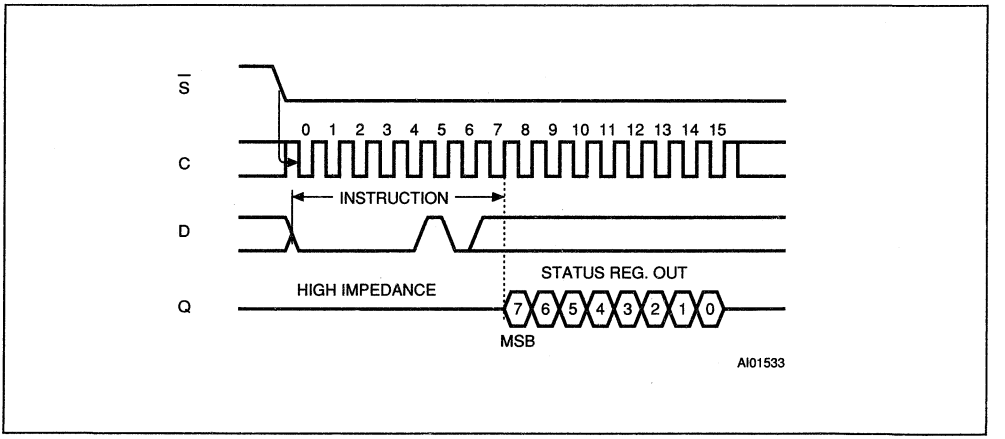
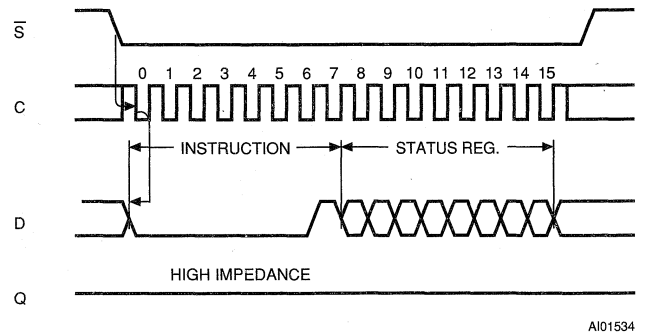


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95081 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remains low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

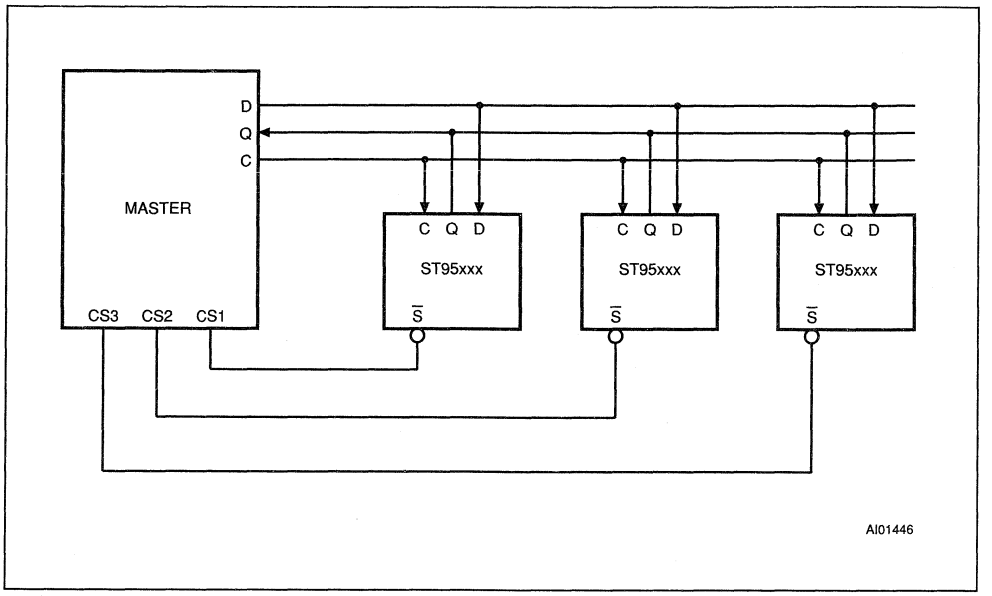
A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur just after the eigth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95081 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

Figure 12. EEPROM and SPI Bus



DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register), i.e. the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Waveforms

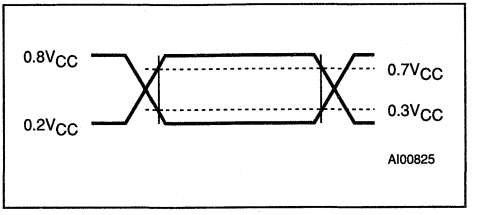


Table 5. Input Parameters (1) (T_A = 25 °C, f = 2 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = 2mA	V_{CC} –0.6		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.

Table 7. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCL}	t_{CSS}	$\overline{S}$ Active Setup Time		100		ns
t_{CLSL}		$\overline{S}$ Active after Falling Edge of C		100		ns
t_{CH}	t_{WH}	Clock High Time		300		ns
t_{CL}	t_{WL}	Clock Low Time		200		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CLDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HHCL}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{HLCL}		Clock High Hold Time after $\overline{HOLD}$ Active		100		ns
t_{CHHL}	t_{HH}	$\overline{HOLD}$ Hold Time		100		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ Inactive		100		ns
t_{CLSH}		$\overline{S}$ not Active after Falling Edge of C		200		ns
t_{SHCL}		$\overline{S}$ not Active before next C Pulse		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			200	ns
t_{QVCL}	t_V	Output Valid from Clock Low			300	ns
t_{CHQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			200	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			200	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data are available.

Figure 14. Serial Input Timing

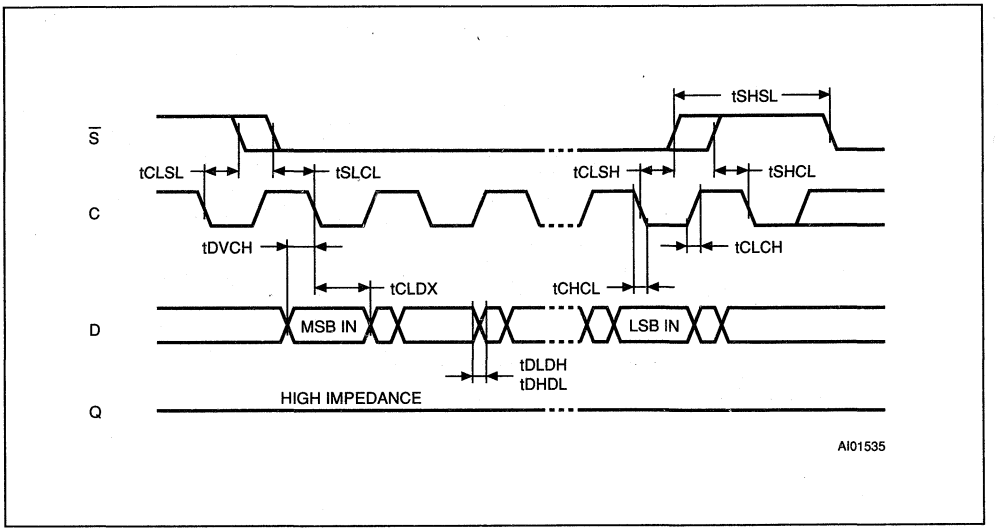


Figure 15. Hold Timing

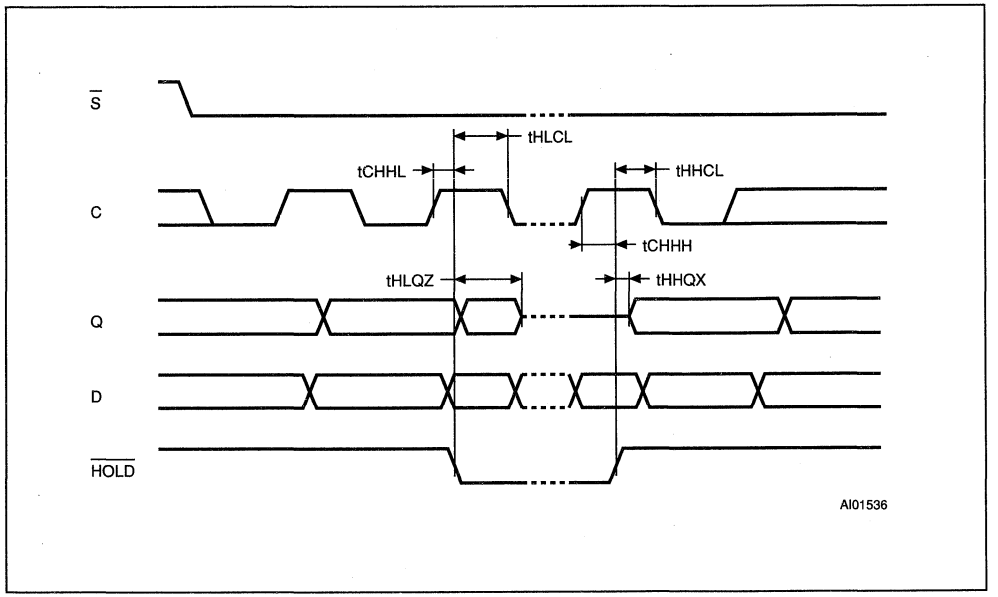
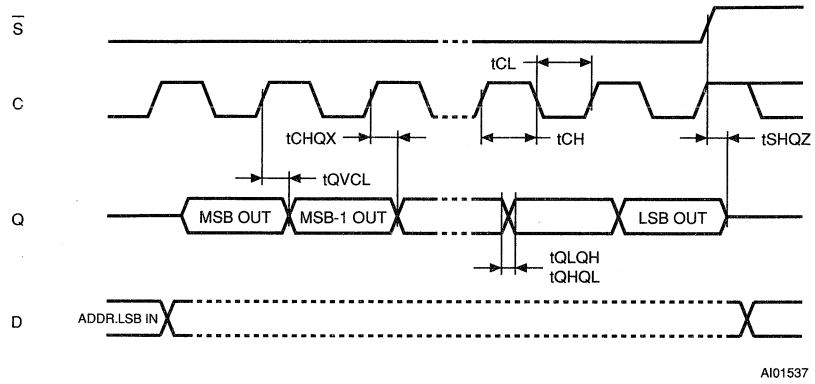
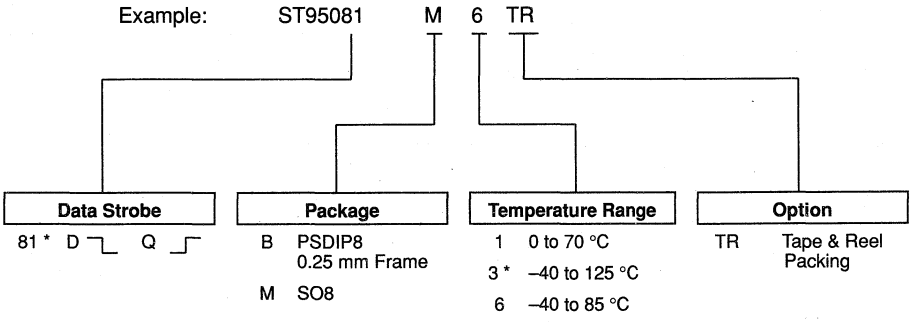


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



Notes: 81 * Data In strobed on falling edge of the clock (C) and Data Out synchronized from the rising edge of the clock.
3 * Temperature range on special request only.

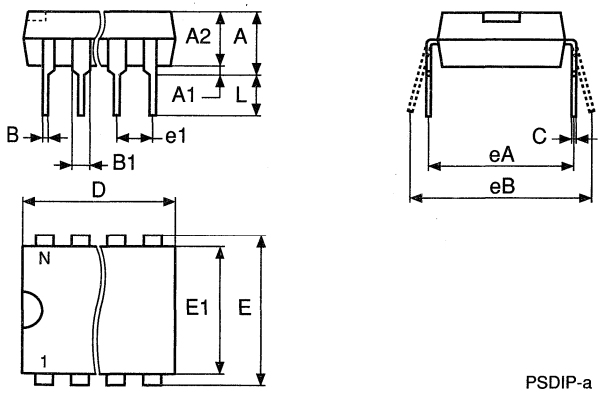
For a list of available options (Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	
CP			0.10			0.004

PSDIP8



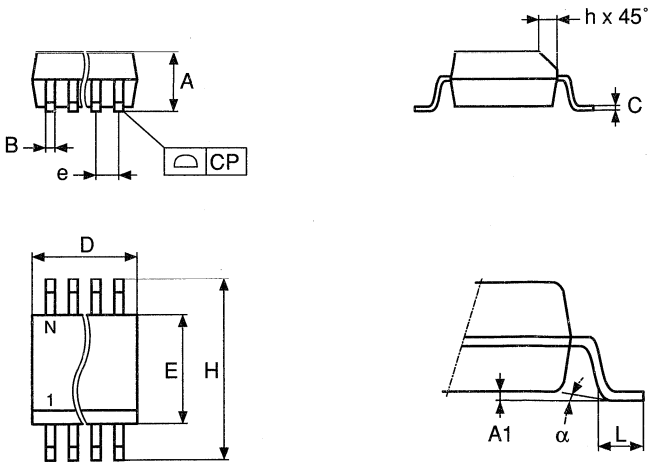
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



SO-a

Drawing is out of scale

PARALLEL EEPROM

PARALLEL ACCESS 16K (2K x 8) EEPROM

PRODUCT PREVIEW

- FAST ACCESS TIME: 70ns
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle: 2ms Max
- ENHANCED END OF WRITE DETECTION:
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP
- SOFTWARE DATA PROTECTION

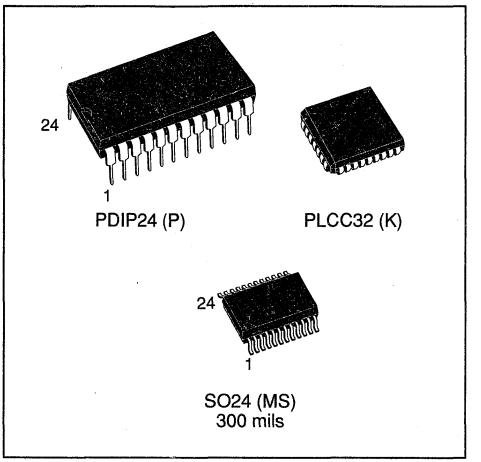
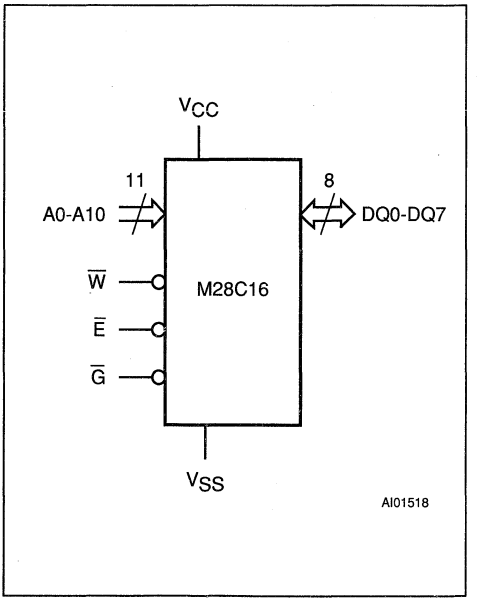


Figure 1. Logic Diagram



DESCRIPTION

The M28C16 is a 2K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time (70ns) with low power dissipation and requires a 5V power supply.

Table 1. Signal Names

A0 - A10	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

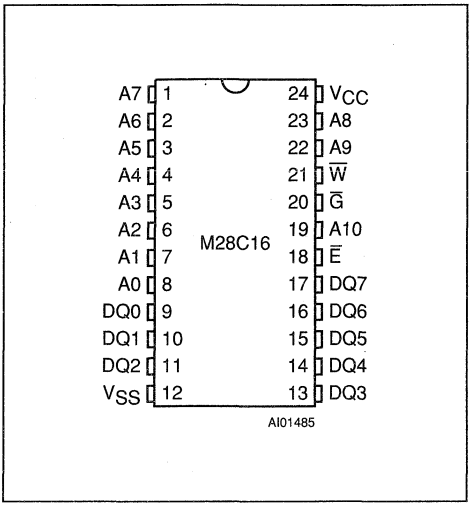
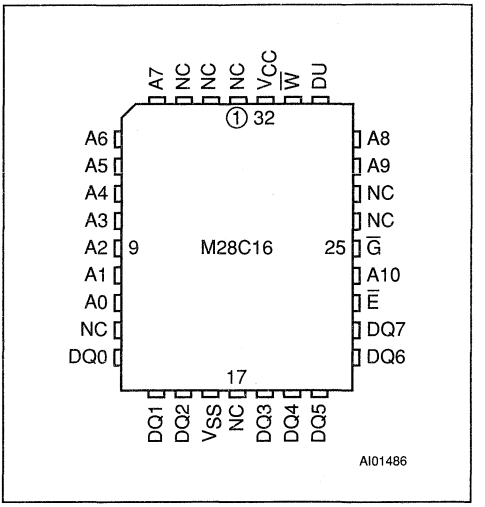
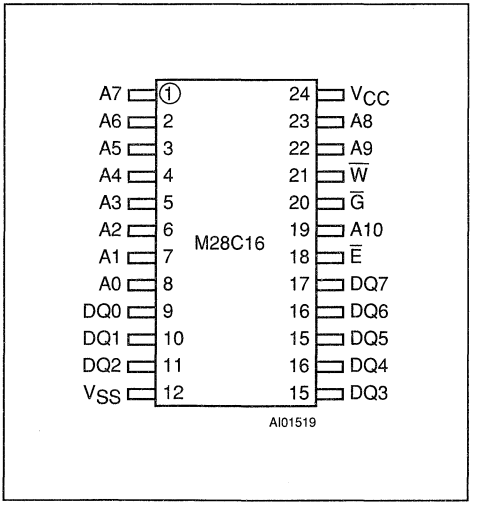


Figure 2B. LCC Pin Connections



Warning: NC = No Connections, DU = Don't Use

Figure 2C. SO Pin Connections



DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Data Polling and Toggle Bit. The M28C16 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRITPION

Addresses (A0-A10). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C16 through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C16.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 3 grade 6	0 to 70 – 40 to 125 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z
Chip Erase	V_{IL}	V_{IH} (2)	V_{IL}	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}
2. V_{IH} = 12V ± 5%

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28C16 is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

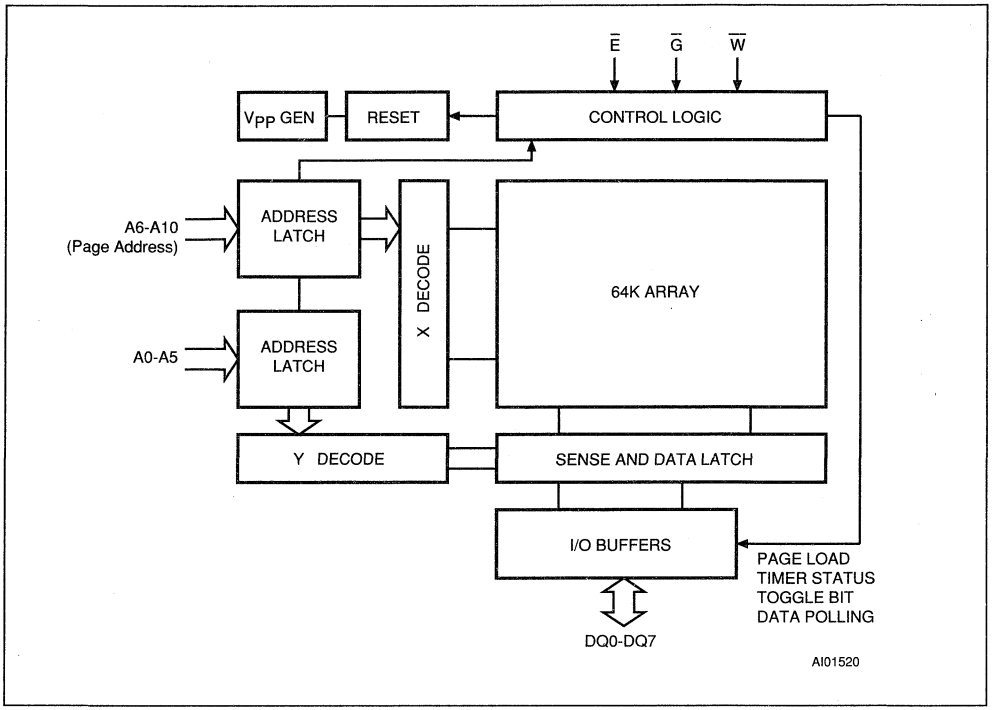
Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28C16 supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 64 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A10 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{WHWH}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within a minimum time (t_{WHWH} max), the internal programming cycle will start.

Figure 3. Block Diagram



Chip Erase

The contents of the entire memory may be erased (FF) by use of the Chip Erase command by setting Chip Enable ($\overline{E}$) Low and Output Enable ($\overline{G}$) to 12V. The chip is cleared when a 10ms low pulse is applied to the Write Enable pin.

Microcontroller Control Interface

The M28C16 provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C16 also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Figure 5. Software Data Protection Enable Algorithm and Memory Write

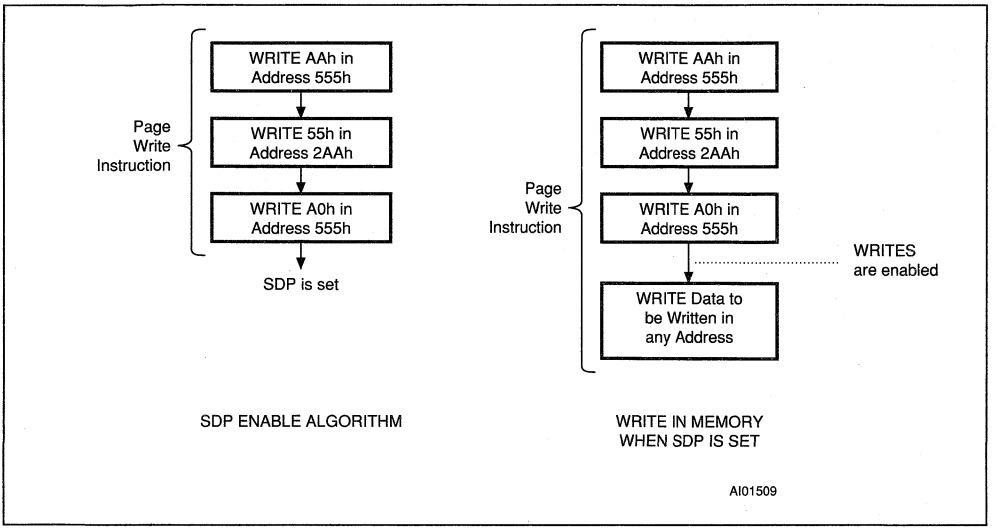
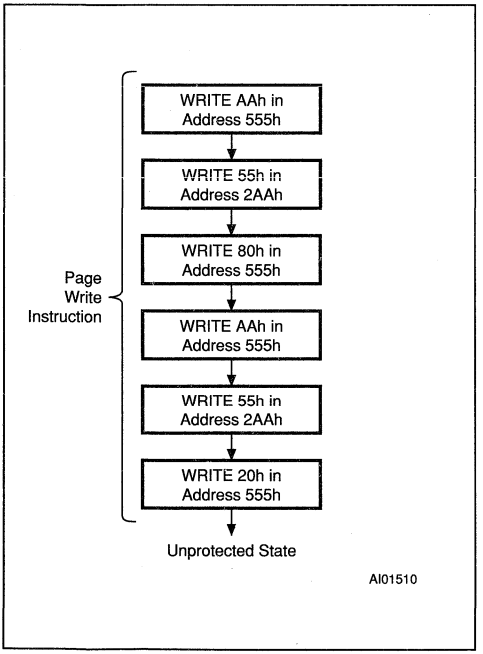


Figure 6. Software Data Protection Disable Algorithm



Software Data Protection

The M28C16 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device including the Chip Erase instruction. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28C16 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents. The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences.

To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write) three specific data bytes to three specific memory locations as per Figure 5. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 6 (with a Page Write). This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

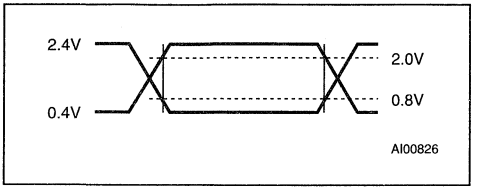


Figure 8. AC Testing Equivalent Load Circuit

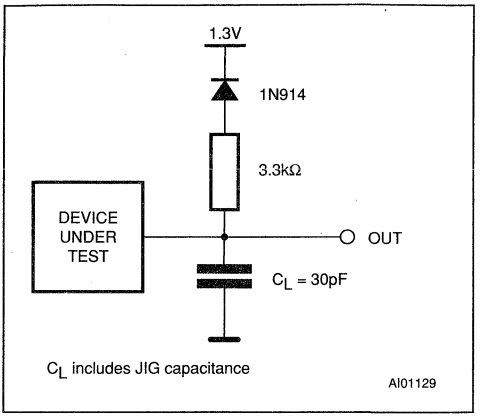


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (TTL inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		30	mA
	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		25	mA
I_{CC1} (1)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

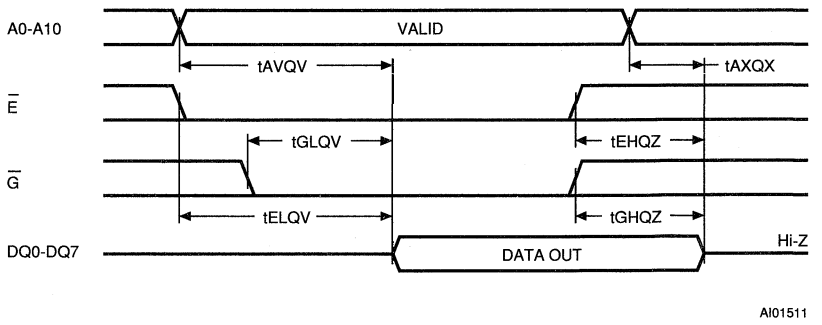
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28C16								Unit
				-70		-90		-120		-150		
				min	max	min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		70		90		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		45		50	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	35	0	40	0	45	0	50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	0	45	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.15	100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			2	ms
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

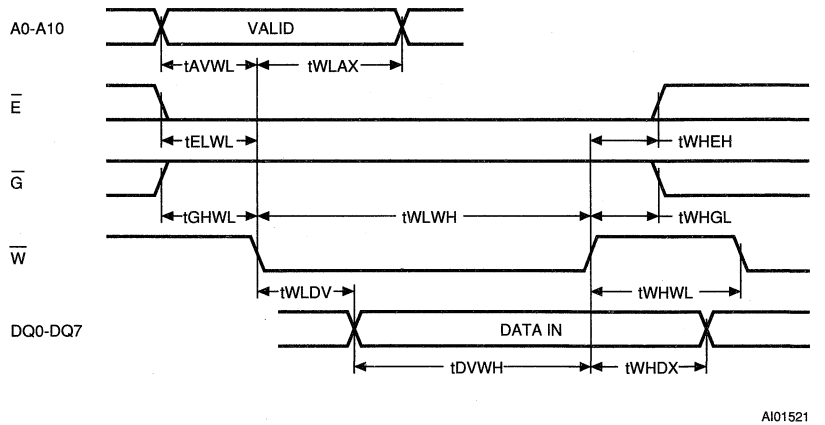


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

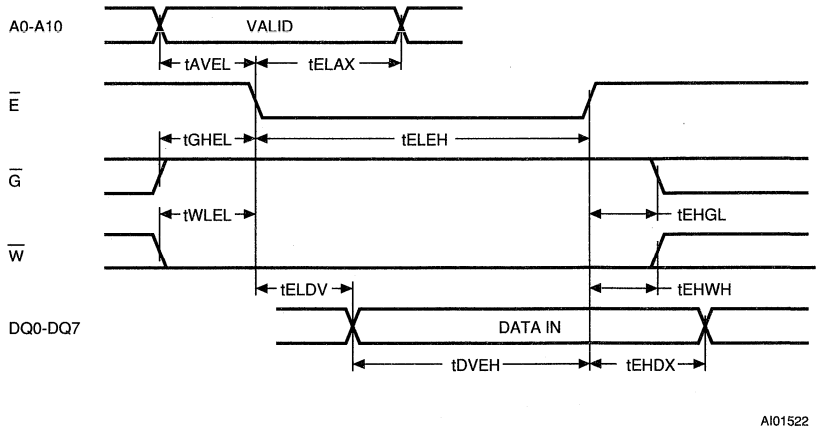


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

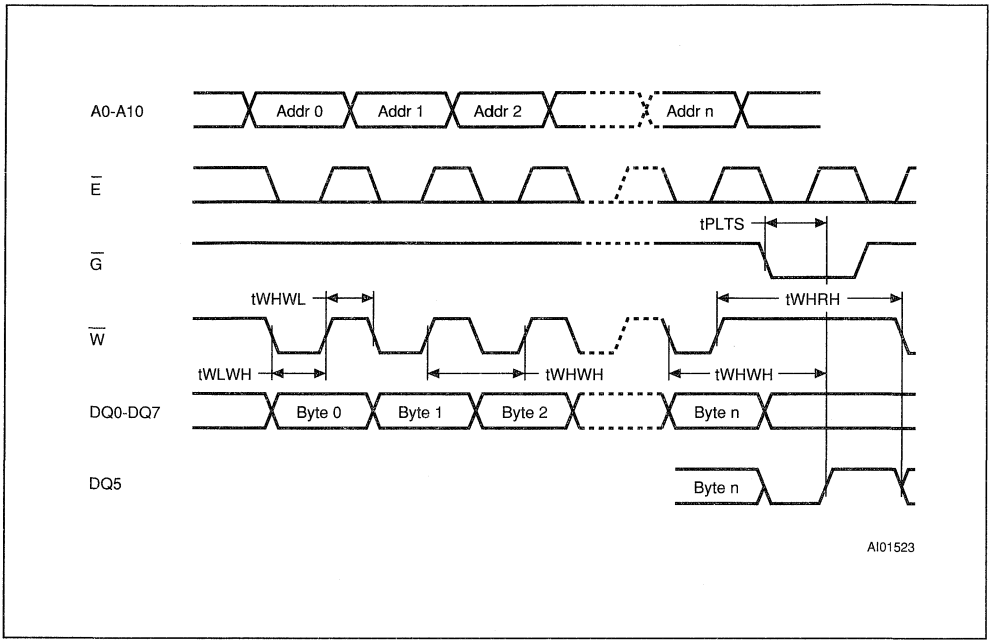
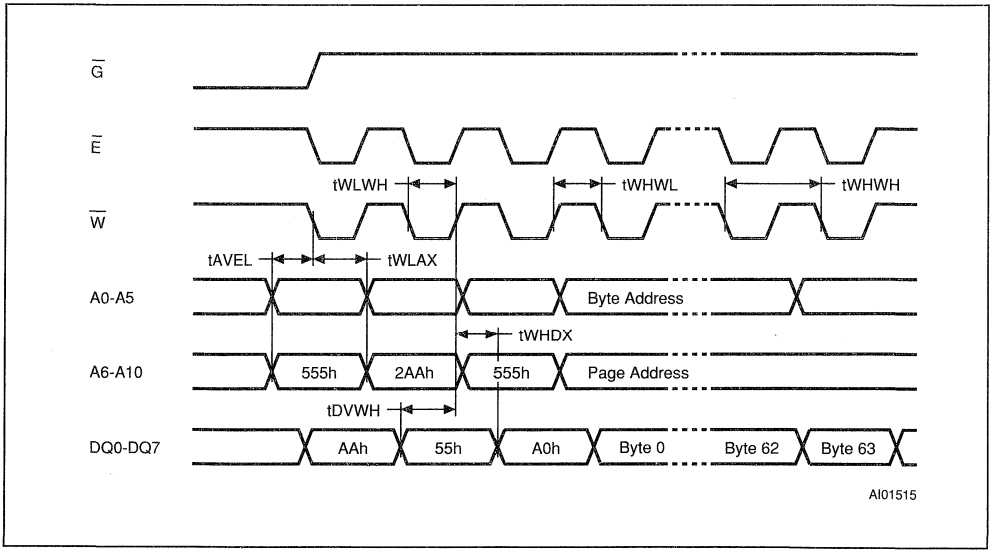


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A10 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Waveforms Sequence

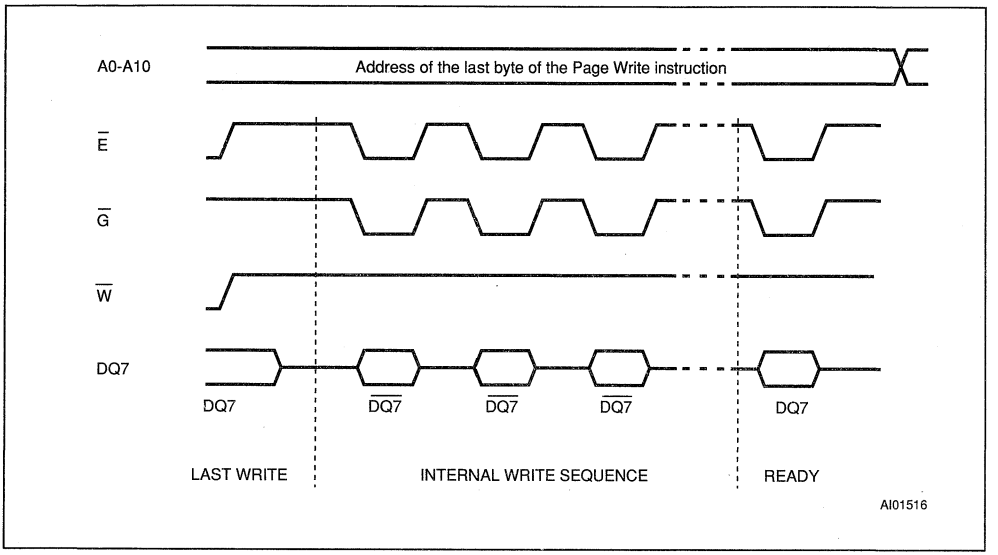
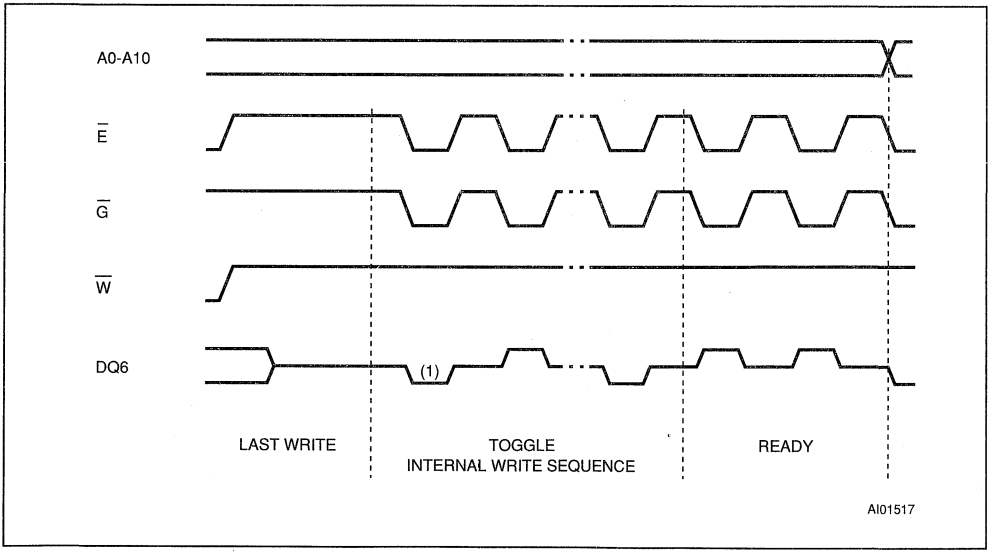


Figure 15. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

Figure 16. Chip Erase Wavforms

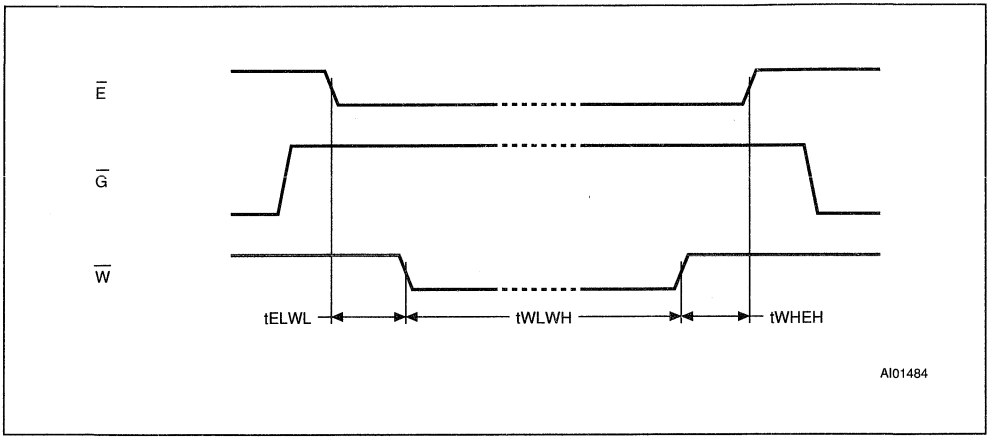


Table 9. Chip Erase AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = 12V	5		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = 12V	5		µs
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{G}$ = 12V	10		ms

ORDERING INFORMATION SCHEME

Example: M28C16 -70 K 1

Speed		Package		Temperature Range	
-70	70ns	P	PDIP24	1	0 to 70 °C
-90	90ns	K	PLCC32	3 *	–40 to 125 °C
-120	120ns	MS	SO24 300mils	6	–40 to 85 °C
-150	150ns				

Note: 3 * Temperature range on special request only.

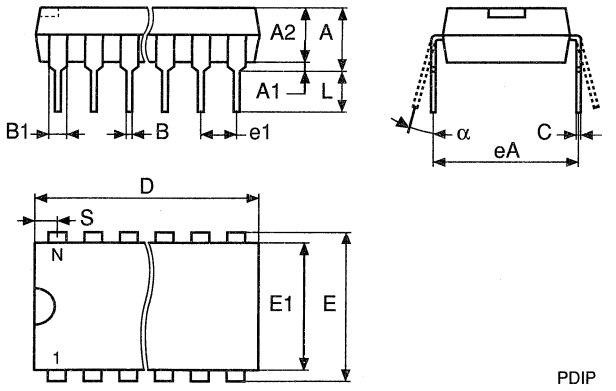
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP24 - 24 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D			32.26			1.270
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	24			24		

PDIP24



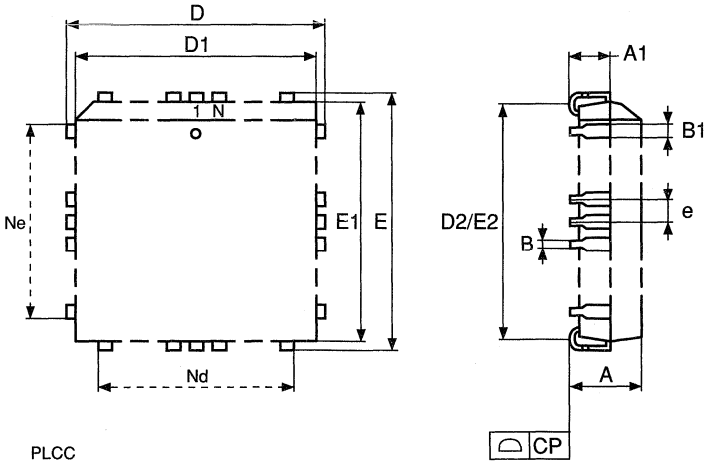
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

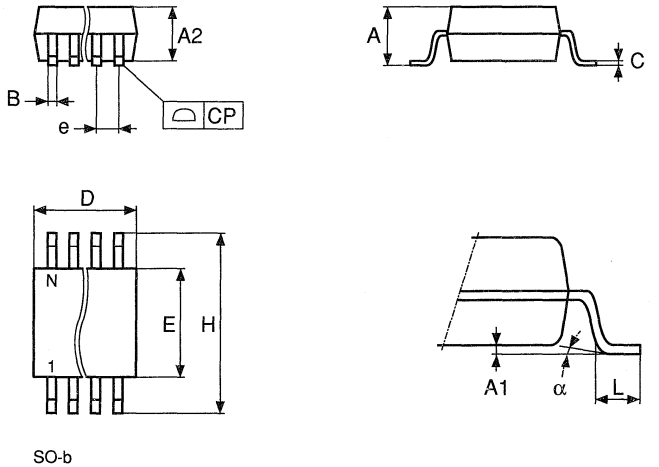


Drawing is out of scale

SO24 - 24 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		15.20	15.60		0.598	0.614
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	24			24		
CP			0.10			0.004

SO24



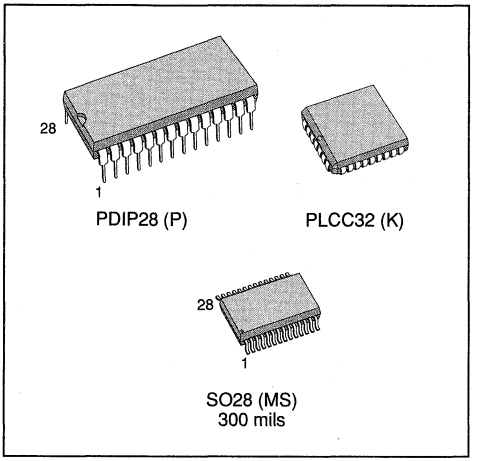
SO-b

Drawing is out of scale

LOW VOLTAGE PARALLEL ACCESS 16K (2K x 8) EEPROM

PRODUCT PREVIEW

- FAST ACCESS TIME: 150ns
- SINGLE 3V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION:
  - Active Current 8mA
  - Standby Current 50µA
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle: 3ms Max
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- SOFTWARE DATA PROTECTION



DESCRIPTION

The M28LV17 is a 2K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 3V ± 10% power supply.

The M28LV17 offers the same features than the M28LV16, in addition to the Ready/Busy pin.

Table 1. Signal Names

A0 - A10	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

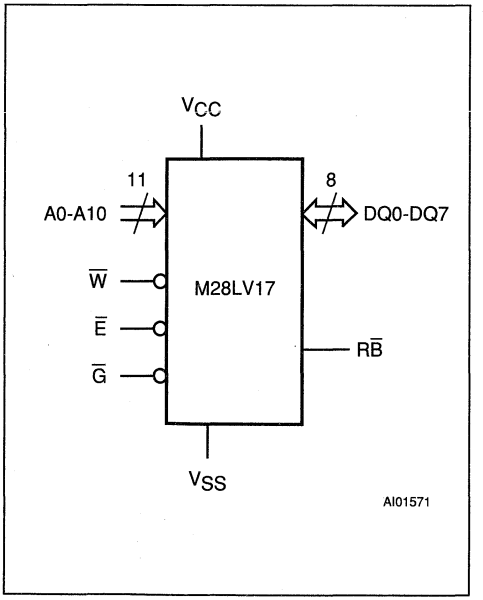
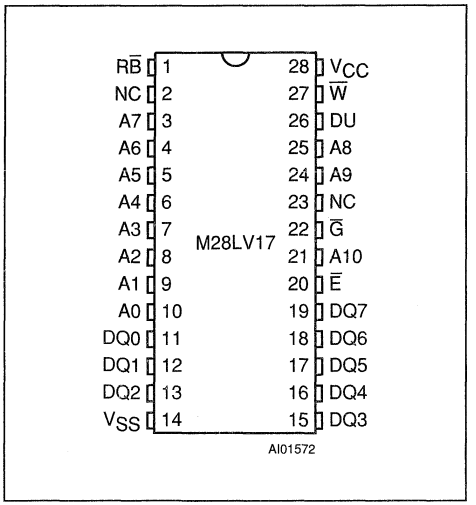
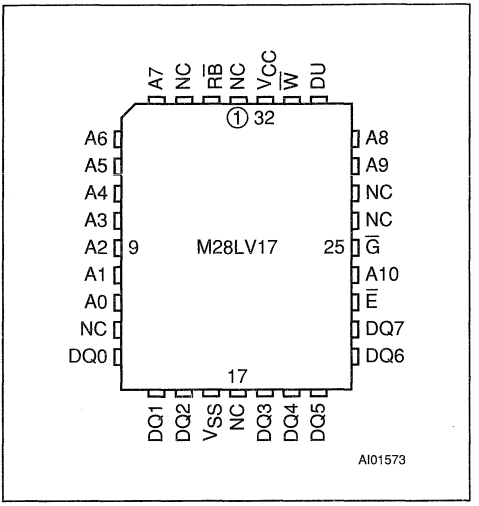


Figure 2A. DIP Pin Connections



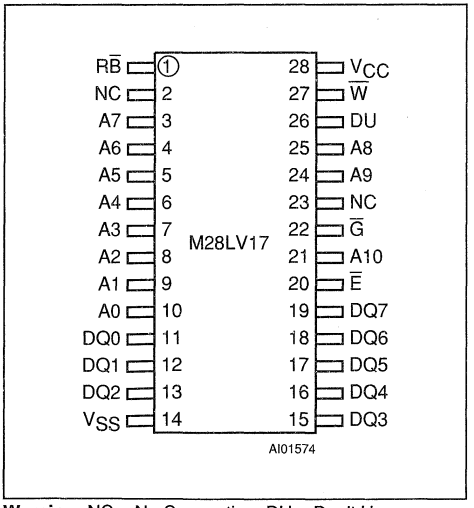
Warning: NC = No Connection, DU = Don't Use

Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use

Figure 2C. SO Pin Connections



Warning: NC = No Connection, DU = Don't Use

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28LV17 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRITPION

Addresses (A0-A10). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28LV17 through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28LV17.

Ready/Busy ($\overline{RB}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 3 grade 6	0 to 70 – 40 to 125 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z
Chip Erase	V_{IL}	V_{IH} (2)	V_{IL}	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}
2. V_{IH} = 12V ± 5%

Read

The M28LV17 is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The M28LV17 supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

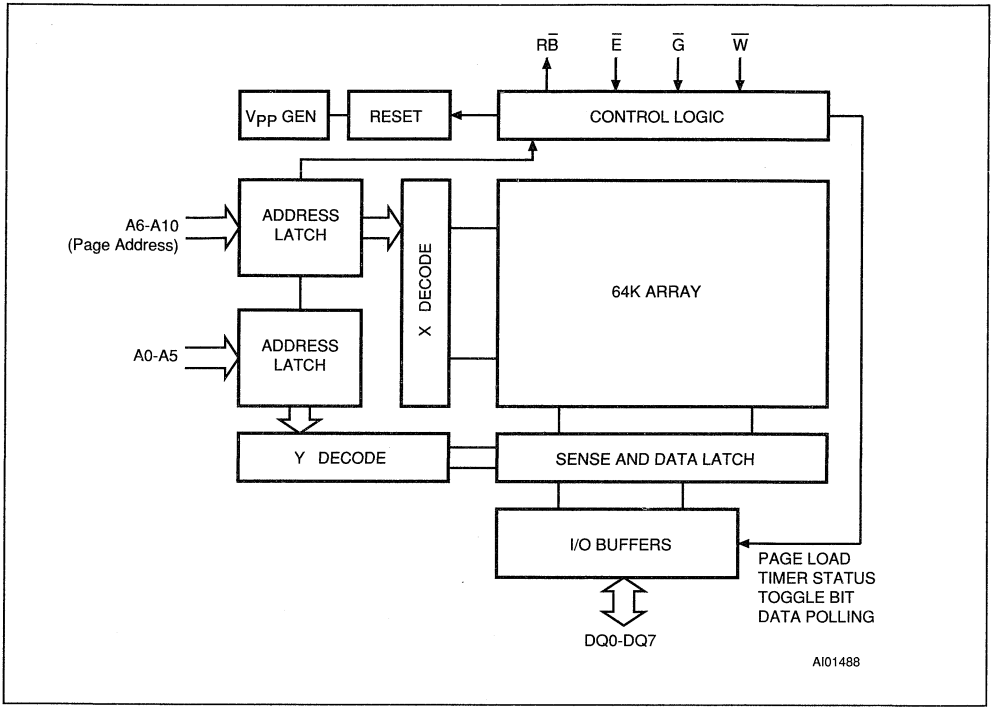
Page write allows up to 64 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A10 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{WHWH}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within a minimum time (t_{WHWH} max), the internal programming cycle will start.

Chip Erase

The contents of the entire memory may be erased (FF) by use of the Chip Erase command by setting Chip Enable ($\overline{E}$) Low and Output Enable ($\overline{G}$) to 12V. The chip is cleared when a 10ms low pulse is applied to the Write Enable pin.

Figure 3. Block Diagram



Microcontroller Control Interface

The M28LV17 provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the RB signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28LV17 also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by E or W. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The RB pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

Figure 5. Software Data Protection Enable Algorithm and Memory Write

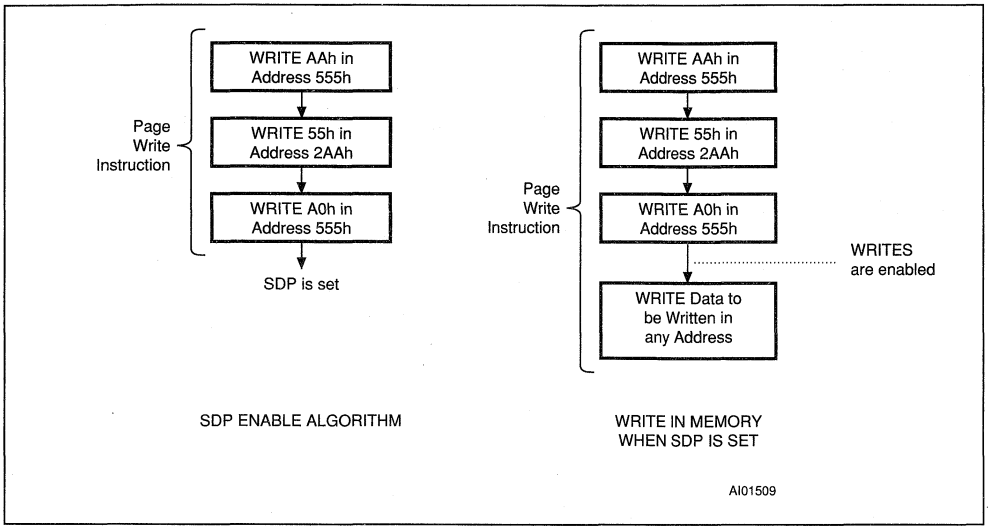
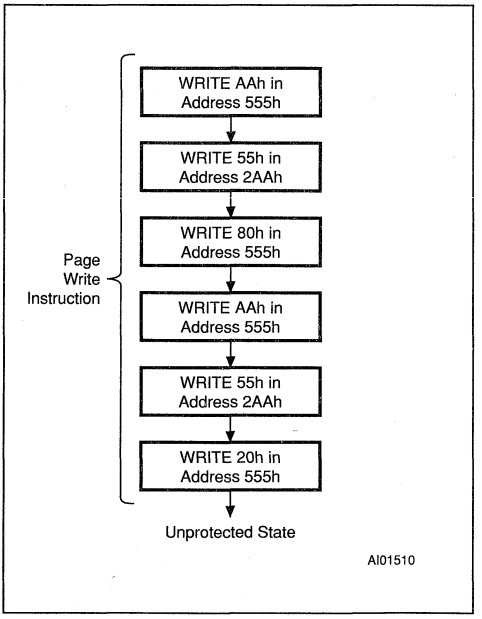


Figure 6. Software Data Protection Disable Algorithm



Software Data Protection

The M28LV17 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device including the Chip Erase instruction. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28LV17 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents. The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences.

To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write) three specific data bytes to three specific memory locations as per Figure 5. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 6 (with a Page Write). This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0V to V_{CC} -0.3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

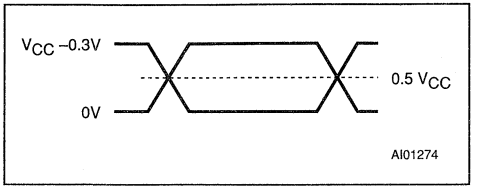


Figure 8. AC Testing Equivalent Load Circuit

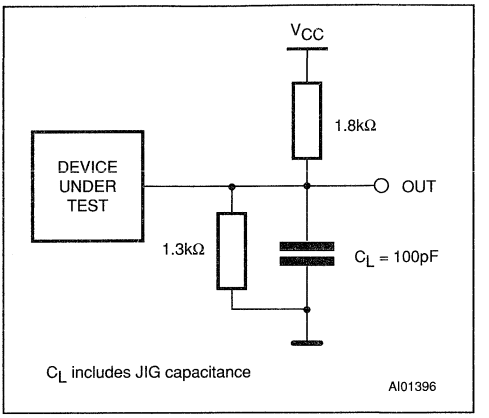


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5 MHz		8	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 1 mA	0.8 V_{CC}		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

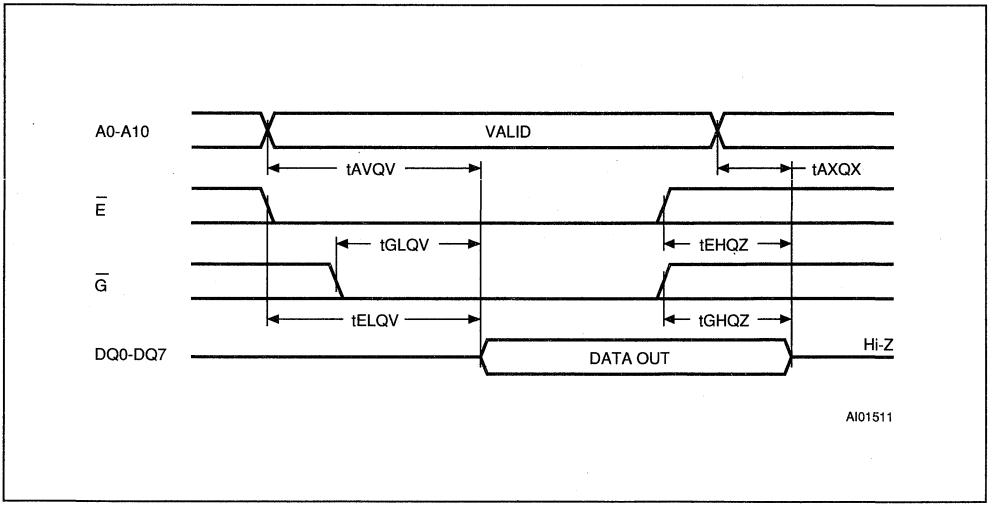
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28LV17						Unit
				-150		-200		-300		
				min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		80		95		150	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	45	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50	1000	ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.15	100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			3	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		50	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

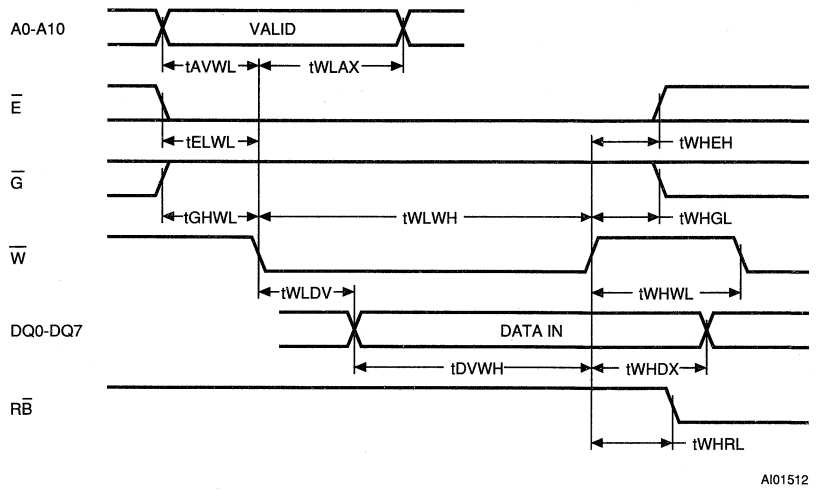


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

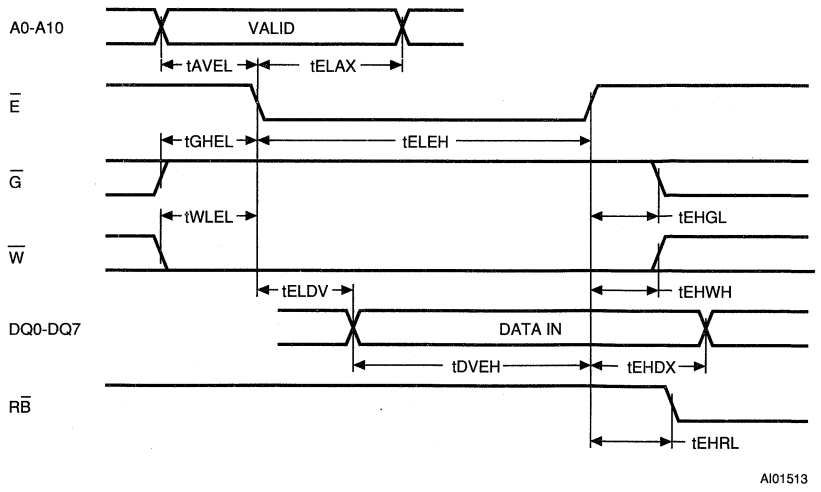


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

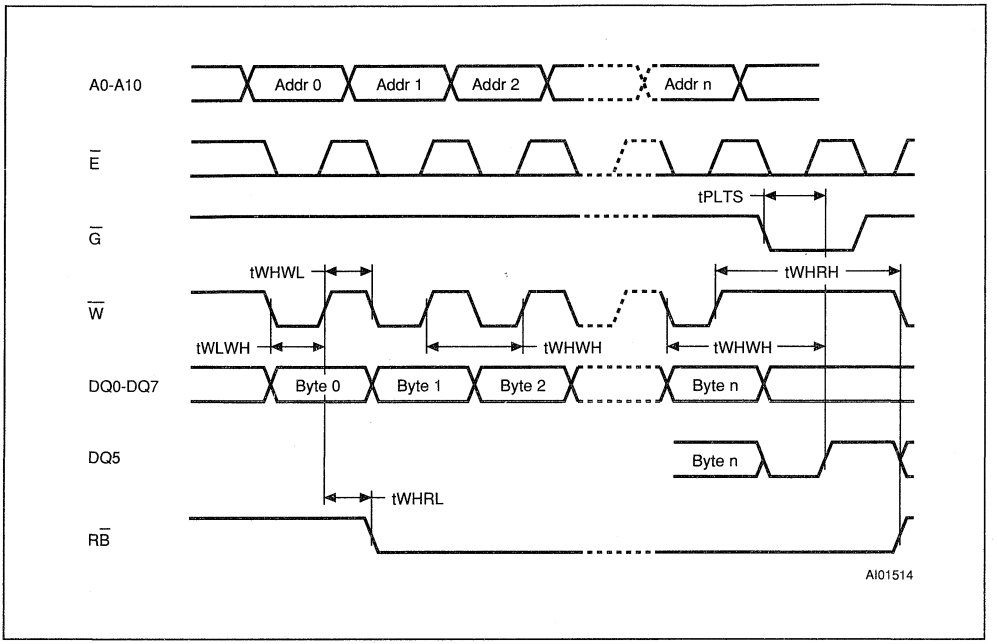
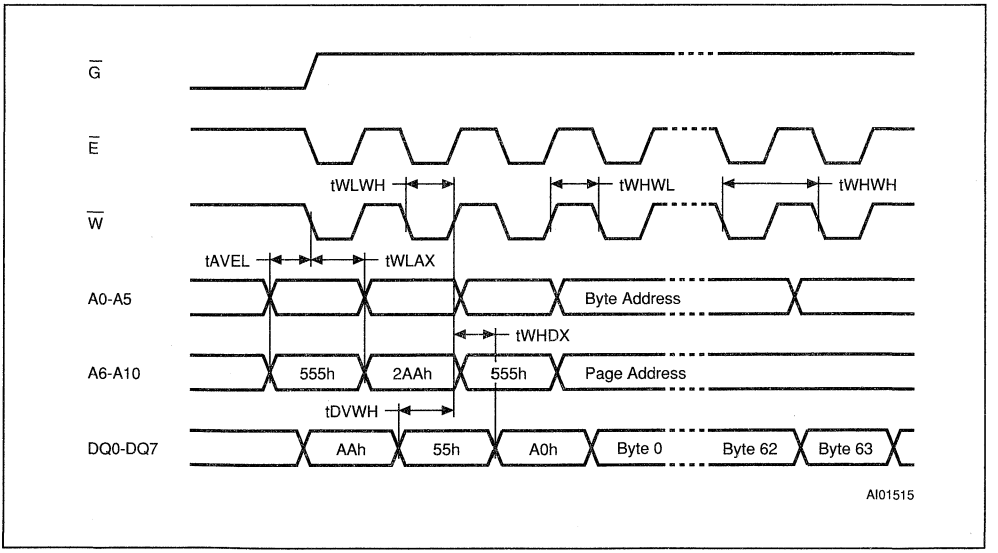


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A10 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Waveforms Sequence

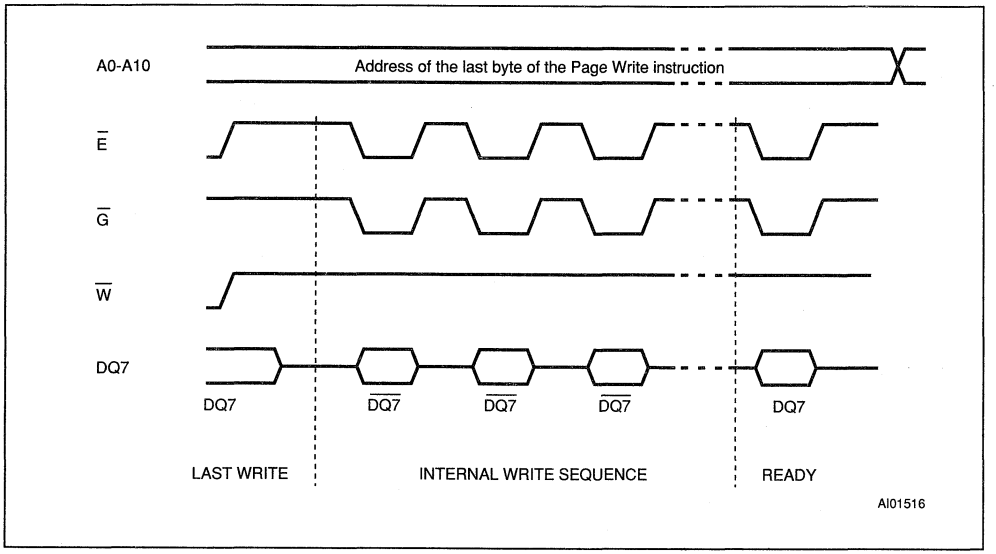
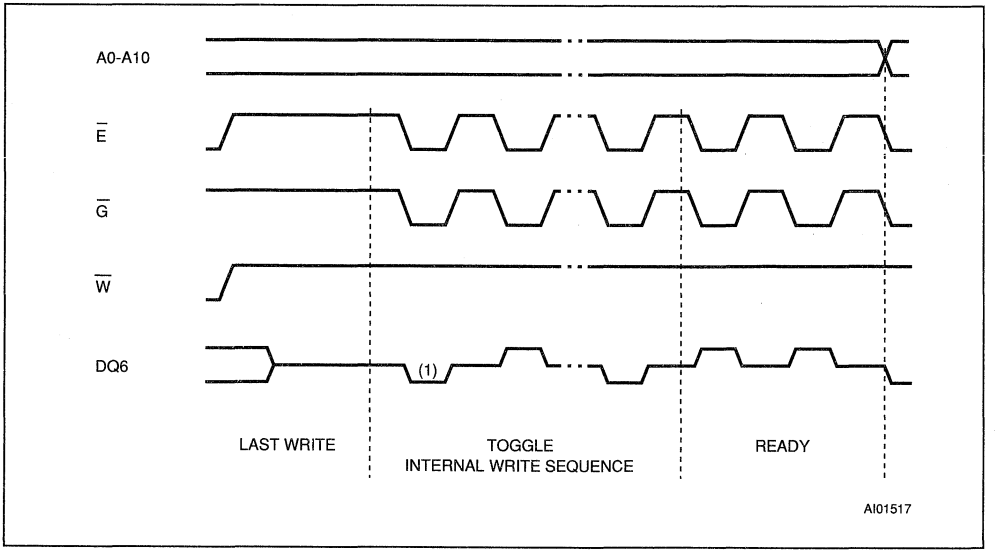


Figure 15. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

Figure 16. Chip Erase Wavforms

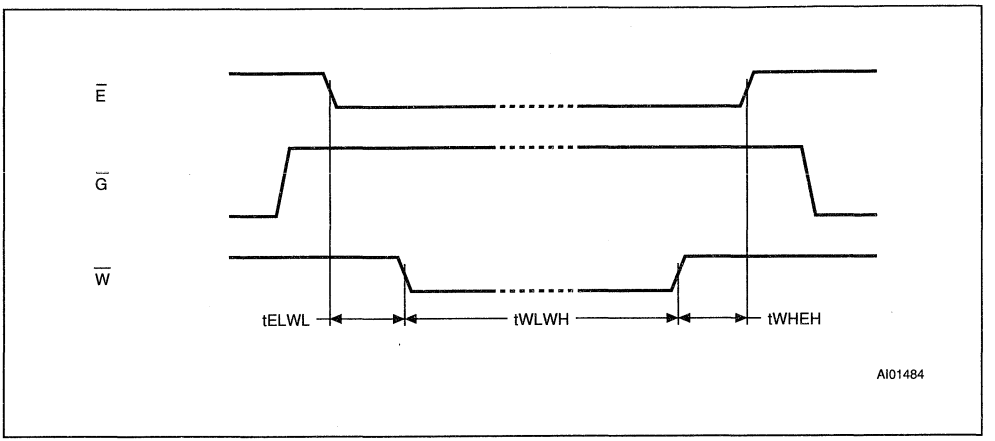


Table 9. Chip Erase AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = 12V	5		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = 12V	5		µs
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{G}$ = 12V	10		ms

ORDERING INFORMATION SCHEME

Example: M28LV17 -200 K 1

Speed		Package		Temperature Range	
-150	150ns	P	PDIP28	1	0 to 70 °C
-200	200ns	K	PLCC32	3 *	–40 to 125 °C
-300	300ns	MS	SO28 300mils	6	–40 to 85 °C

Note: 3 * Temperature range on special request only.

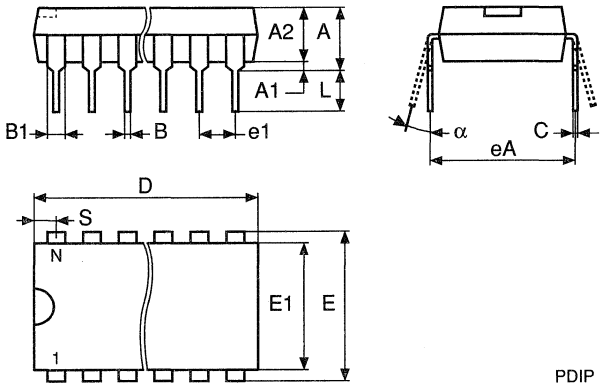
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



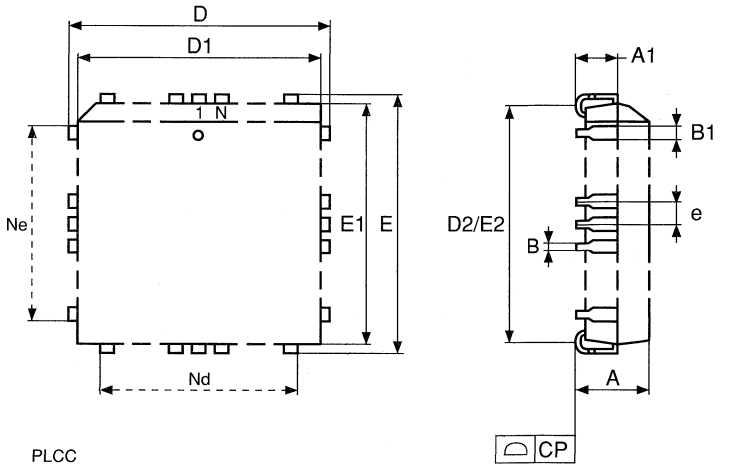
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

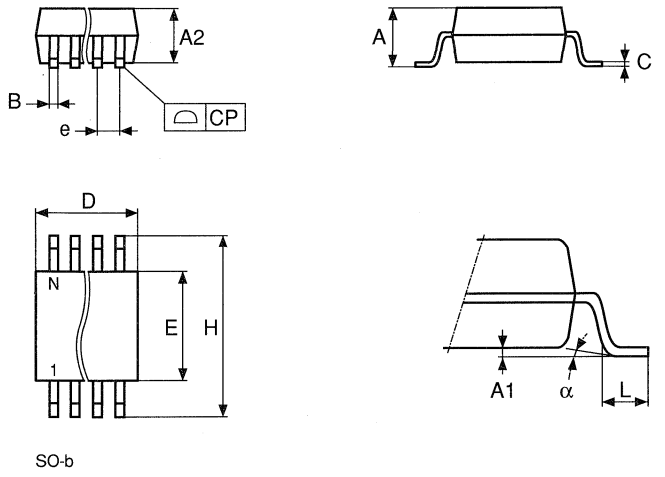


Drawing is out of scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SO28



SO-b

Drawing is out of scale

PARALLEL ACCESS 64K (8K x 8) EEPROM

PRELIMINARY DATA

- FAST ACCESS TIME: 70ns
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle: 2ms Max
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP
- SOFTWARE DATA PROTECTION

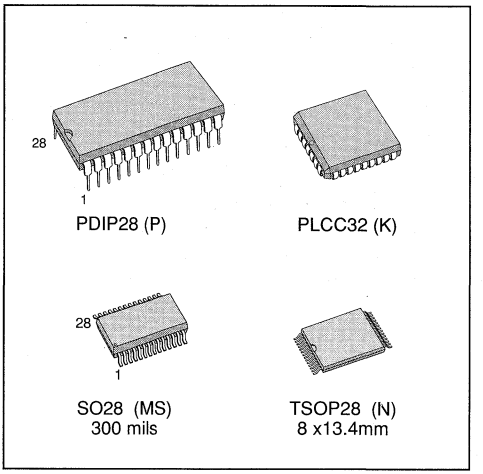
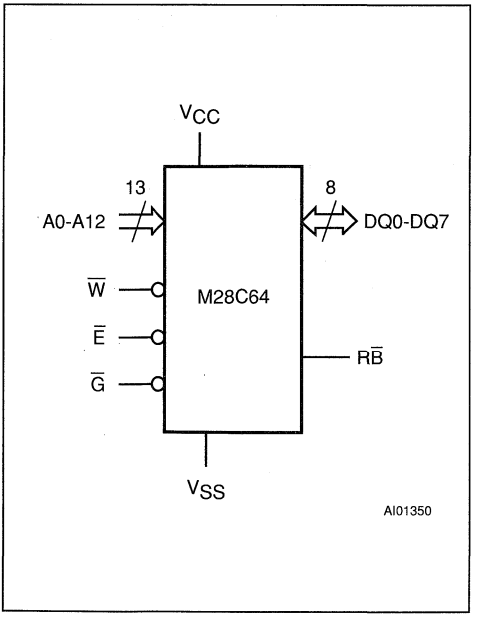


Figure 1. Logic Diagram



DESCRIPTION

The M28C64 is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time (70ns) with low power dissipation and requires a 5V power supply.

Table 1. Signal Names

A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

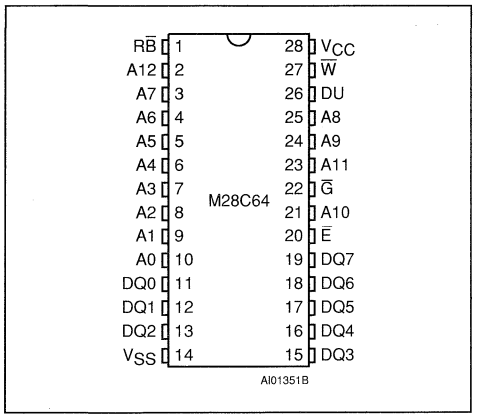
Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 3 grade 6	0 to 70 – 40 to 125 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

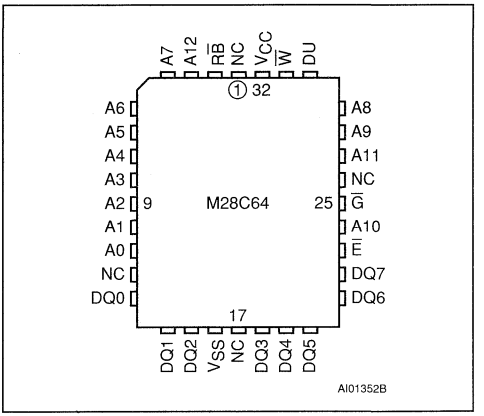
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7

Figure 2A. DIP Pin Connections



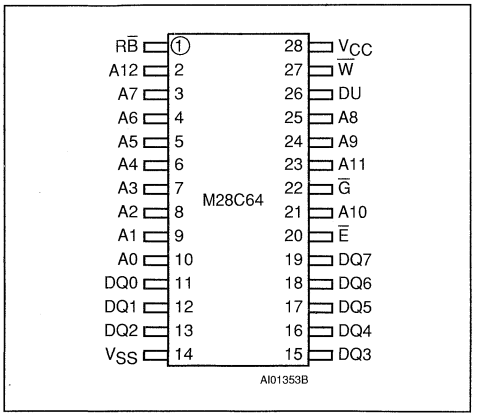
Warning: DU = Don't Use

Figure 2B. LCC Pin Connections



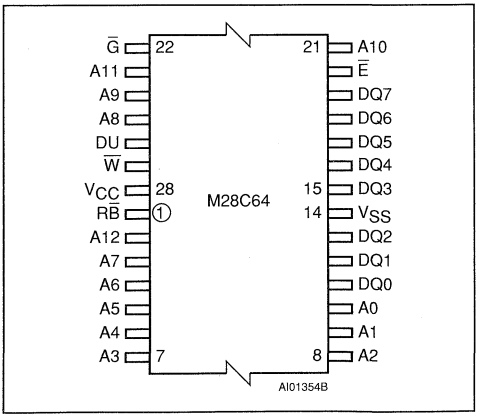
Warning: NC = No Connections, DU = Don't Use

Figure 2C. SO Pin Connections



Warning: DU = Don't Use

Figure 2D. TSOP Pin Connections



Warning: DU = Don't Use

Figure 3. Block Diagram

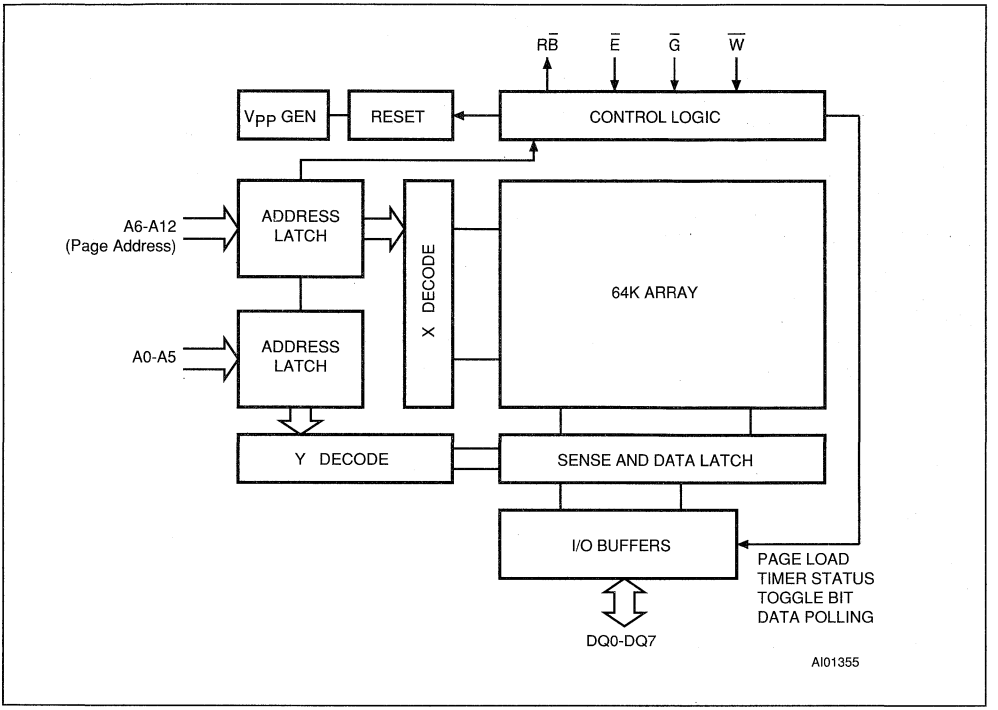


Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z
Chip Erase	V_{IL}	V_{IH} (2)	V_{IL}	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}
2. V_{IH} = 12V ± 5%

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28C64 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C64 through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C64.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28C64 is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28C64 supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 64 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A12 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data up to a maximum of 100µs after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{BLC}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within 100µs, the internal programming cycle will start.

Chip Erase

The contents of the entire memory may be erased (FF) by use of the Chip Erase command by setting Chip Enable ($\overline{E}$) Low and Output Enable ($\overline{G}$) to 12V. The chip is cleared when a 10ms low pulse is applied to the Write Enable pin.

Microcontroller Control Interface

The M28C64 provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the $R\overline{B}$ signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C64 also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$ up to 100µs after the previous byte. Up to 64 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The $R\overline{B}$ pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

Figure 5. Software Data Protection Enable Algorithm and Memory Write

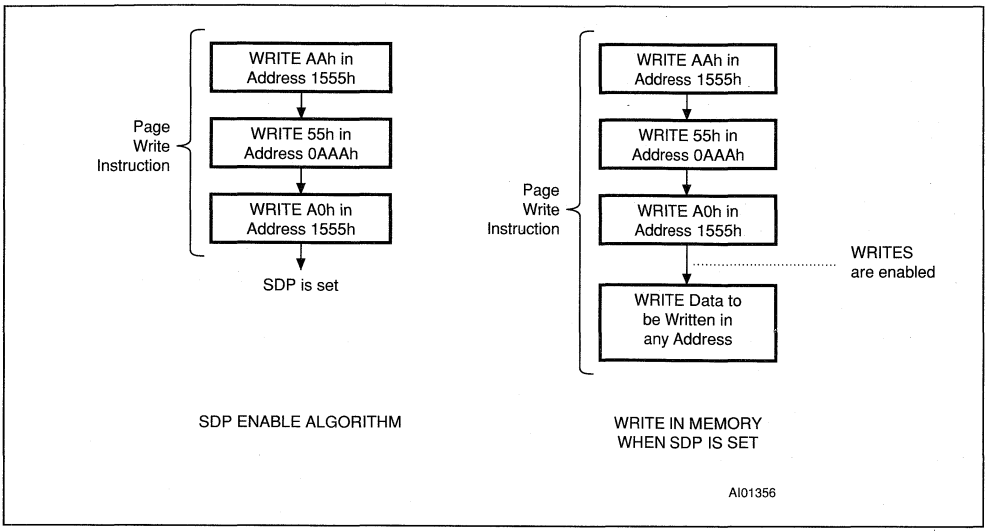
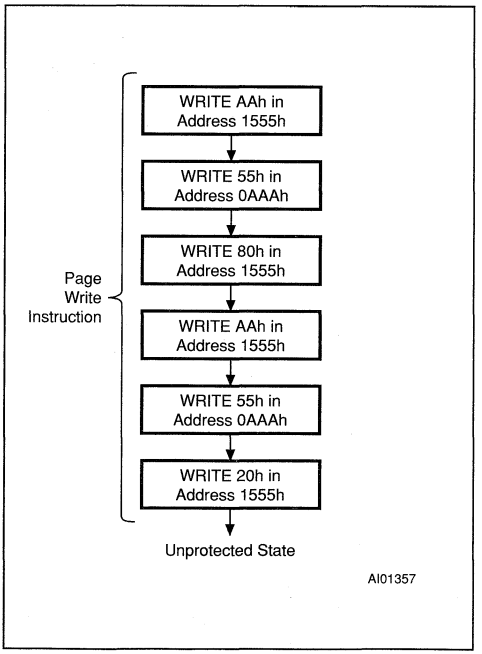


Figure 6. Software Data Protection Disable Algorithm



Software Data Protection

The M28C64 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device including the Chip Erase instruction. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28C64 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents. The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences.

To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write) three specific data bytes to three specific memory locations as per Figure 5. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 6 (with a Page Write). This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

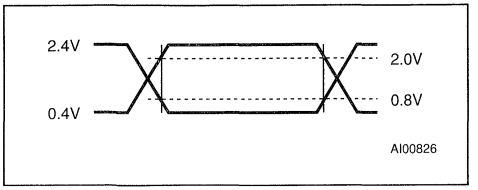


Figure 8. AC Testing Equivalent Load Circuit

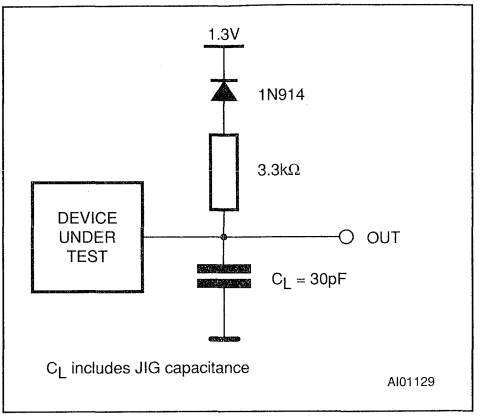


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (TTL inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		30	mA
	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		25	mA
I_{CC1} (1)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

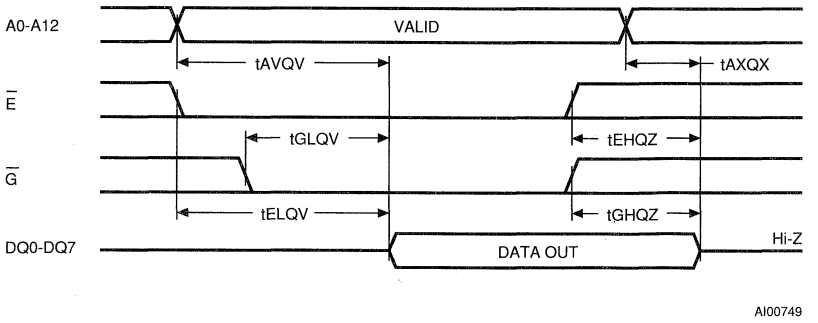
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28C64								Unit
				-70		-90		-120		-150		
				min	max	min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		70		90		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		45		50	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	35	0	40	0	45	0	50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	0	45	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.15	100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			2	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

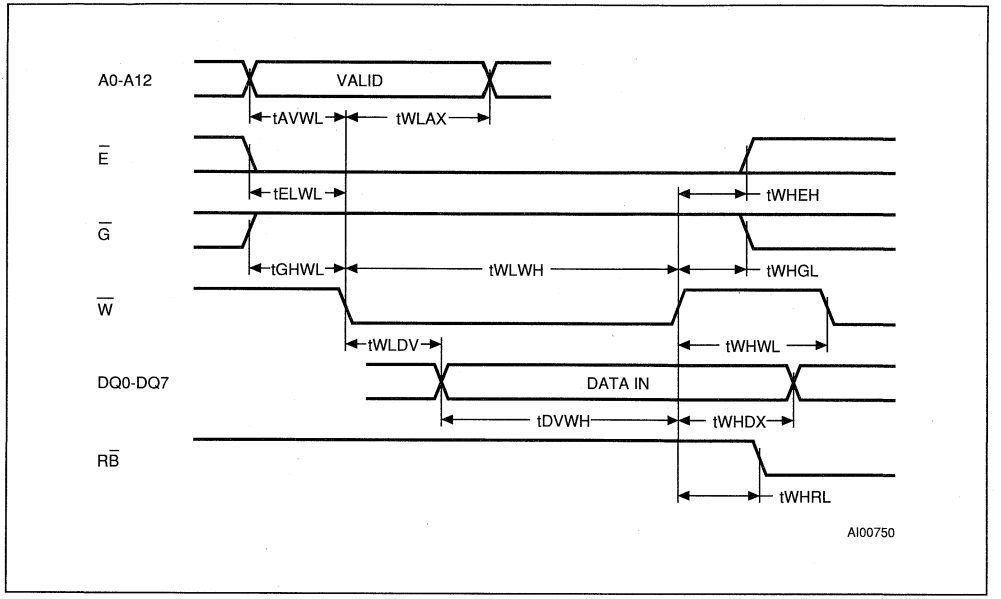


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

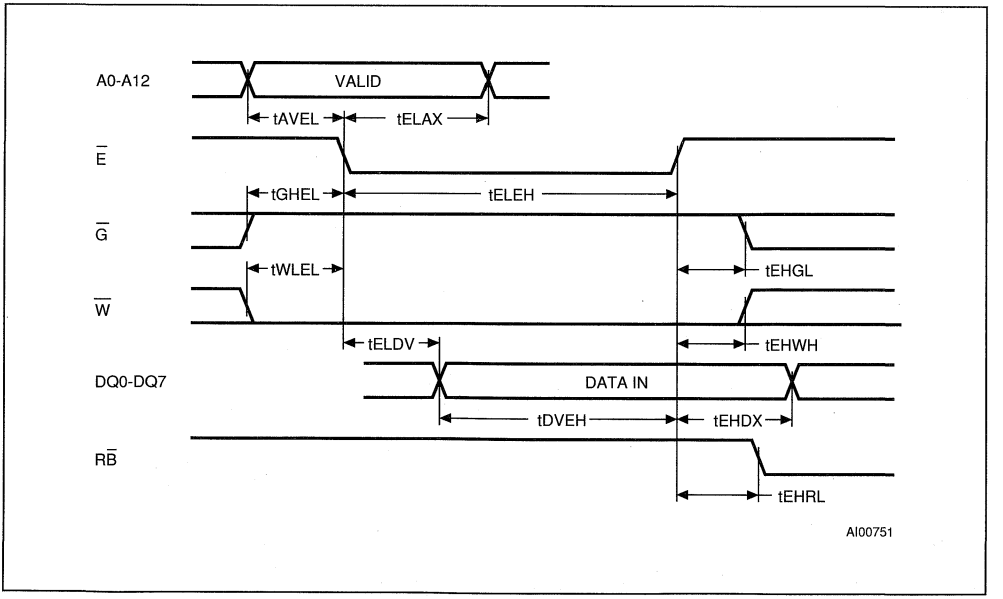


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

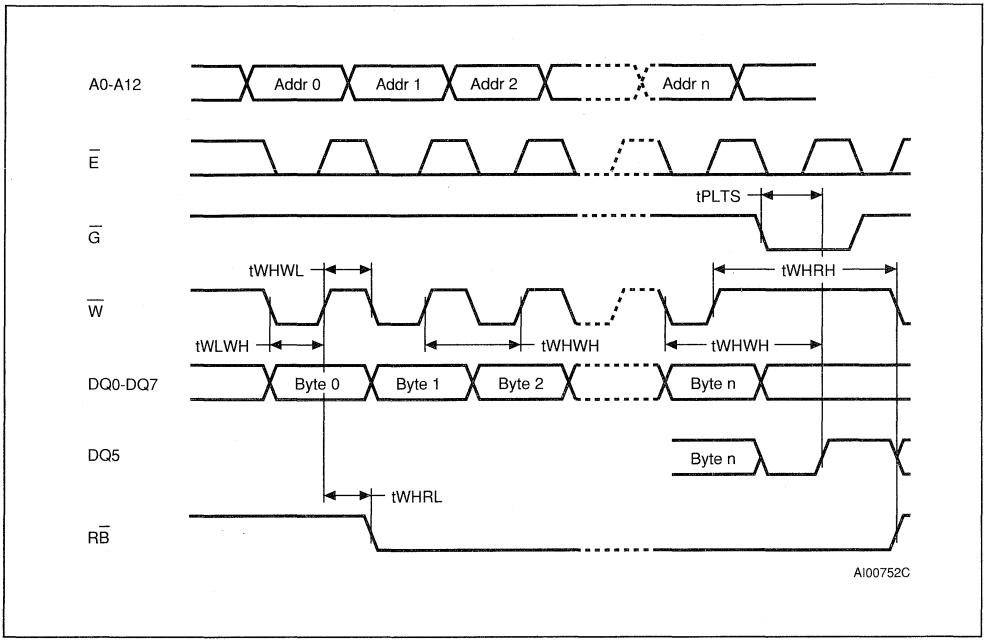
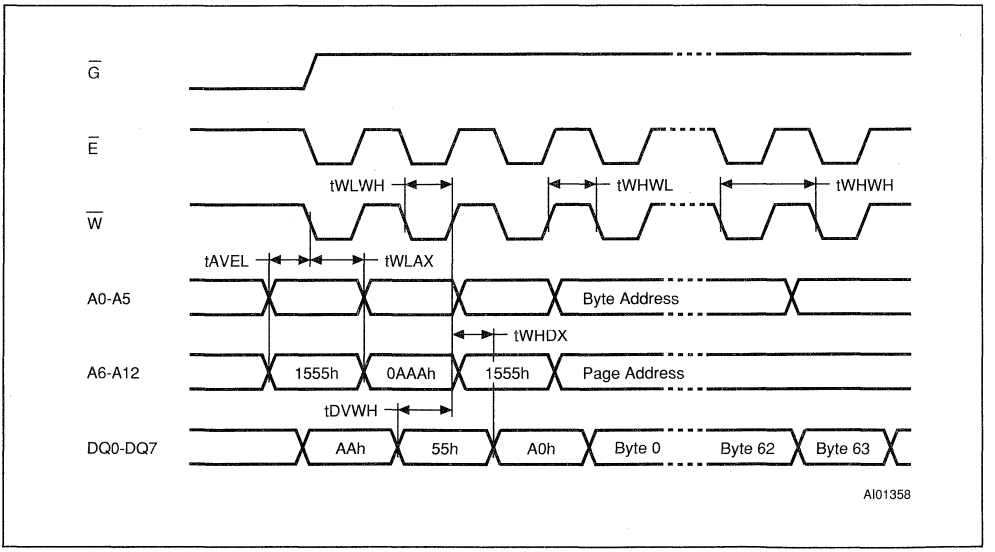


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A12 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Waveforms Sequence

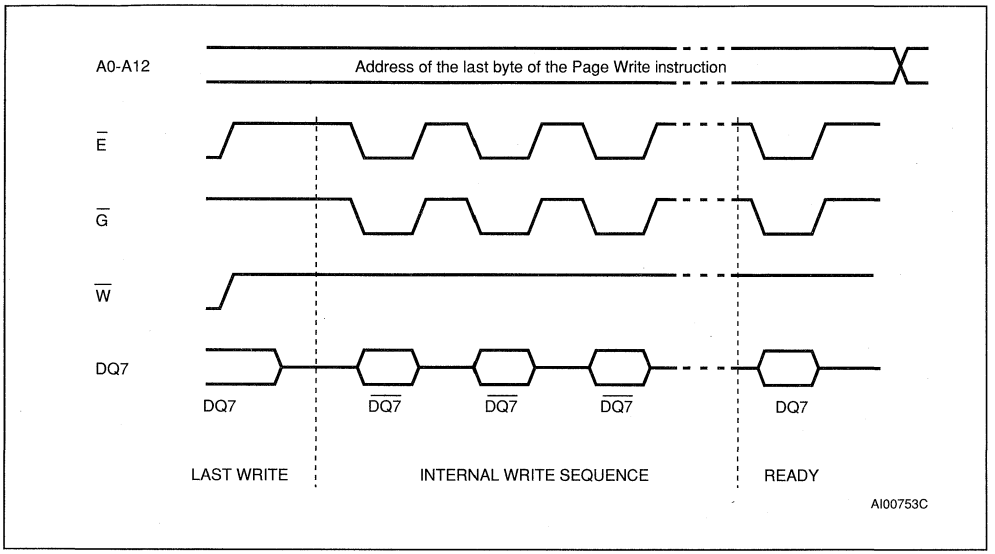
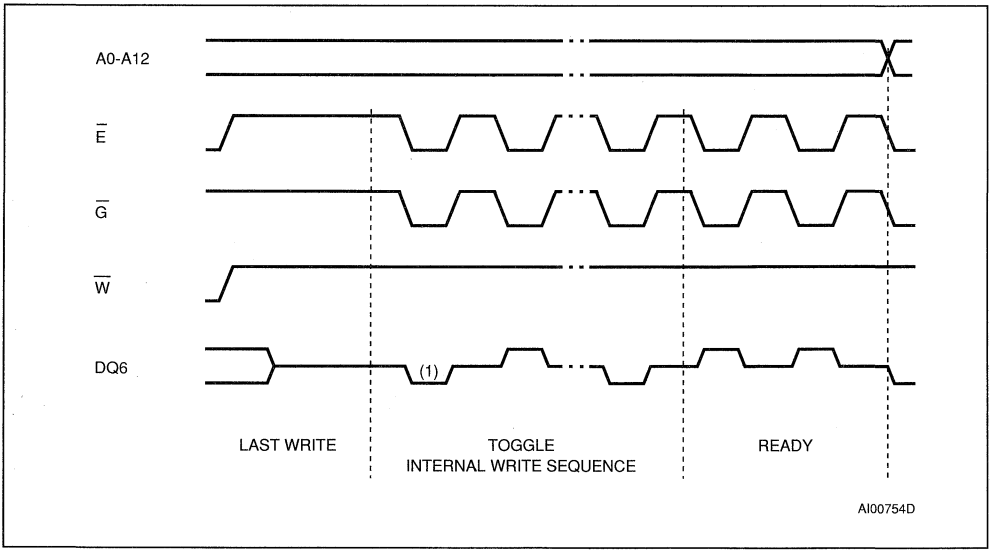


Figure 15. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

Figure 16. Chip Erase AC Waveforms

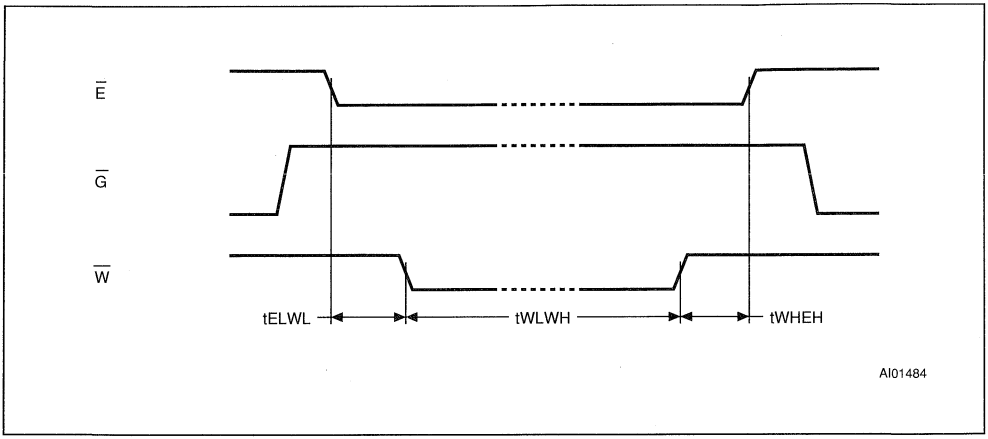


Table 9. Chip Erase AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = 12V	5		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = 12V	5		µs
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{G}$ = 12V	10		ms

ORDERING INFORMATION SCHEME

Example: M28C64 -70 K 1

Speed		Package		Temperature Range	
-70	70ns	P	PDIP28	1	0 to 70 °C
-90	90ns	K	PLCC32	3 *	–40 to 125 °C
-120	120ns	MS	SO28 300 mils	6	–40 to 85 °C
-150	150ns	N	TSOP28 8 x 13.4mm		

Note: 3 * Temperature range on special request only.

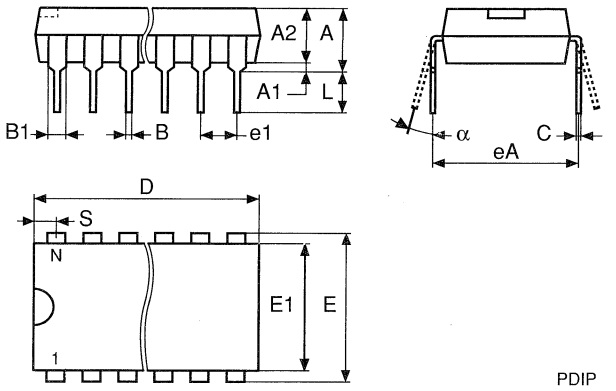
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



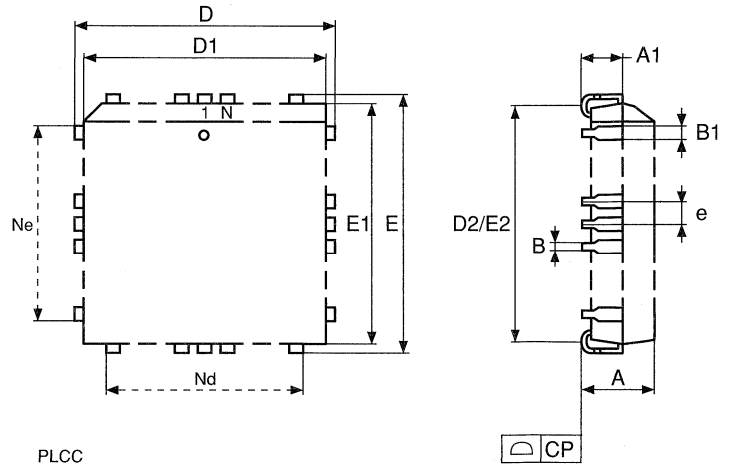
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

PLCC32

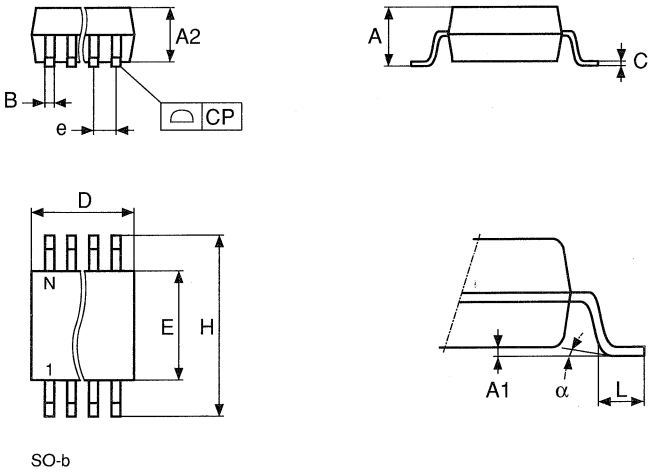


Drawing is out of scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SO28



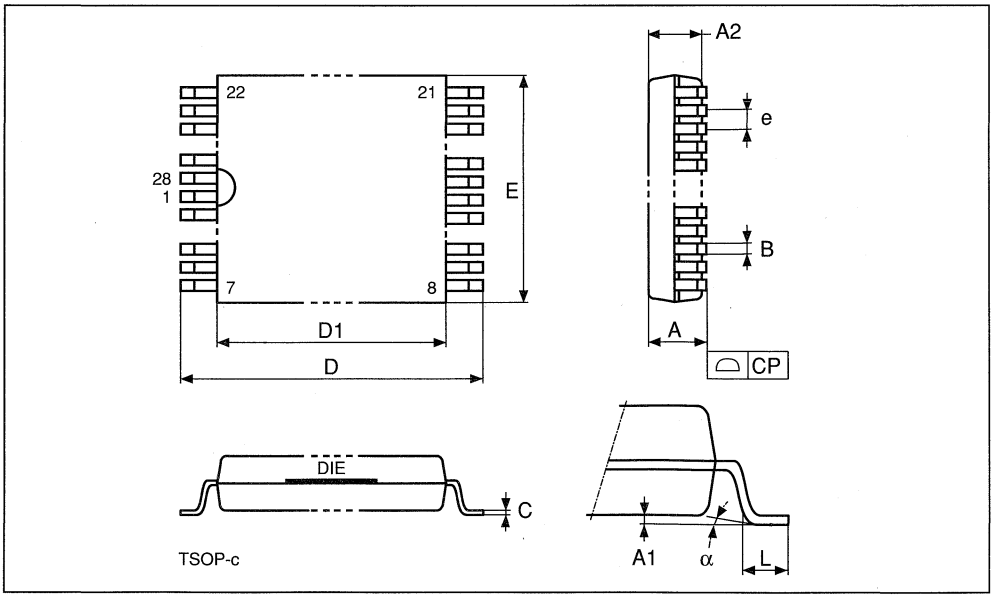
SO-b

Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

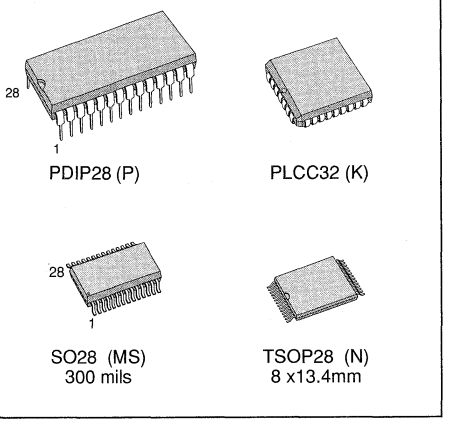
TSOP28



Drawing is out of scale

PARALLEL ACCESS 64K (8K x 8) EEPROM

- FAST ACCESS TIME: 150ns
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION
  - Active Current 30mA
  - Standby Current 100µA
- FAST WRITE CYCLE
  - 32 Bytes Page Write Operation
  - Byte or Page Write Cycle: 5ms
- ENHANCED END OF WRITE DETECTION
  - Ready/Busy Open Drain Output (for M28C64C product only)
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP



DESCRIPTION

The M28C64C is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time (150ns) with low power dissipation and requires a 5V power supply.

Table 1. Signal Names

A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

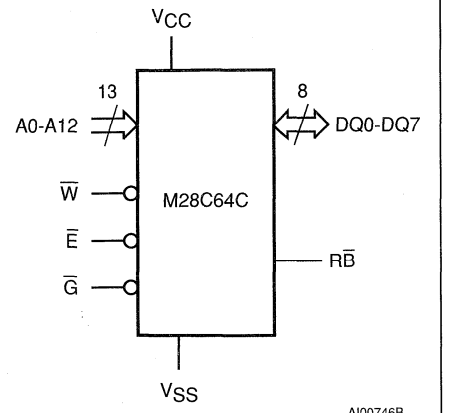
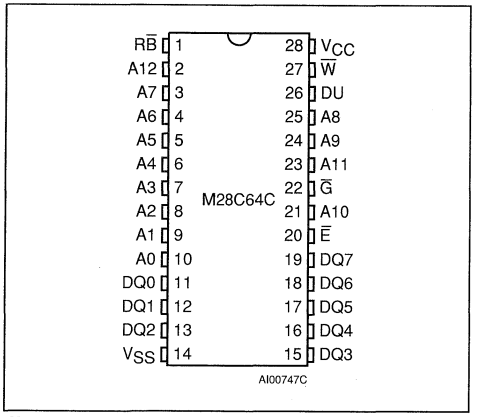


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 6	0 to 70 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)		2000	V

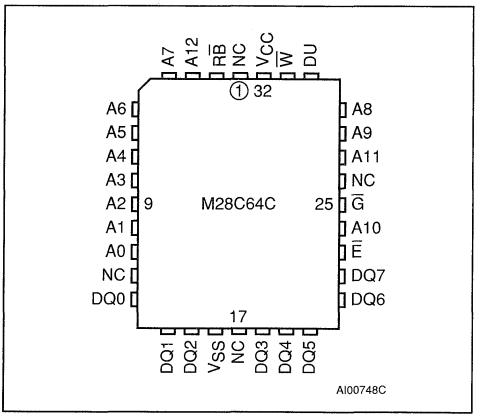
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2A. DIP Pin Connections



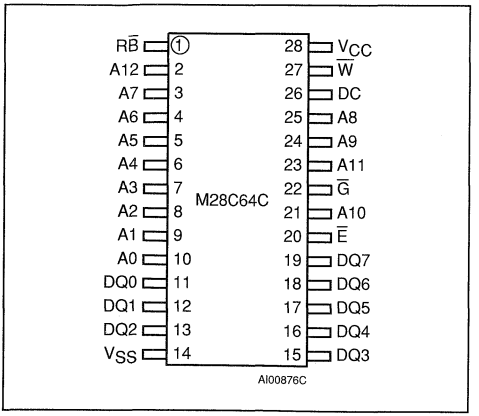
Warning: DU = Don't Use

Figure 2B. LCC Pin Connections



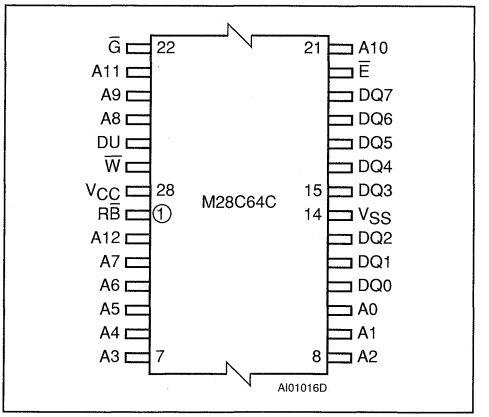
Warning: NC = No Connections, DU = Don't Use

Figure 2C. SO Pin Connections



Warning: DU = Don't Use

Figure 2D. TSOP Pin Connections



Warning: DU = Don't Use

Figure 3. Block Diagram

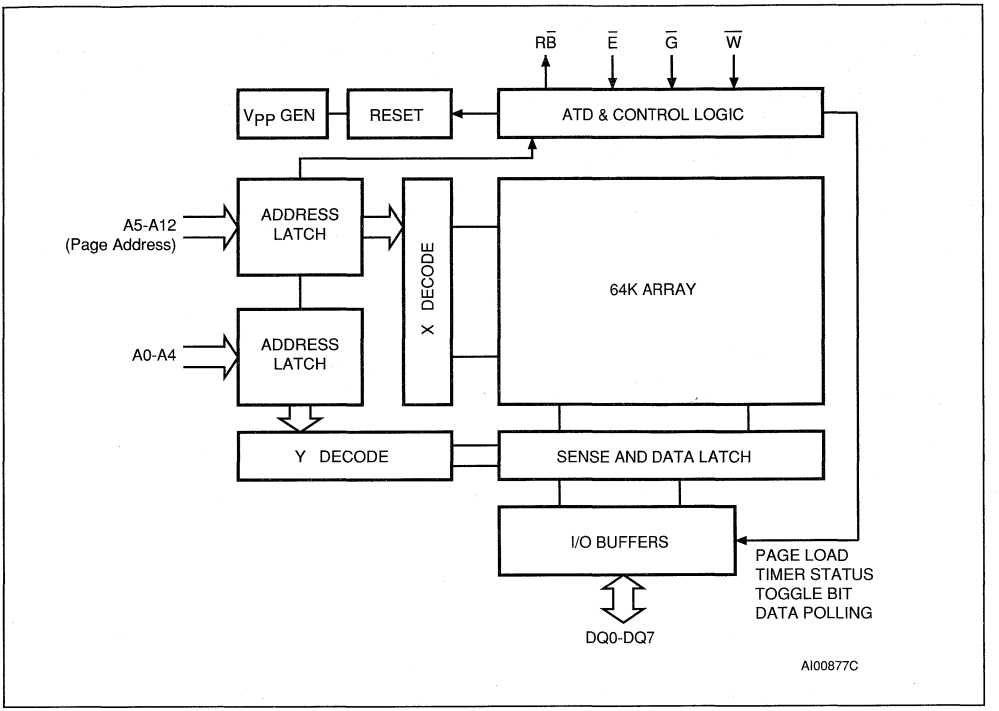


Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking mode with Ready/Busy, Data Polling and Toggle Bit. The M28C64C supports 32 byte page write operation.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

PIN DESCRIPTION (cont'd)

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C64C through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C64C.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28C64C is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The M28C64C supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5 - A12 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data up to a maximum of 100µs after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{BLC}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within 100µs, the internal programming cycle will start.

Microcontroller Control Interface

The M28C64C provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the $R\overline{B}$ signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C64C also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any address in the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$ up to 100µs after the previous byte. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The $R\overline{B}$ pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input Output Waveforms

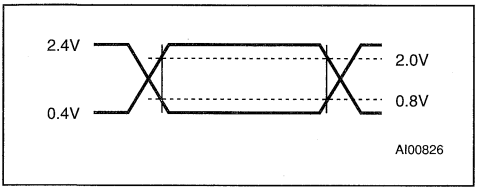


Figure 6. AC Testing Equivalent Load Circuit

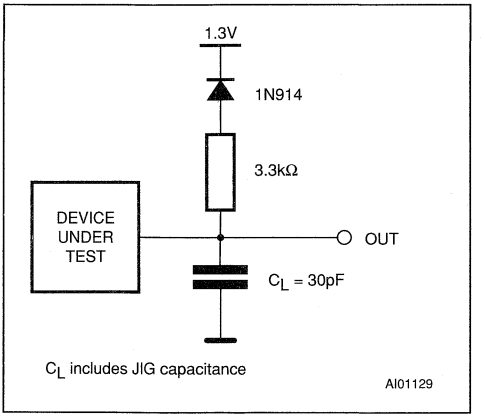


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (TTL and CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5 MHz		30	mA
I_{CC1} (1)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		2	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

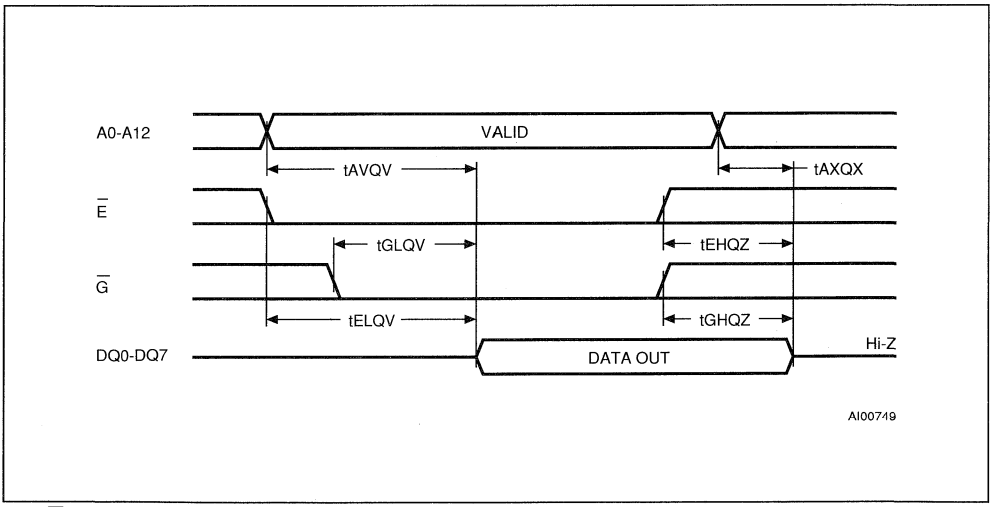
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28C64C						Unit
				-150		-200		-250		
				min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$G = V_{IL}$		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		100		110	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	60	0	65	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	60	0	65	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		150		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		150		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		150		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		150		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		10		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		10		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.35	50	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

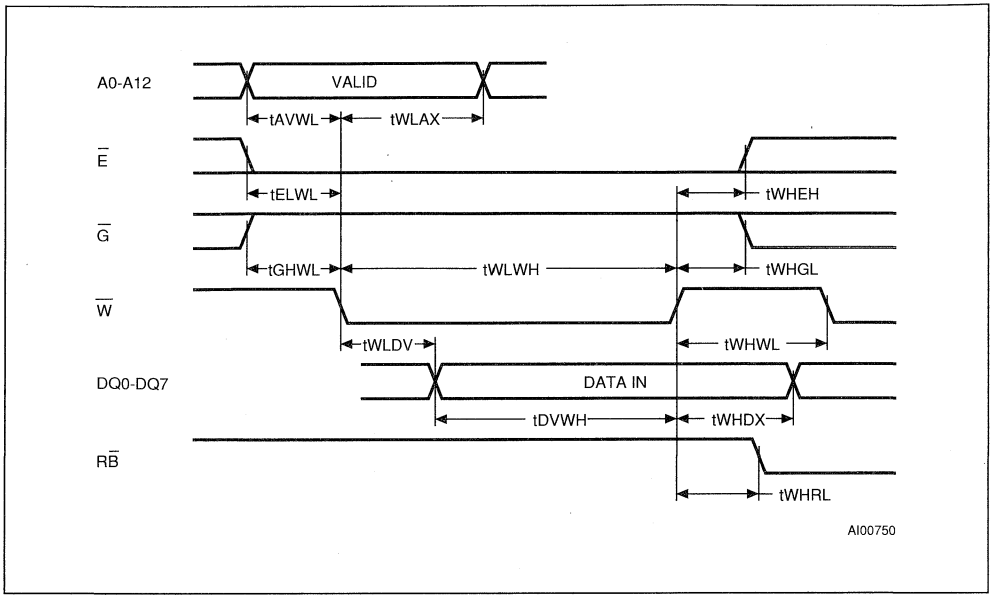


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

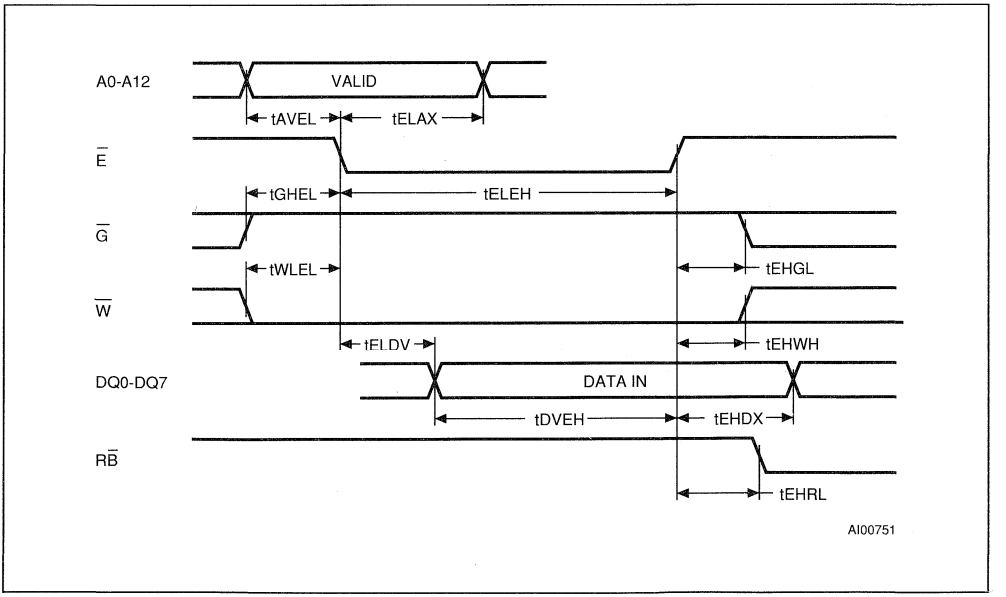


Figure 10. Page Write Mode AC Waveforms - Write Enable Controlled

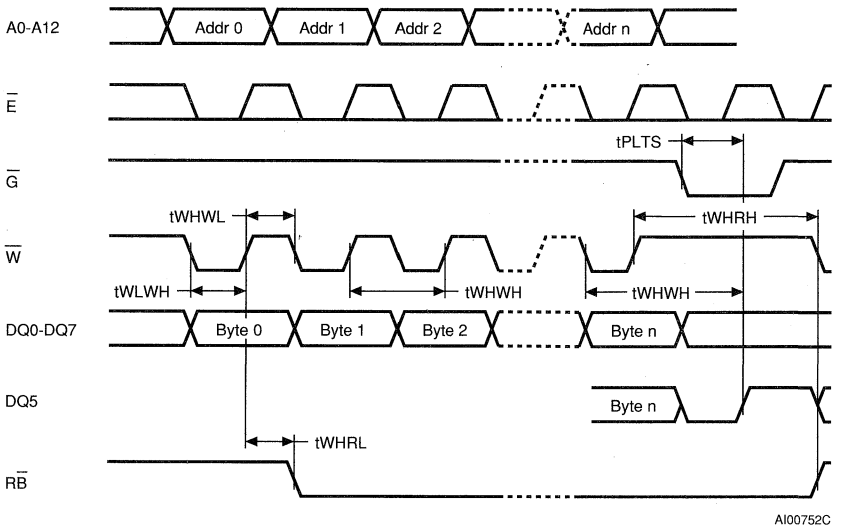


Figure 11. Data Polling Waveforms Sequence

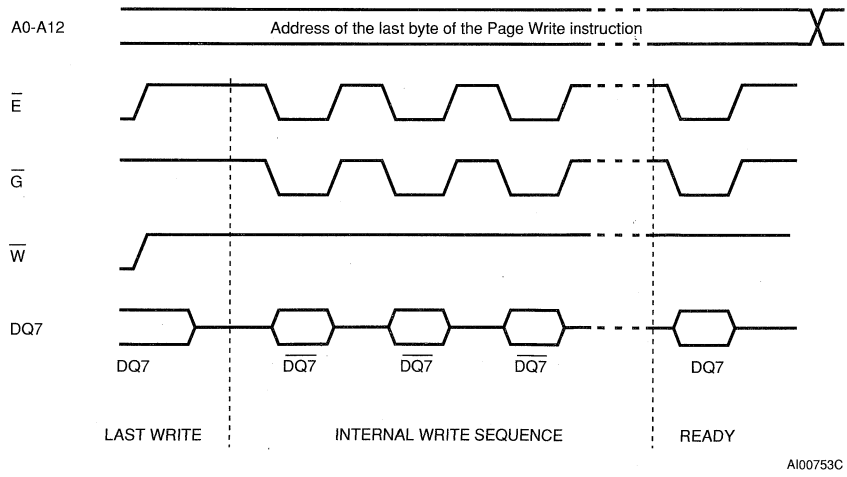
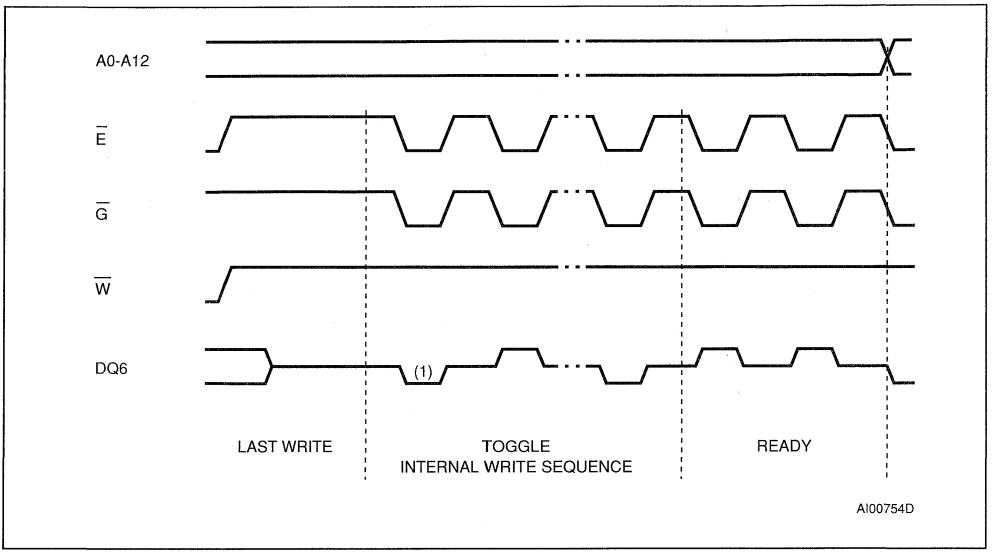


Figure 12. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME

Example: M28C64C -150 K 1

Version		Speed		Package		Temperature Range	
C	RB available	-150	150 ns	P	PDIP28	1	0 to 70 °C
X	RB not bonded (pin NC)	-200	200 ns	K	PLCC32	6	–40 to 85 °C
		-250	250 ns	MS	SO28 300 mils		
				N	TSOP28 8 x 13.4mm		

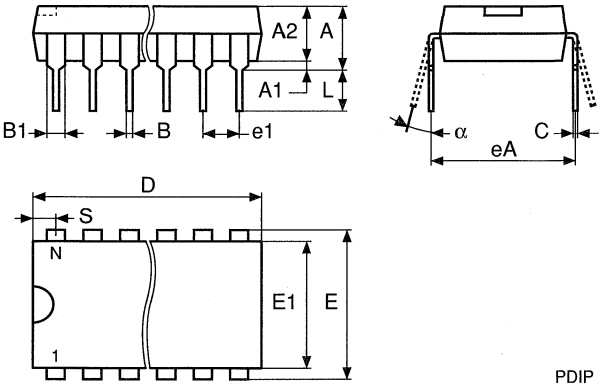
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



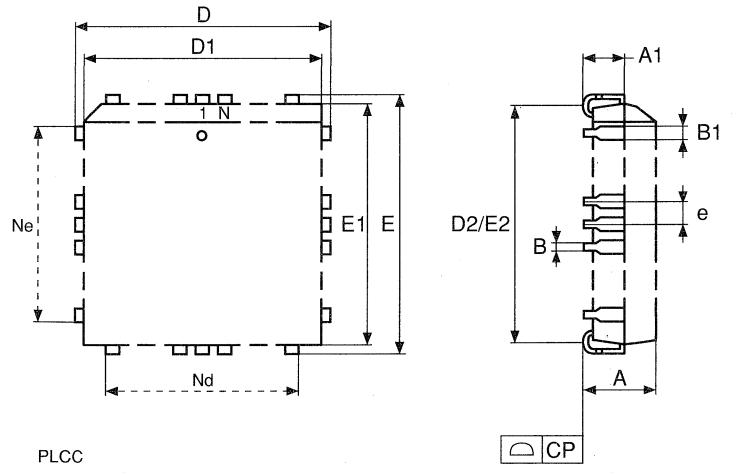
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



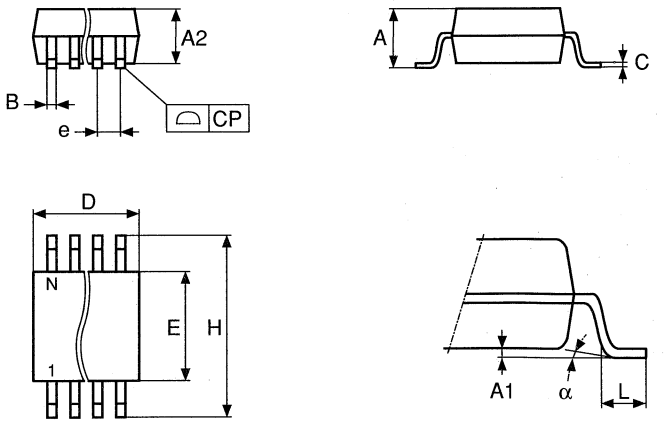
PLCC

Drawing is out of scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SO28



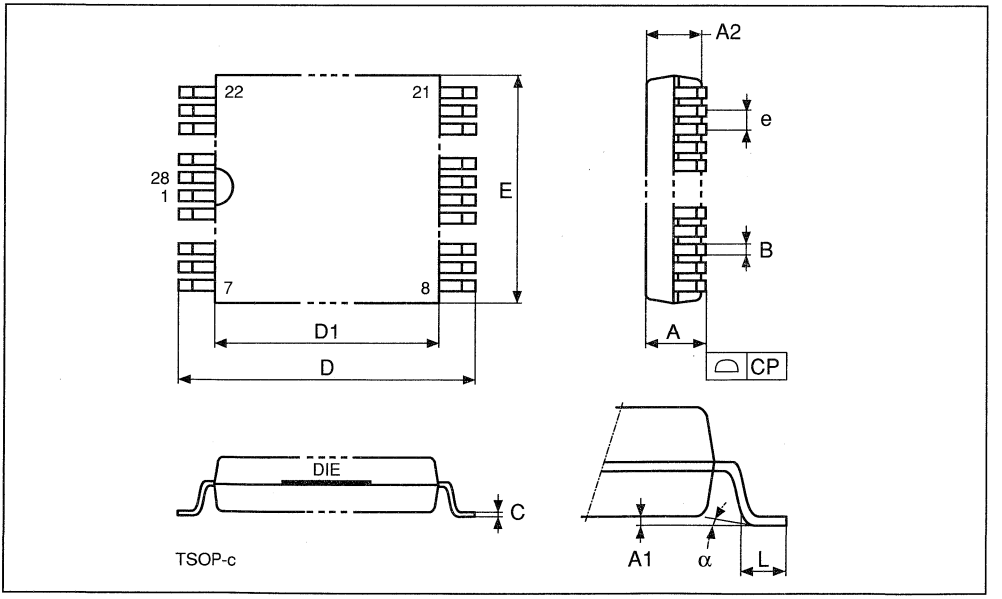
SO-b

Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

TSOP28

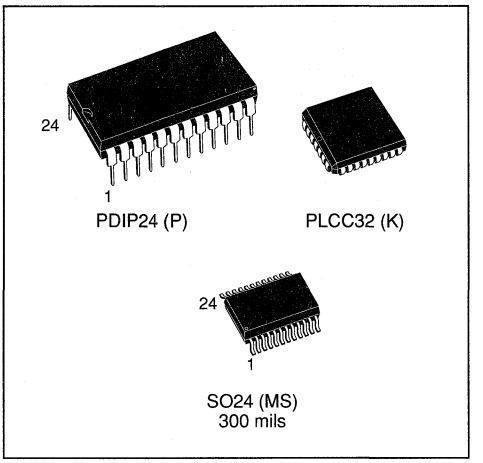


Drawing is out of scale

LOW VOLTAGE PARALLEL ACCESS 16K (2K x 8) EEPROM

PRODUCT PREVIEW

- FAST ACCESS TIME: 150ns
- SINGLE 3V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION:
  - Active Current 8mA
  - Standby Current 50µA
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle: 3ms Max
- ENHANCED END OF WRITE DETECTION:
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP
- SOFTWARE DATA PROTECTION



DESCRIPTION

The M28LV16 is a 2K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 3V ± 10% power supply.

Table 1. Signal Names

A0 - A10	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

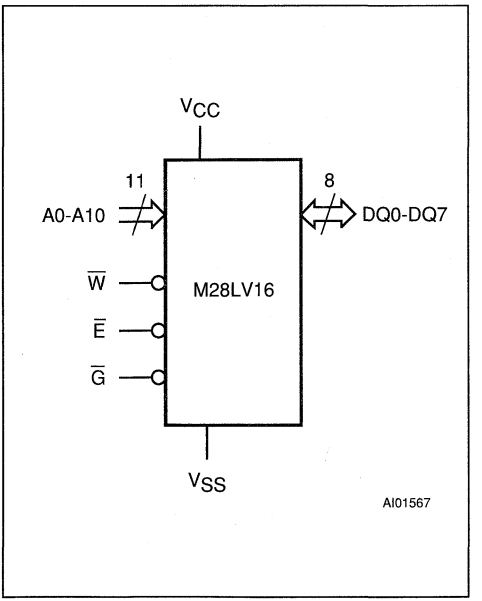


Figure 2A. DIP Pin Connections

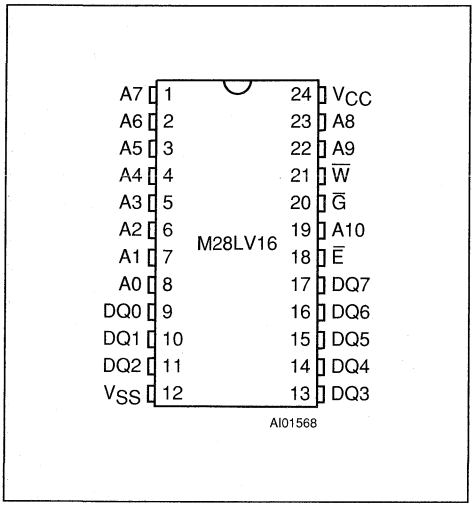
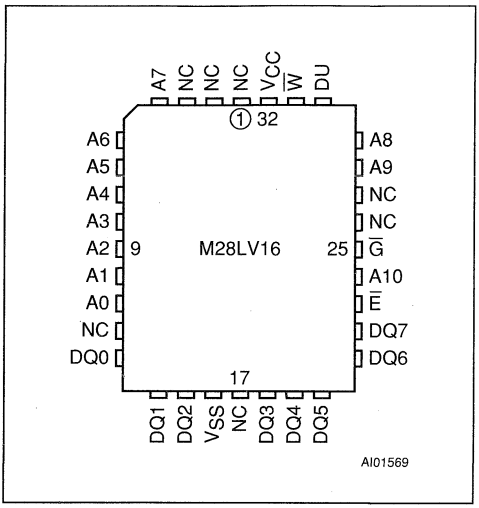
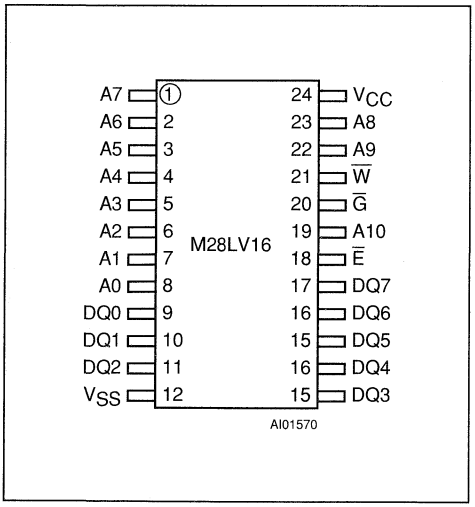


Figure 2B. LCC Pin Connections



Warning: NC = No Connections, DU = Don't Use

Figure 2C. SO Pin Connections



DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Data Polling and Toggle Bit. The M28LV16 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRITPION

Addresses (A0-A10). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28LV16 through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28LV16.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 3 grade 6	0 to 70 – 40 to 125 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z
Chip Erase	V_{IL}	V_{IH} (2)	V_{IL}	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}
2. V_{IH} = 12V ± 5%

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28LV16 is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

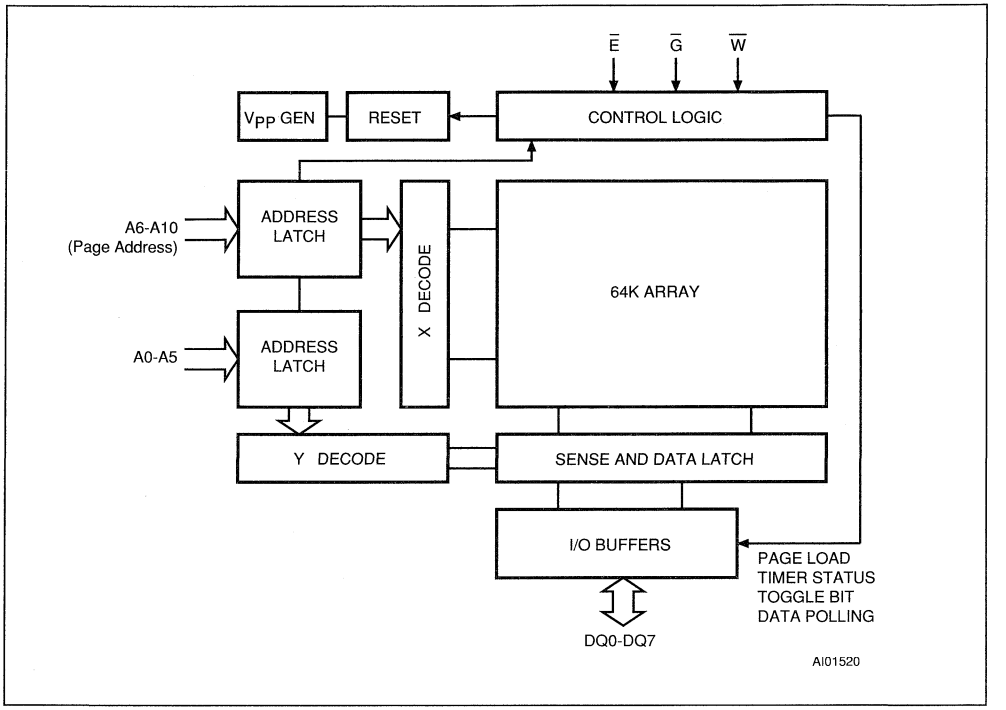
Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28LV16 supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 64 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A10 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{WHWH}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within a minimum time (t_{WHWH} max), the internal programming cycle will start.

Figure 3. Block Diagram



Chip Erase

The contents of the entire memory may be erased (FF) by use of the Chip Erase command by setting Chip Enable ($\overline{E}$) Low and Output Enable ($\overline{G}$) to 12V. The chip is cleared when a 10ms low pulse is applied to the Write Enable pin.

Microcontroller Control Interface

The M28LV16 provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28LV16 also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Figure 5. Software Data Protection Enable Algorithm and Memory Write

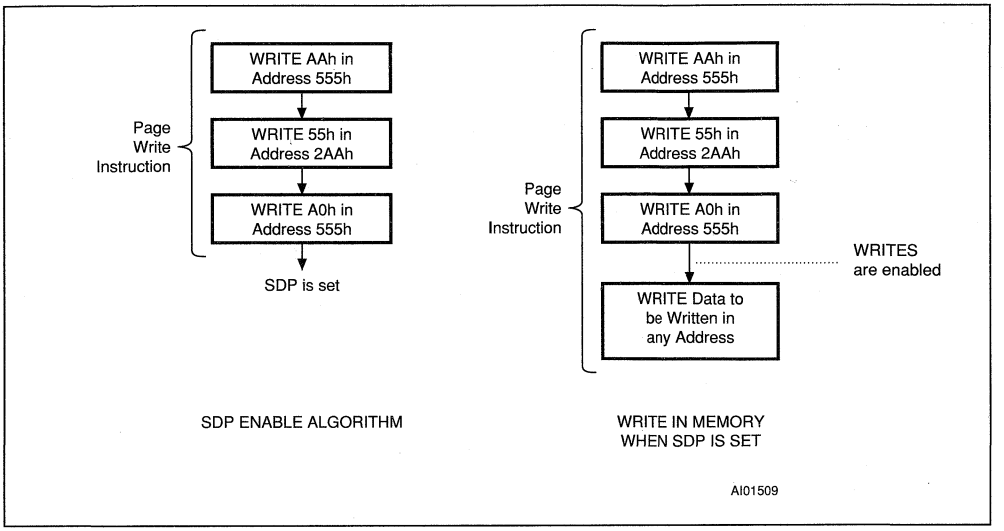
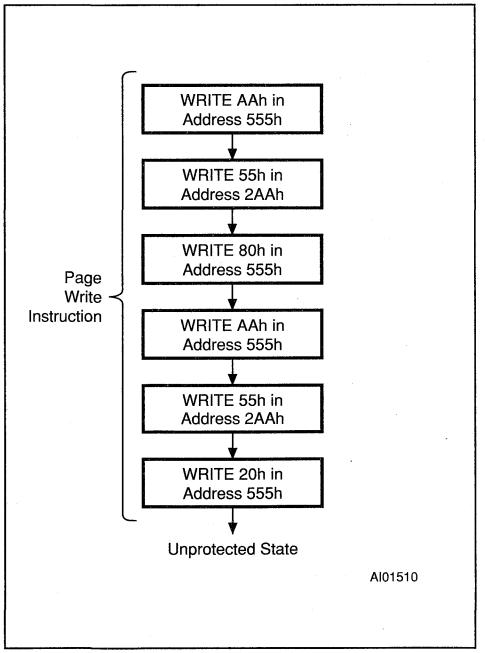


Figure 6. Software Data Protection Disable Algorithm



Software Data Protection

The M28LV16 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device including the Chip Erase instruction. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28LV16 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents. The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences.

To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write) three specific data bytes to three specific memory locations as per Figure 5. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 6 (with a Page Write). This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0V to V_{CC} -0.3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

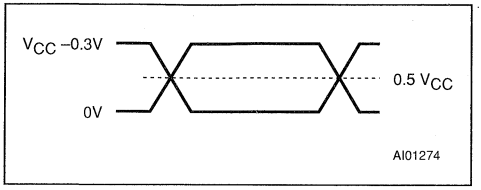


Figure 8. AC Testing Equivalent Load Circuit

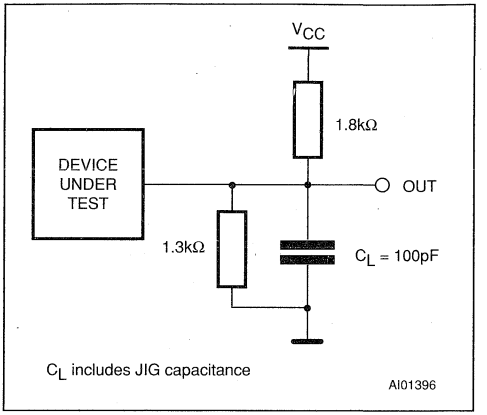


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		8	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 1 mA	0.8 V_{CC}		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

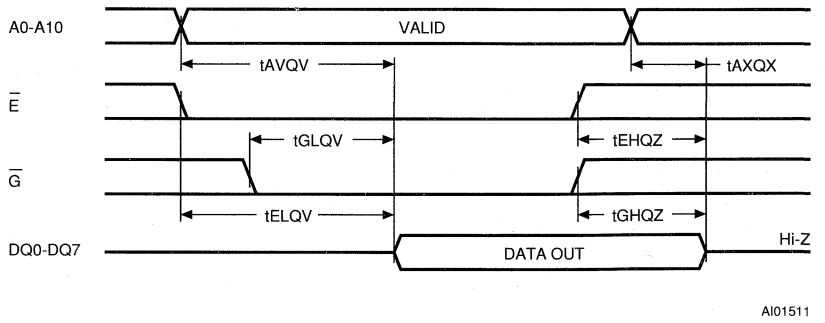
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28LV16						Unit
				-150		-200		-300		
				min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		80		95		150	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	45	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50	1000	ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.15	100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			3	ms
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

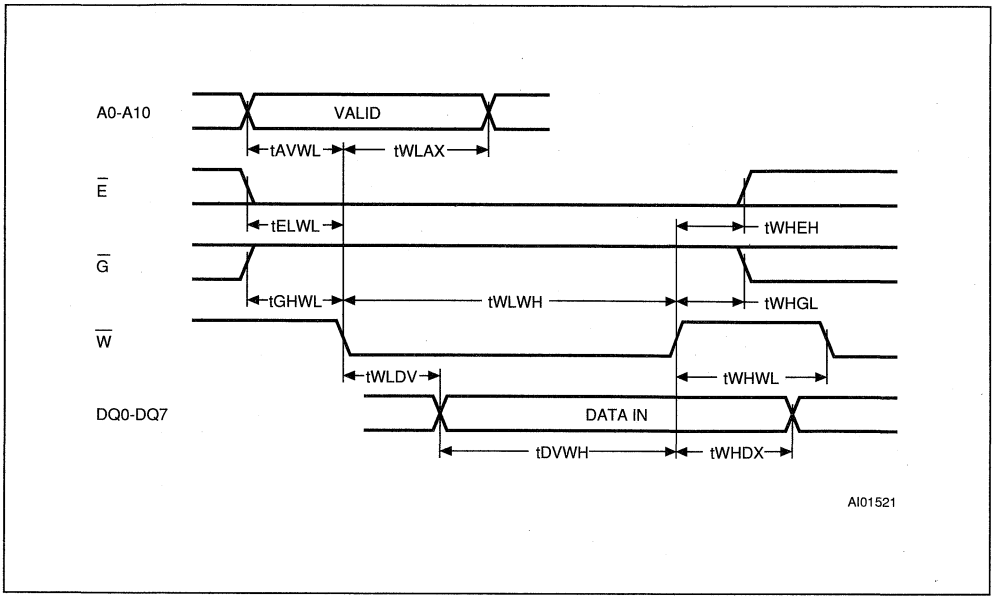


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

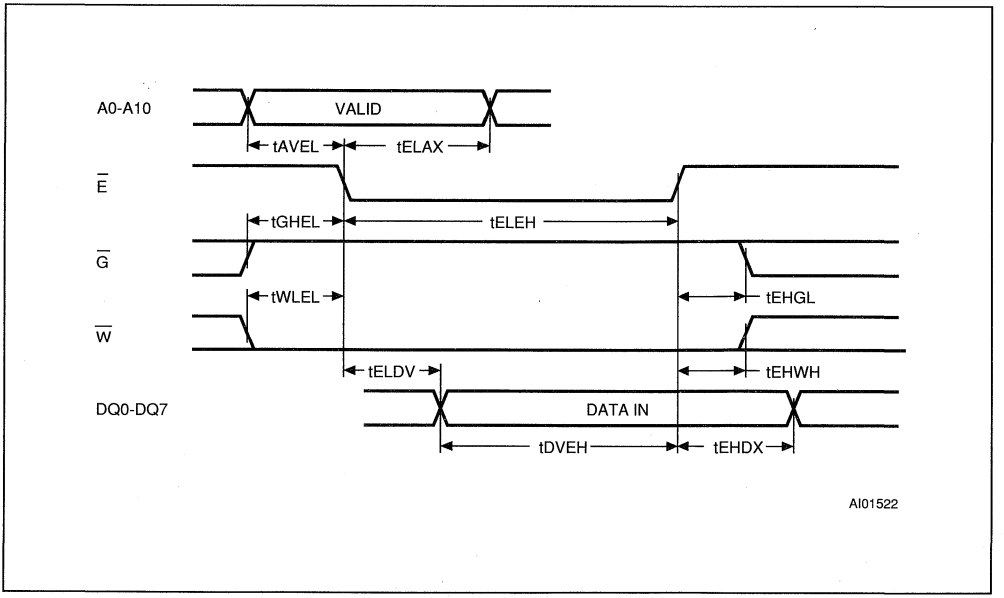


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

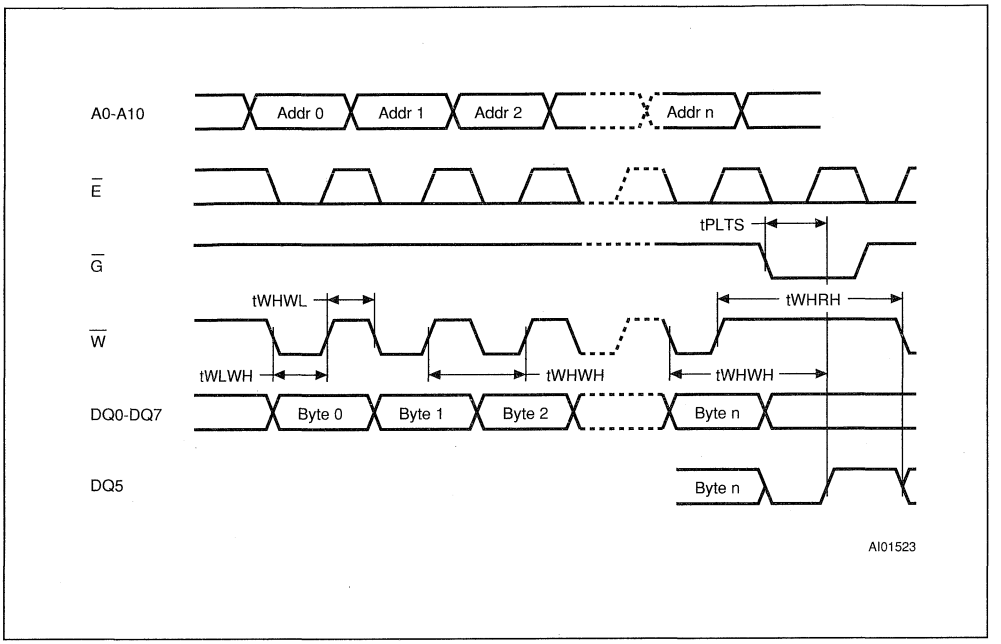
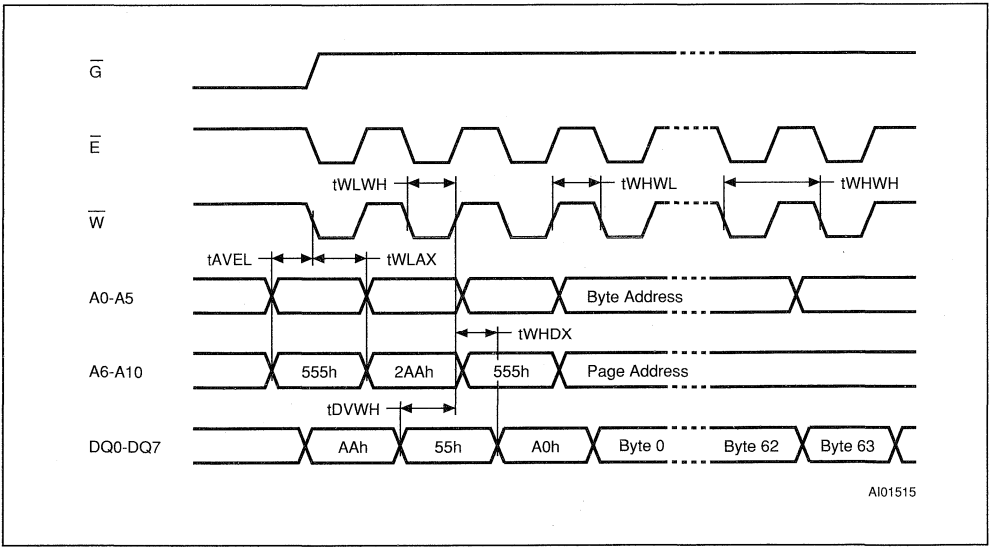


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A10 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Waveforms Sequence

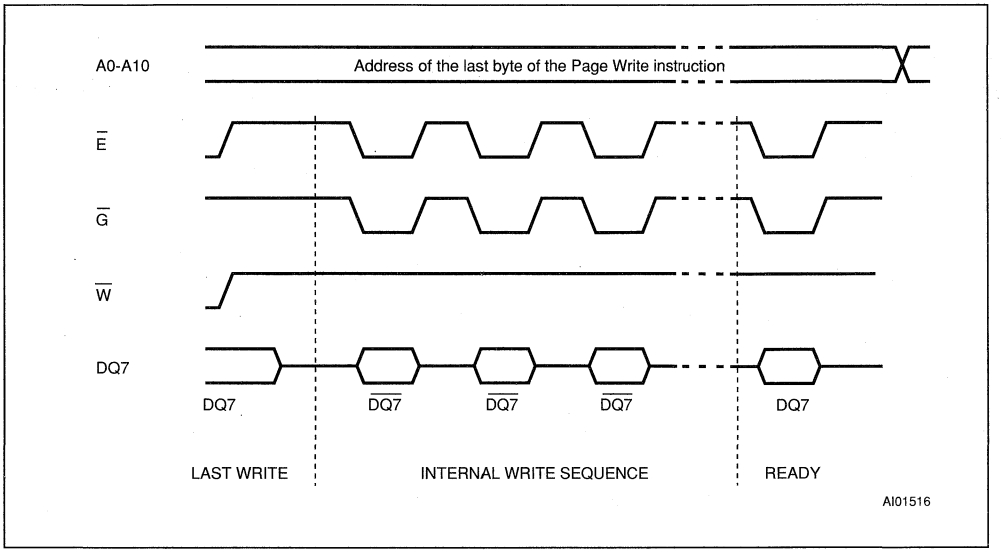
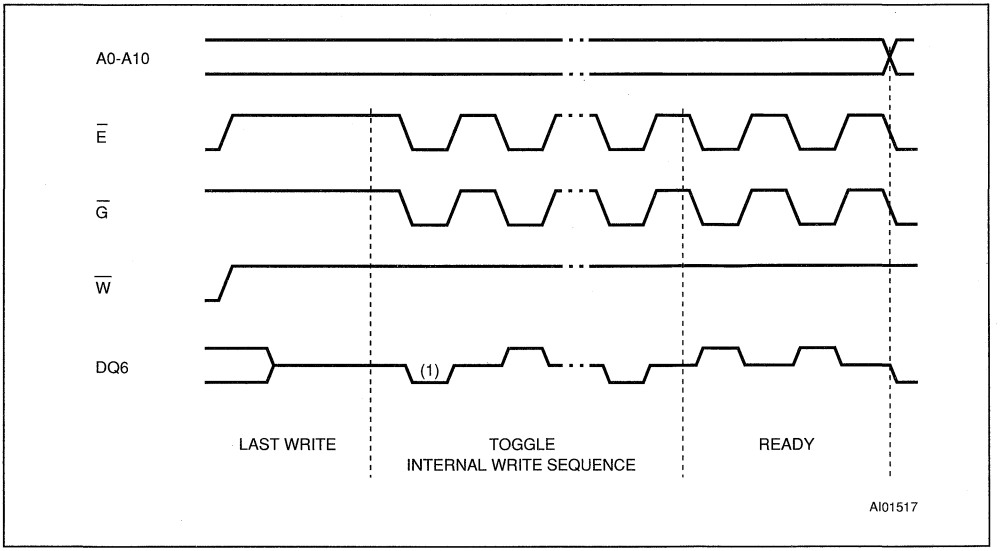


Figure 15. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

Figure 16. Chip Erase Wavforms

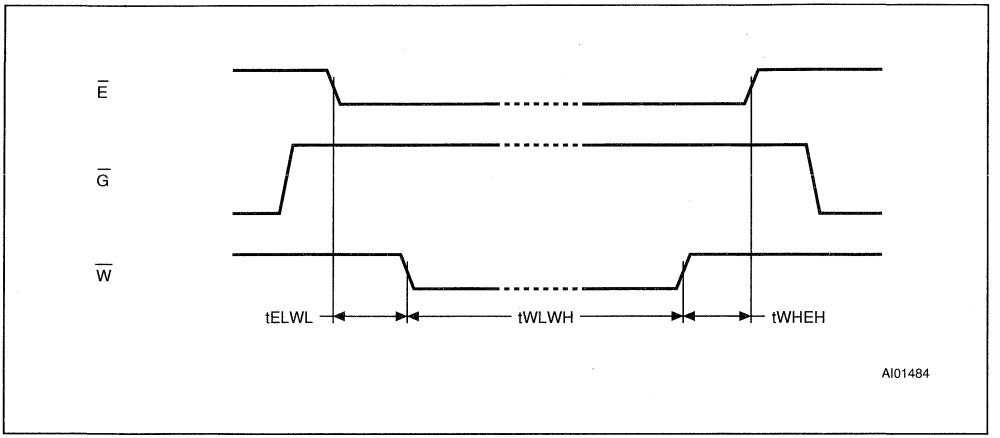


Table 9. Chip Erase AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = 12V	5		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = 12V	5		µs
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{G}$ = 12V	10		ms

ORDERING INFORMATION SCHEME

Example: M28LV16 -200 K 1

Speed		Package		Temperature Range	
-150	150ns	P	PDIP24	1	0 to 70 °C
-200	200ns	K	PLCC32	3 *	–40 to 125 °C
-300	300ns	MS	SO24 300mils	6	–40 to 85 °C

Note: 3 * Temperature range on special request only.

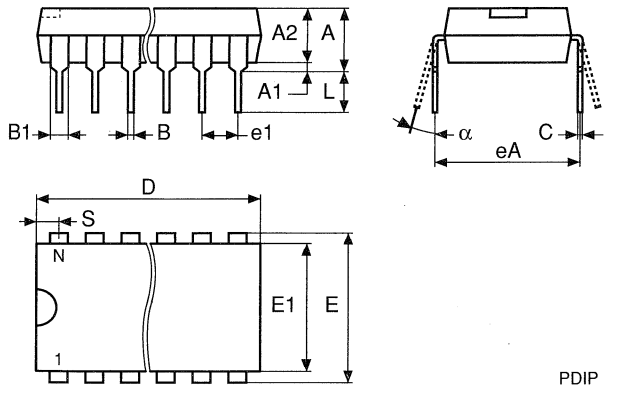
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP24 - 24 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D			32.26			1.270
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	24			24		

PDIP24



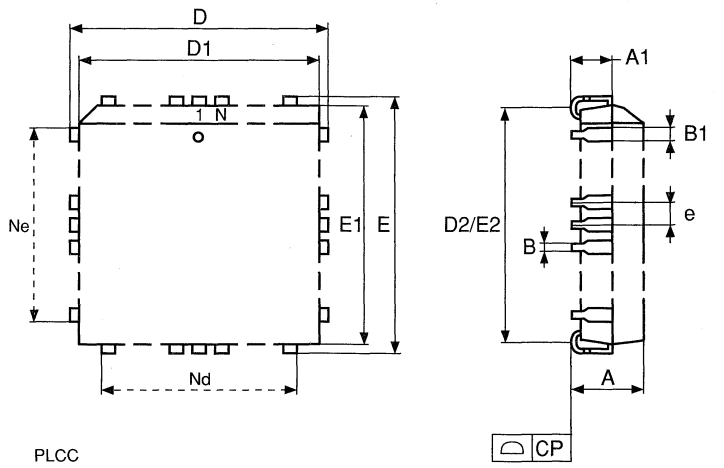
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

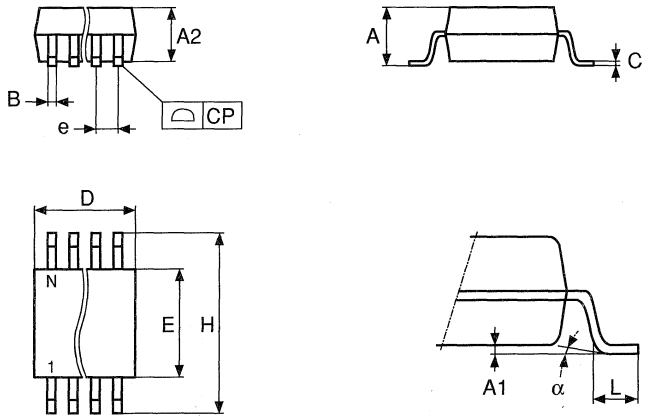


Drawing is out of scale

SO24 - 24 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		15.20	15.60		0.598	0.614
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	24			24		
CP			0.10			0.004

SO24



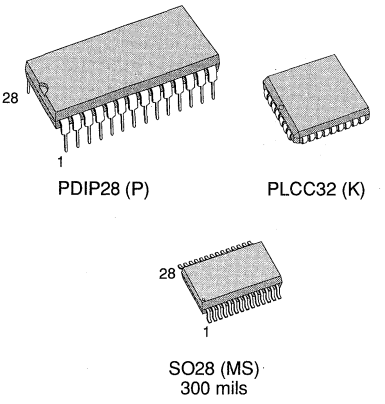
SO-b

Drawing is out of scale

PARALLEL ACCESS 16K (2K x 8) EEPROM

PRODUCT PREVIEW

- FAST ACCESS TIME: 70ns
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle: 2ms Max
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- SOFTWARE DATA PROTECTION



DESCRIPTION

The M28C17 is a 2K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time (70ns) with low power dissipation and requires a 5V power supply.

The M28C17 offers the same features than the M28C16, in addition to the Ready/Busy pin.

Table 1. Signal Names

A0 - A10	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

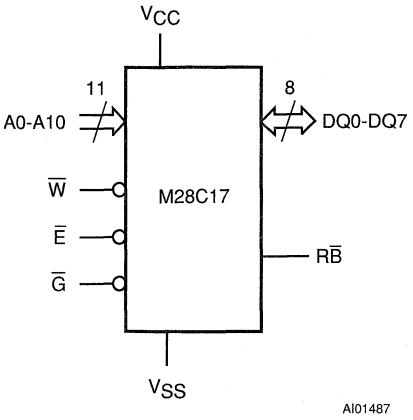
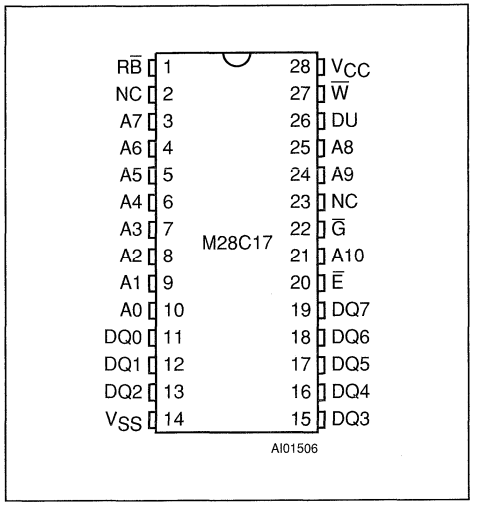
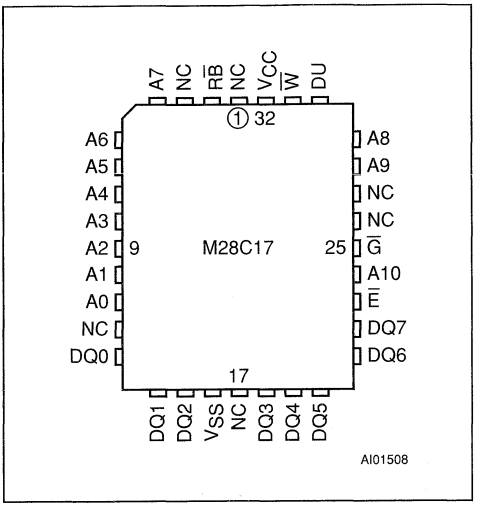


Figure 2A. DIP Pin Connections



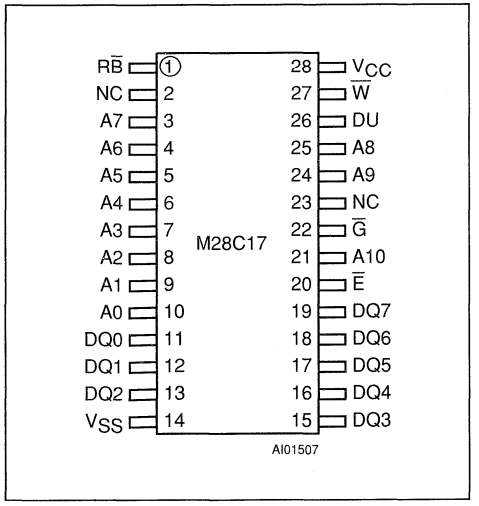
Warning: NC = No Connection, DU = Don't Use

Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use

Figure 2C. SO Pin Connections



Warning: NC = No Connection, DU = Don't Use

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28C17 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRITPION

Addresses (A0-A10). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C17 through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C17.

Ready/Busy ($\overline{RB}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 3 grade 6	0 to 70 – 40 to 125 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z
Chip Erase	V_{IL}	V_{IH} (2)	V_{IL}	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}
2. V_{IH} = 12V ± 5%

Read

The M28C17 is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28C17 supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

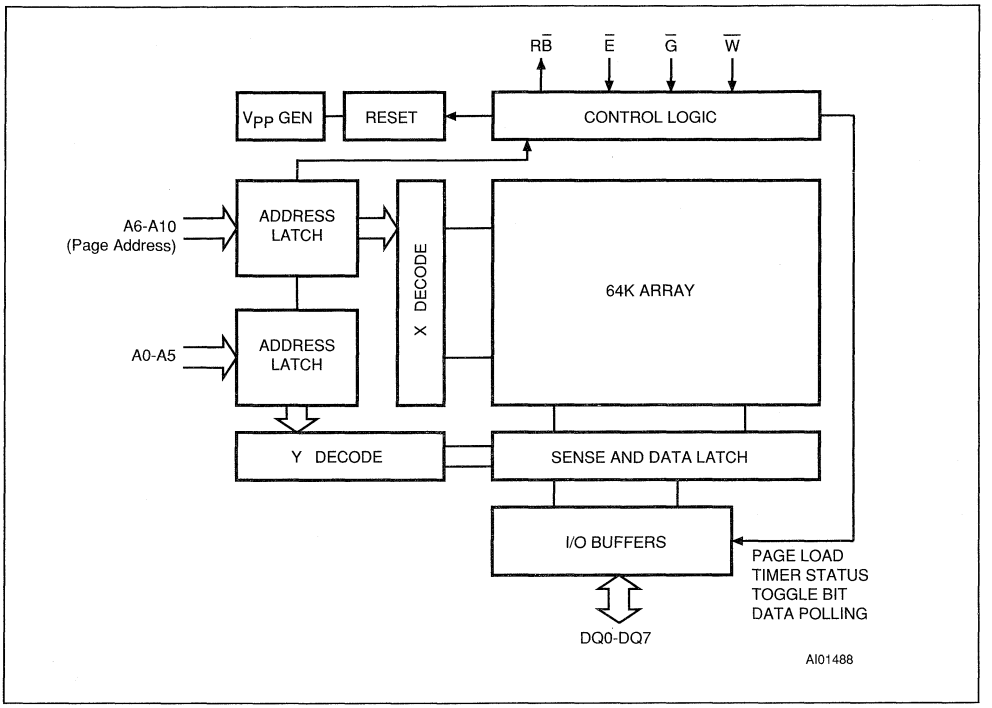
Page write allows up to 64 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A10 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{WHWH}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within a minimum time (t_{WHWH} max), the internal programming cycle will start.

Chip Erase

The contents of the entire memory may be erased (FF) by use of the Chip Erase command by setting Chip Enable ($\overline{E}$) Low and Output Enable ($\overline{G}$) to 12V. The chip is cleared when a 10ms low pulse is applied to the Write Enable pin.

Figure 3. Block Diagram



Microcontroller Control Interface

The M28C17 provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the RB signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C17 also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by E or W. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The RB pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

Figure 5. Software Data Protection Enable Algorithm and Memory Write

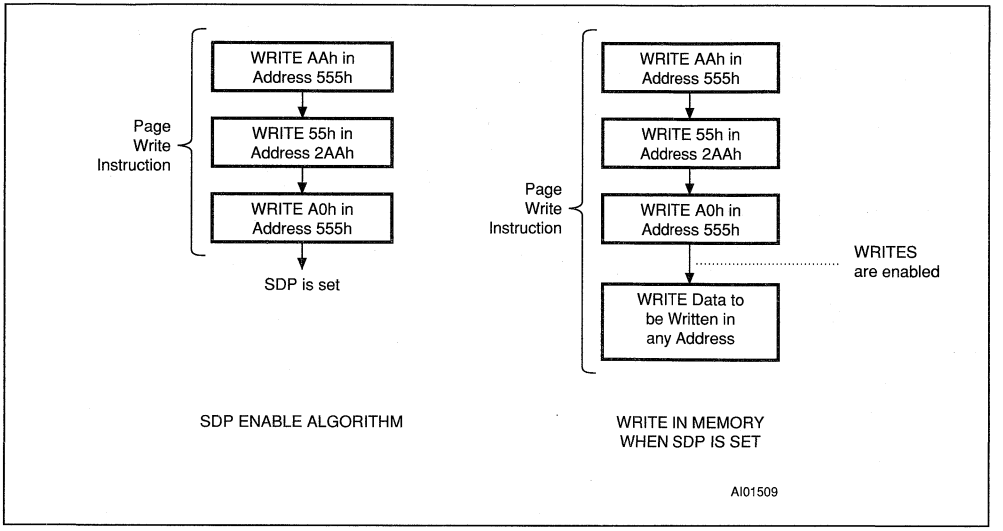
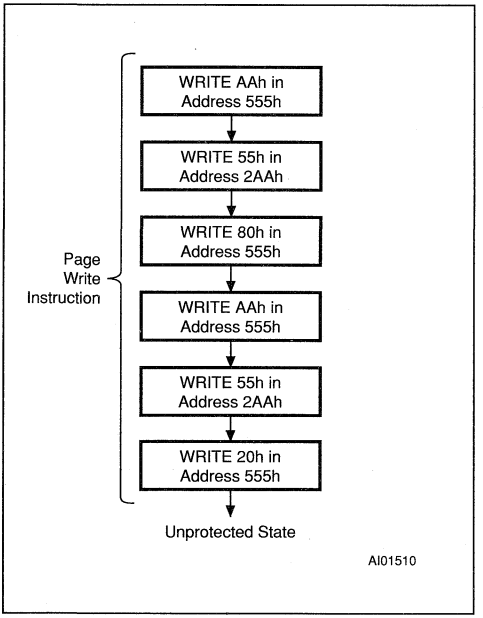


Figure 6. Software Data Protection Disable Algorithm



Software Data Protection

The M28C17 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device including the Chip Erase instruction. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28C17 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents. The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences.

To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write) three specific data bytes to three specific memory locations as per Figure 5. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 6 (with a Page Write). This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

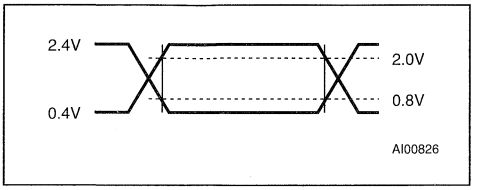


Figure 8. AC Testing Equivalent Load Circuit

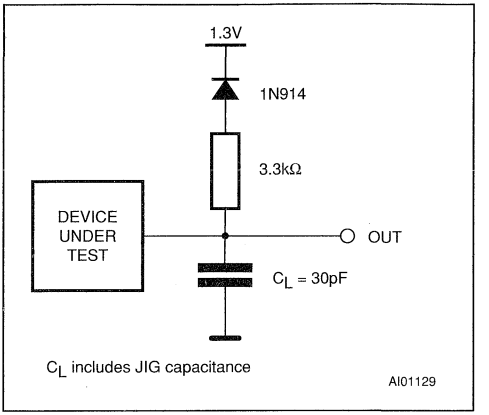


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (TTL inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		30	mA
	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		25	mA
I_{CC1} (1)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

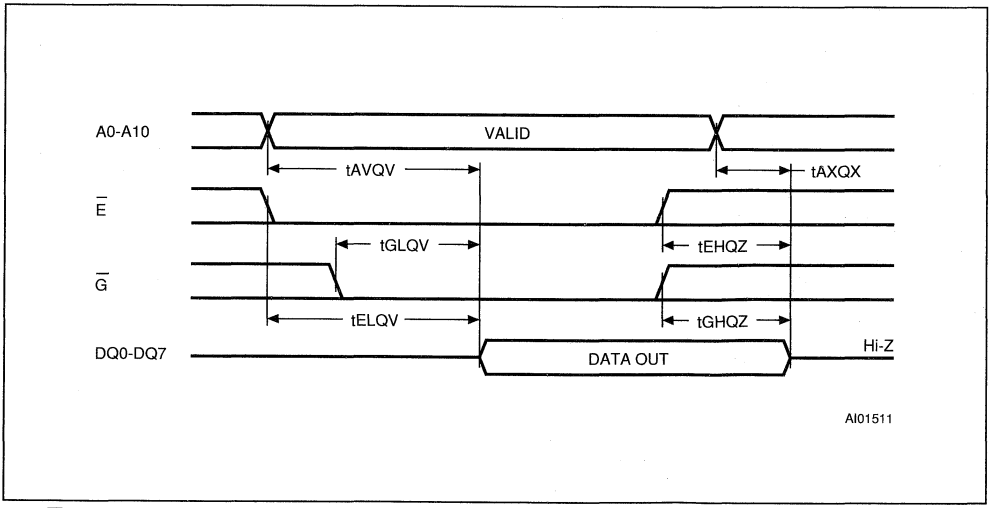
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28C17								Unit
				-70		-90		-120		-150		
				min	max	min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		90		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		45		50	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	35	0	40	0	45	0	50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	0	45	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.15	100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			2	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

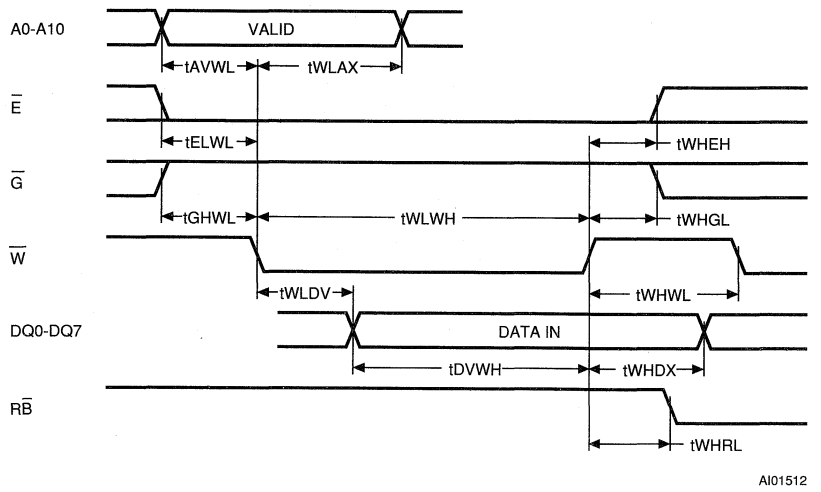


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

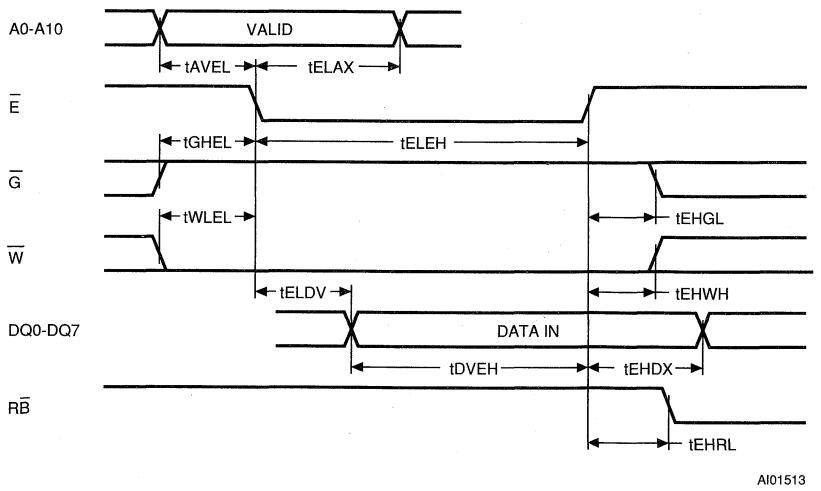


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

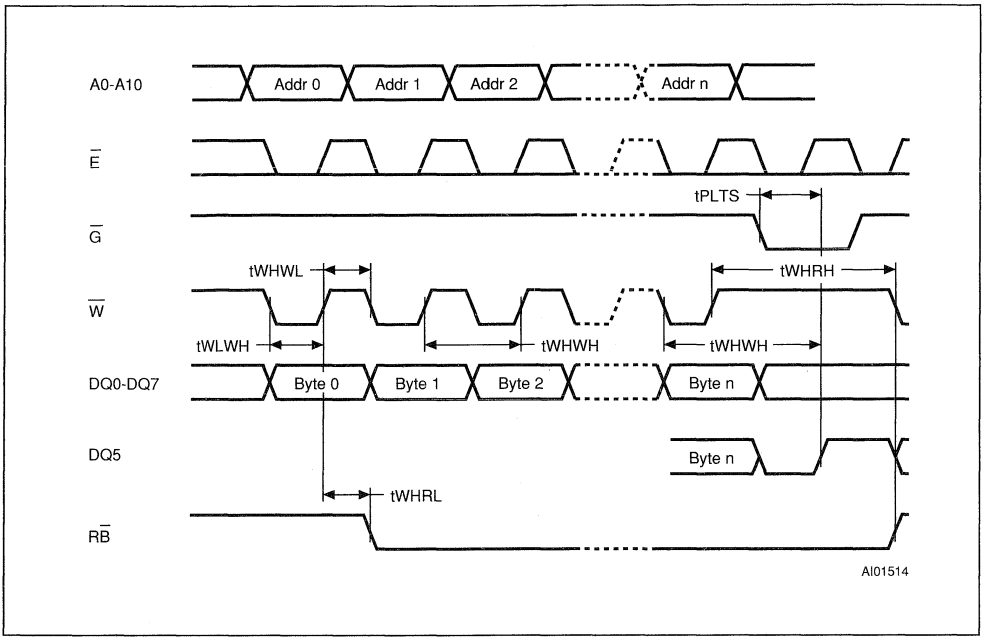
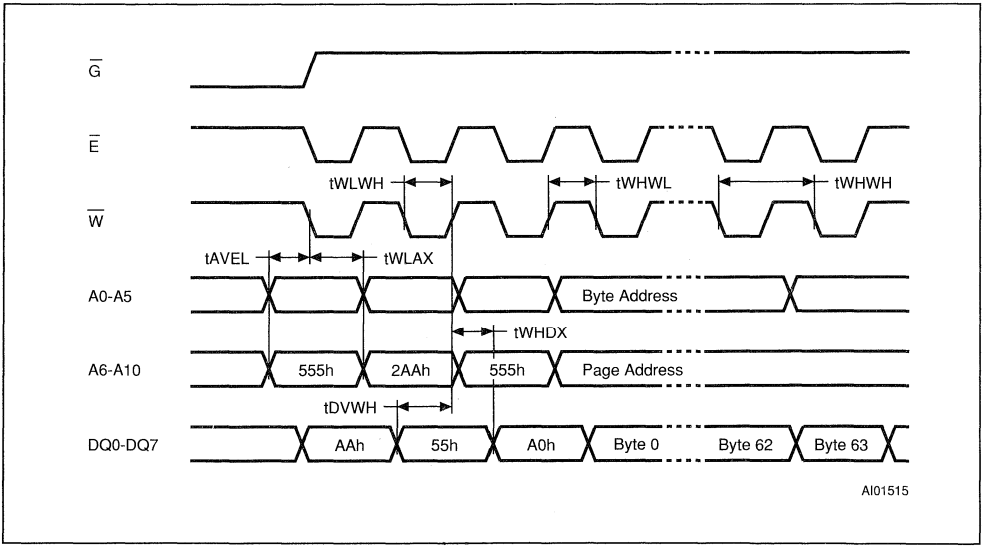


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A10 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Waveforms Sequence

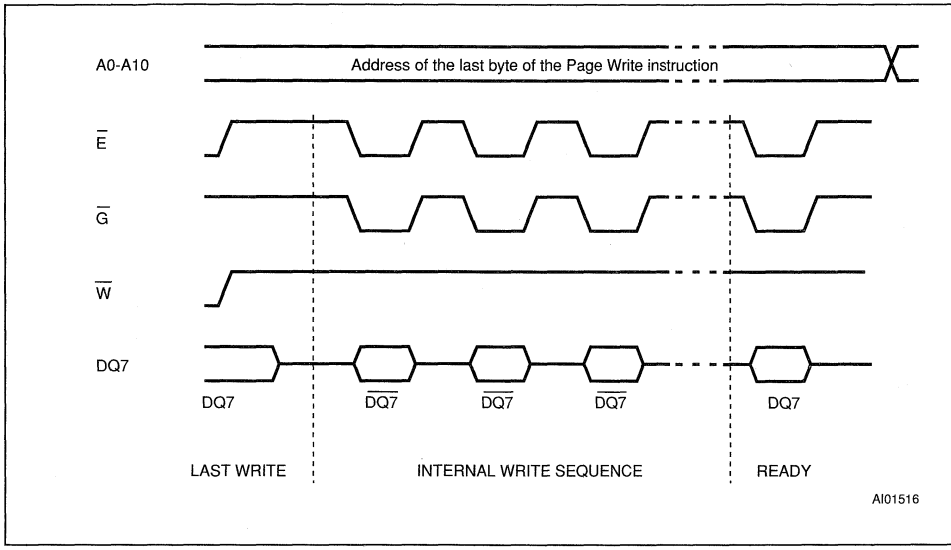
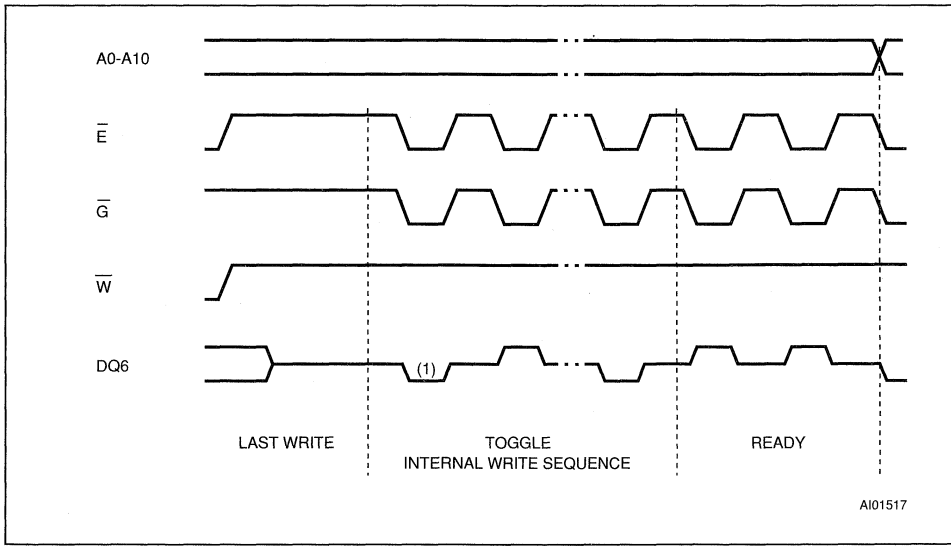


Figure 15. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

Figure 16. Chip Erase Wavforms

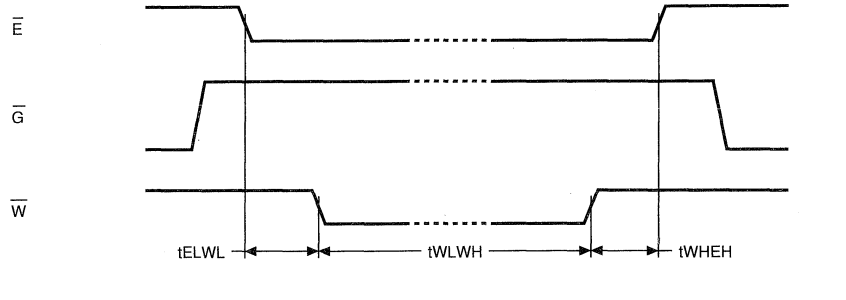


Table 9. Chip Erase AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = 12V	5		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = 12V	5		µs
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{G}$ = 12V	10		ms

ORDERING INFORMATION SCHEME

Example: M28C17 -70 K 1

Speed		Package		Temperature Range	
-70	70ns	P	PDIP28	1	0 to 70 °C
-90	90ns	K	PLCC32	3 *	–40 to 125 °C
-120	120ns	MS	SO28 300mils	6	–40 to 85 °C
-150	150ns				

Note: 3 * Temperature range on special request only.

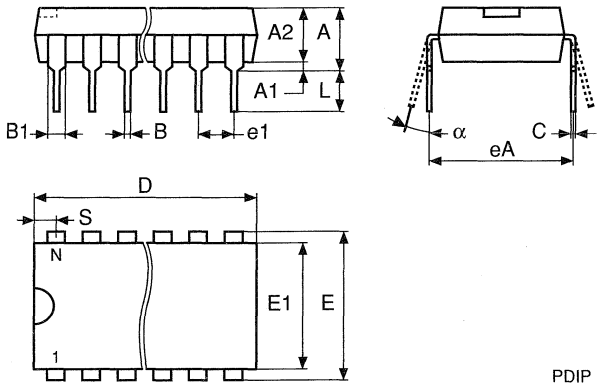
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



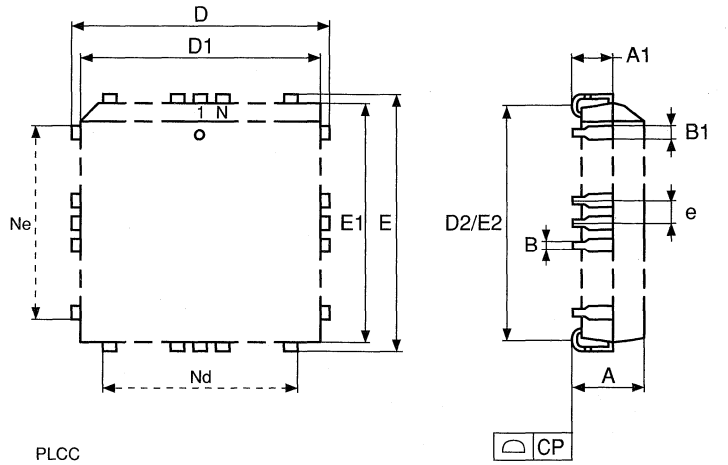
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

PLCC32

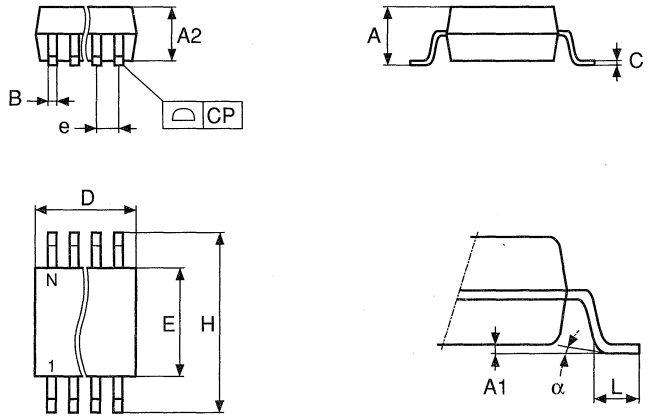


Drawing is out of scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SO28



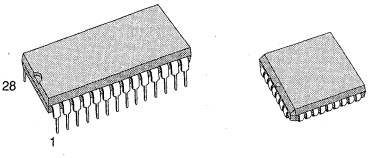
SO-b

Drawing is out of scale

LOW VOLTAGE PARALLEL ACCESS 64K (8K x 8) EEPROM

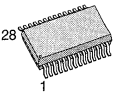
PRODUCT PREVIEW

- FAST ACCESS TIME: 150ns
- SINGLE 3V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION:
  - Active Current 8mA
  - Standby Current 50µA
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle: 3ms Max
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP
- SOFTWARE DATA PROTECTION

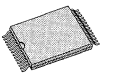


PDIP28 (P)

PLCC32 (K)

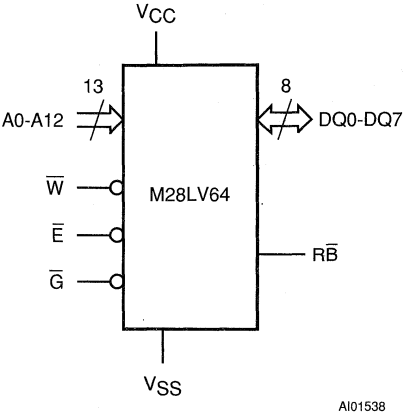


SO28 (MS)
300 mils



TSOP28 (N)
8 x13.4mm

Figure 1. Logic Diagram



DESCRIPTION

The M28LV64 is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 3V ± 10% power supply.

Table 1. Signal Names

A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

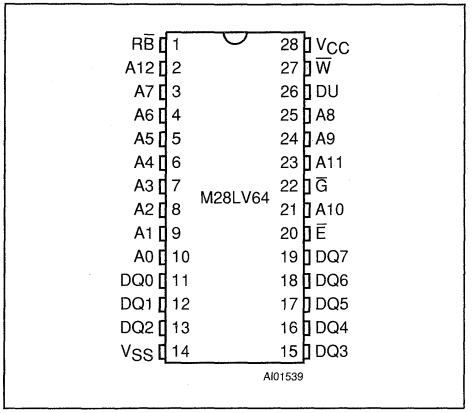
Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 3 grade 6	0 to 70 – 40 to 125 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

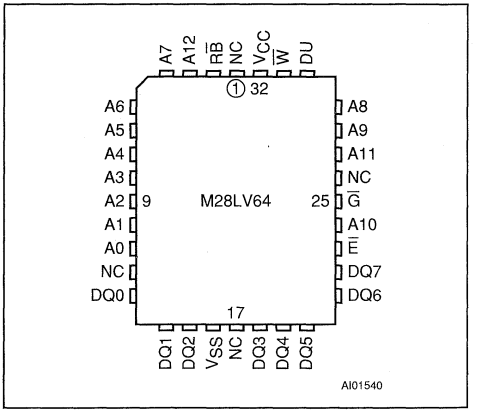
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7

Figure 2A. DIP Pin Connections



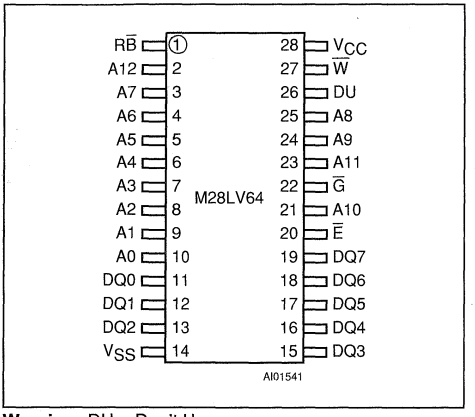
Warning: DU = Don't Use

Figure 2B. LCC Pin Connections



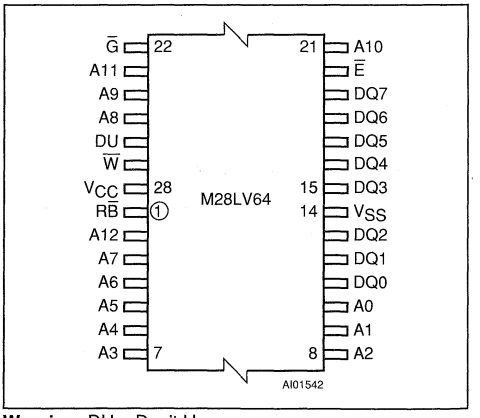
Warning: NC = No Connections, DU = Don't Use

Figure 2C. SO Pin Connections



Warning: DU = Don't Use

Figure 2D. TSOP Pin Connections



Warning: DU = Don't Use

Figure 3. Block Diagram

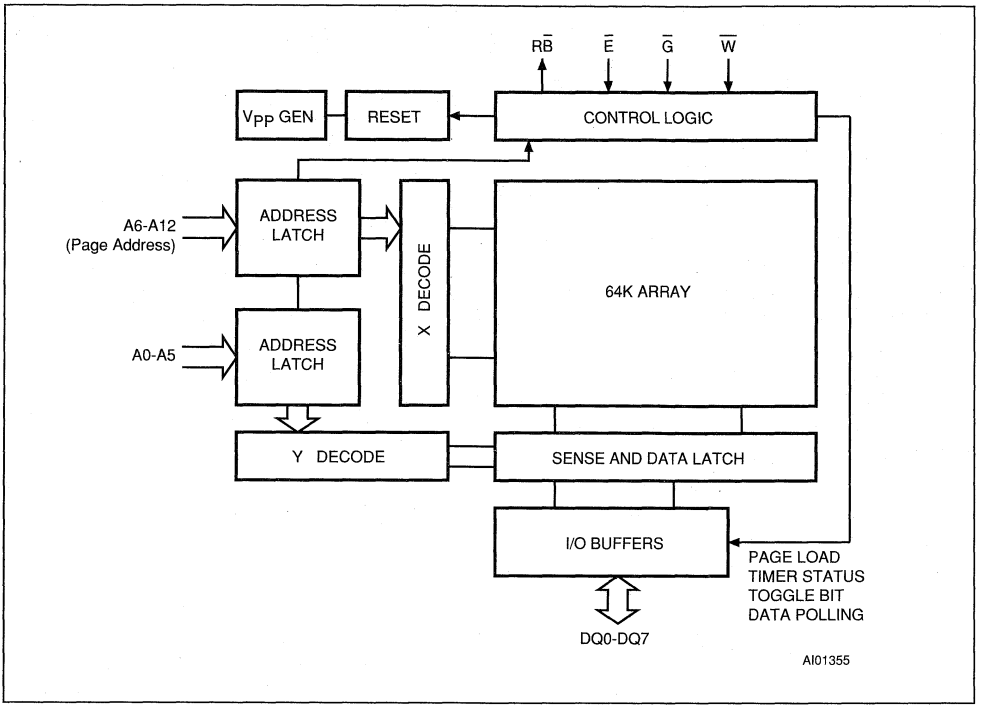


Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z
Chip Erase	V_{IL}	V_{IH} (2)	V_{IL}	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}
2. V_{IH} = 12V ± 5%

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28LV64 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28LV64 through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28LV64.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28LV64 is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28LV64 supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 64 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A12 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data up to a maximum of 100µs after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{BLC}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within 100µs, the internal programming cycle will start.

Chip Erase

The contents of the entire memory may be erased (FF) by use of the Chip Erase command by setting Chip Enable ($\overline{E}$) Low and Output Enable ($\overline{G}$) to 12V. The chip is cleared when a 10ms low pulse is applied to the Write Enable pin.

Microcontroller Control Interface

The M28LV64 provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the $R\overline{B}$ signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28LV64 also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$. Up to 64 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The $R\overline{B}$ pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

Figure 5. Software Data Protection Enable Algorithm and Memory Write

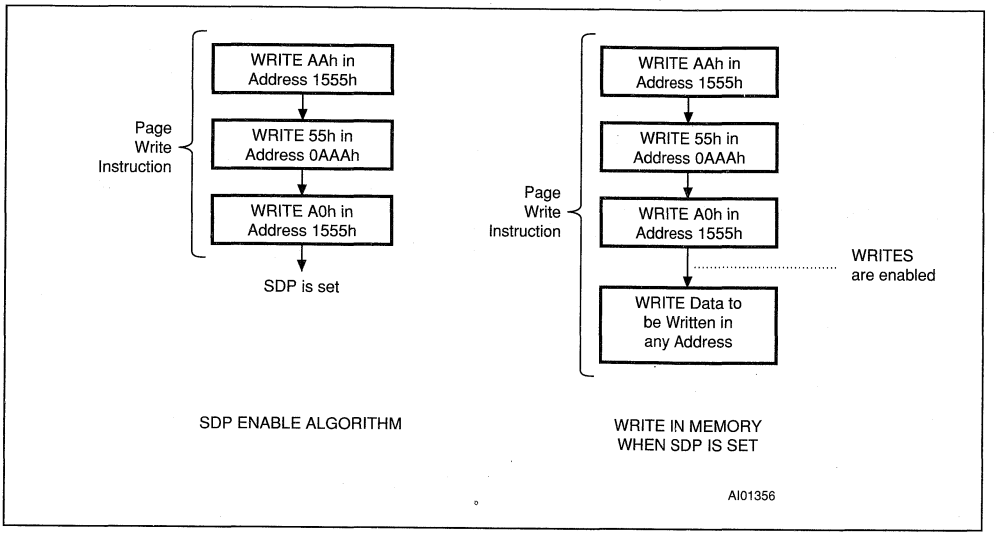
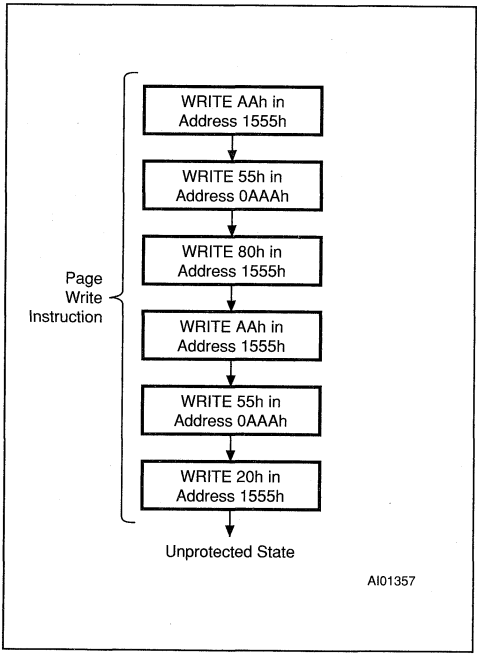


Figure 6. Software Data Protection Disable Algorithm



Software Data Protection

The M28LV64 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device including the Chip Erase instruction. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28LV64 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents. The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences.

To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write) three specific data bytes to three specific memory locations as per Figure 5. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 6 (with a Page Write). This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0V to V_{CC} -0.3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

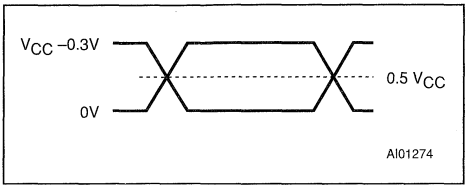


Figure 8. AC Testing Equivalent Load Circuit

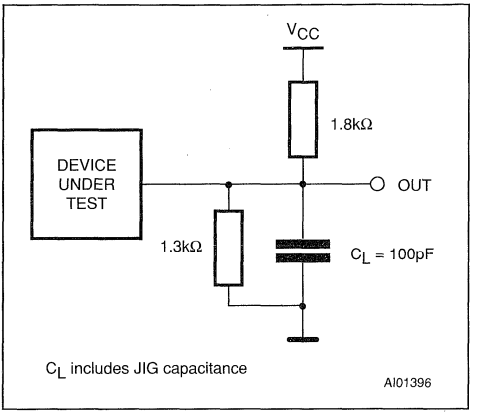


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		8	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 1 mA	0.8 V_{CC}		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

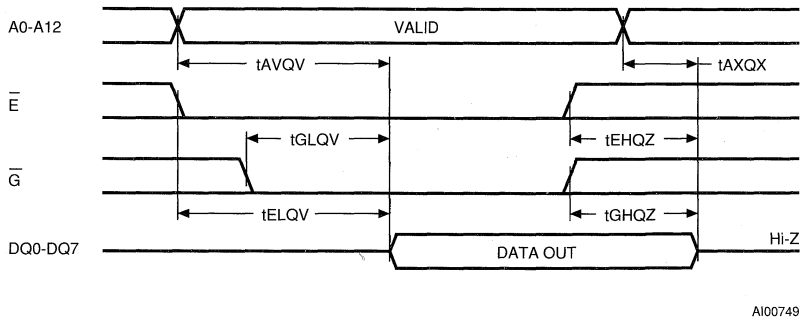
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28LV64						Unit
				-150		-200		-300		
				min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		80		95		150	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	45	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 9. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50	1000	ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.15	100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			3	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		50	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

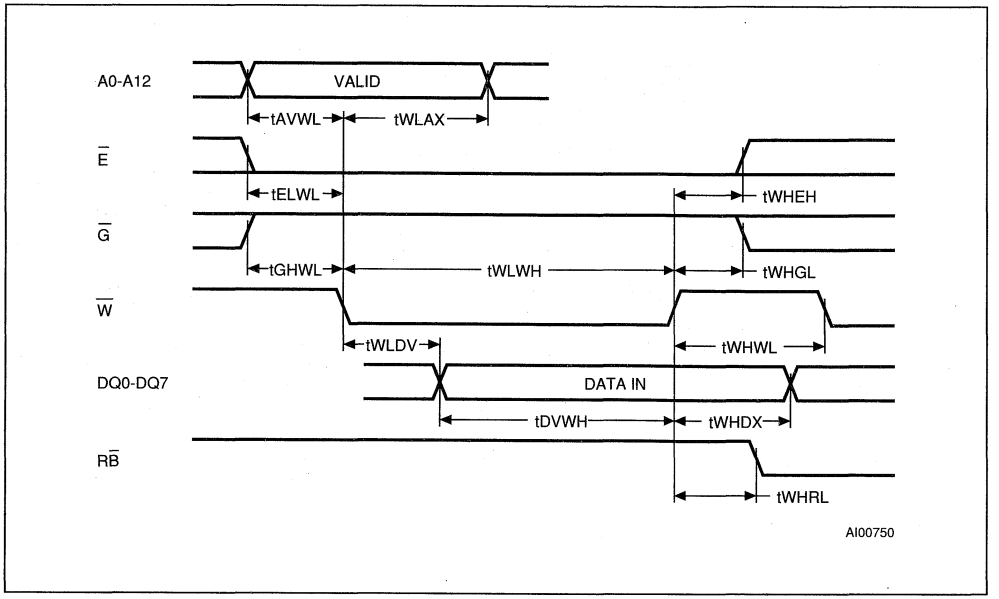


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

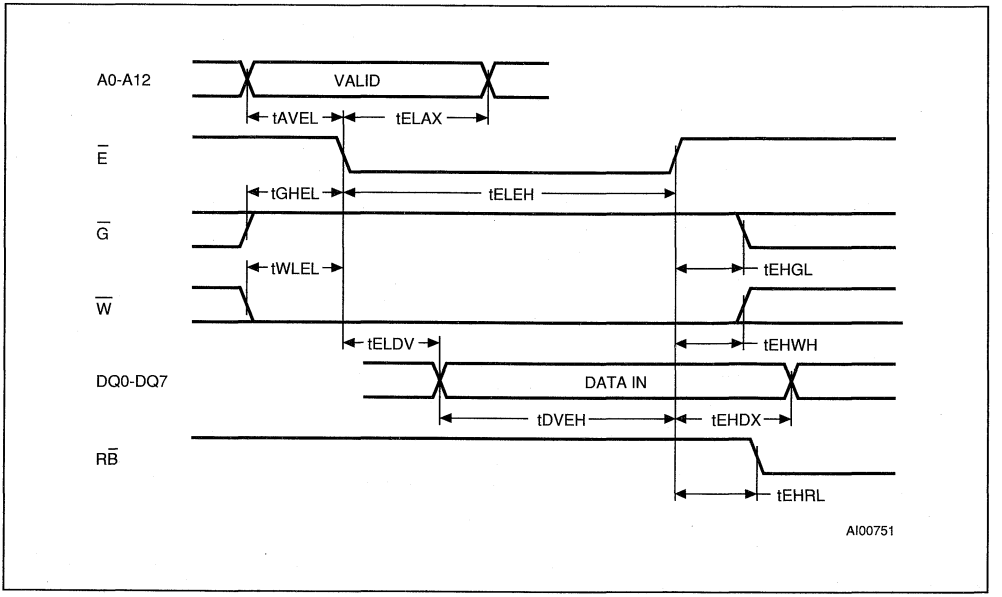


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

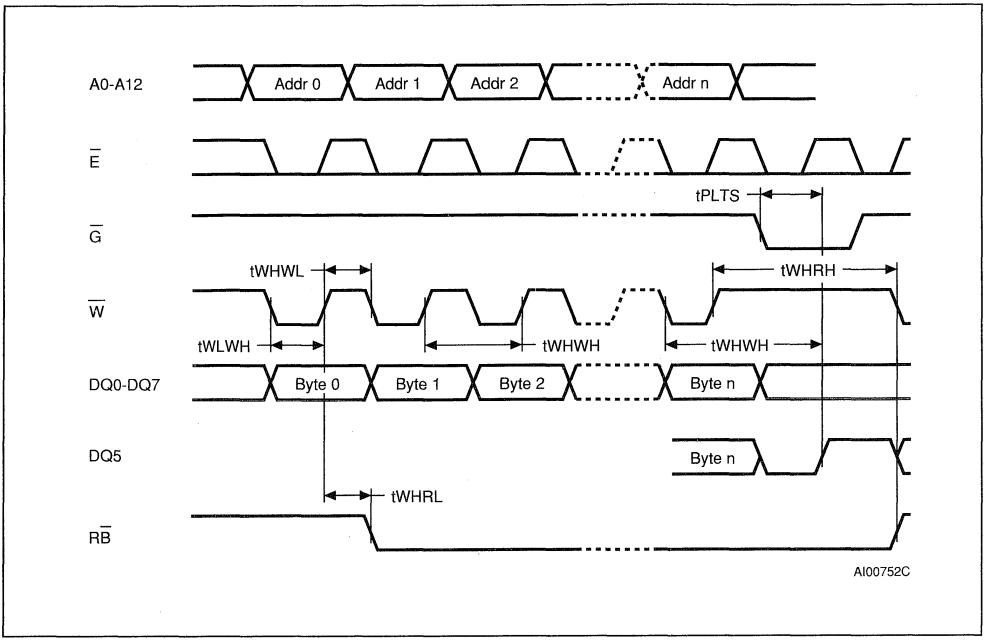
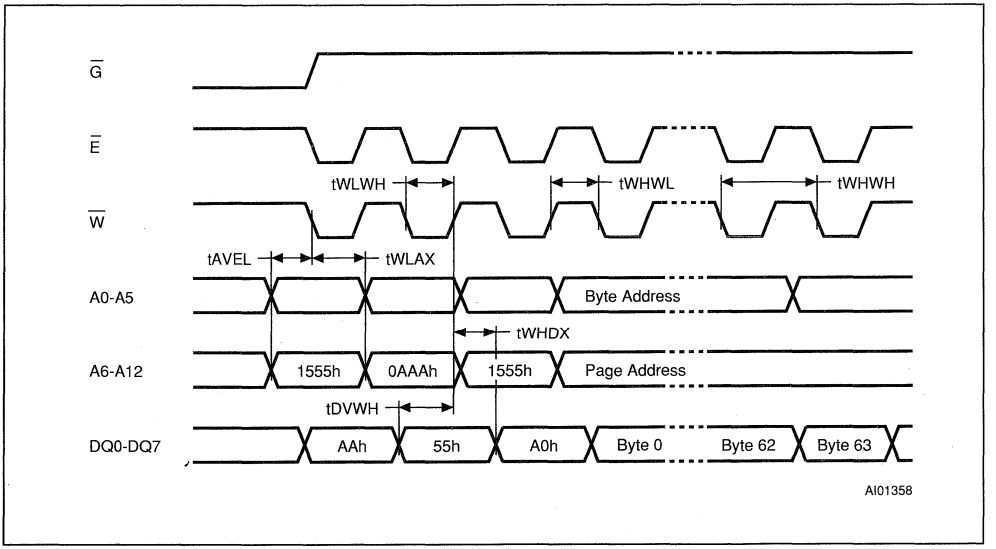


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A12 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Waveforms Sequence

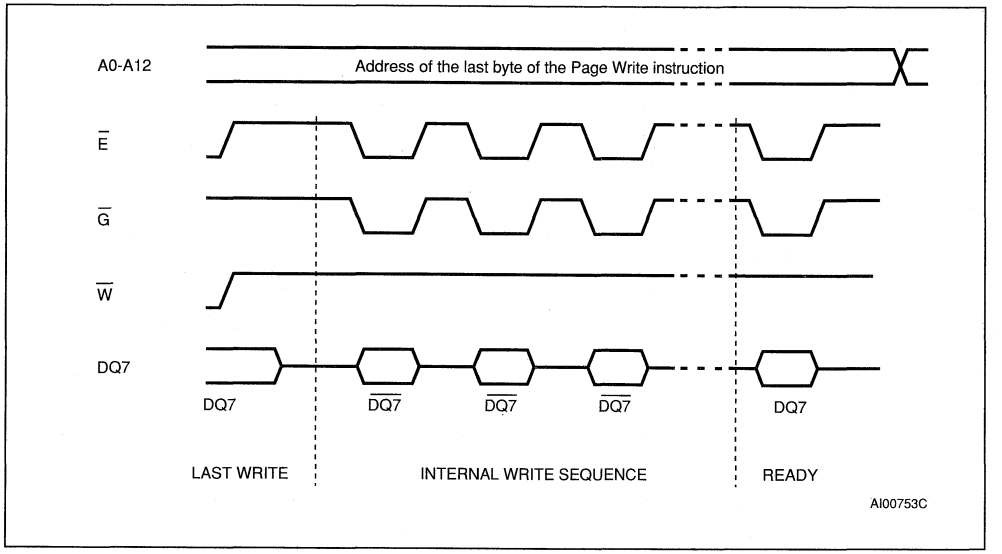
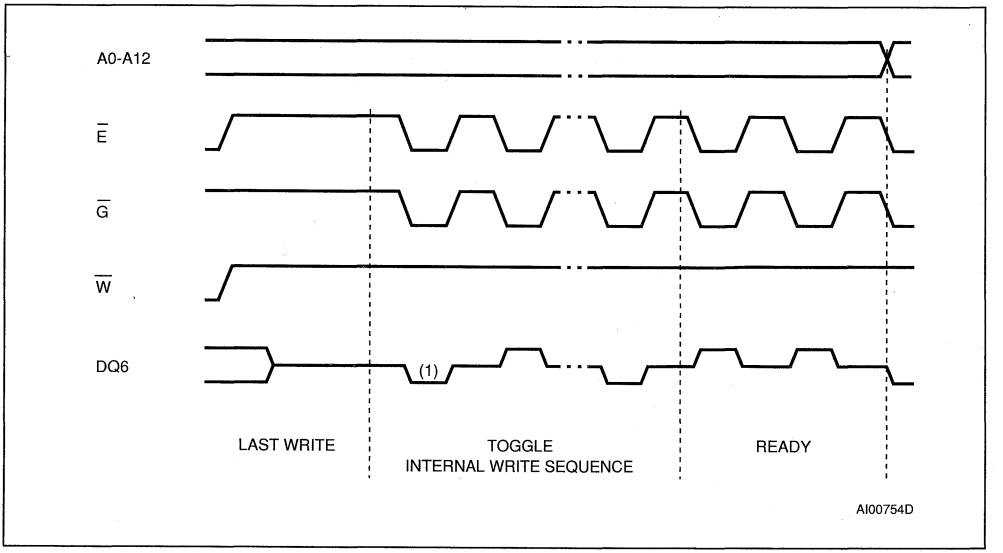


Figure 15. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

Figure 16. Chip Erase AC Waveforms

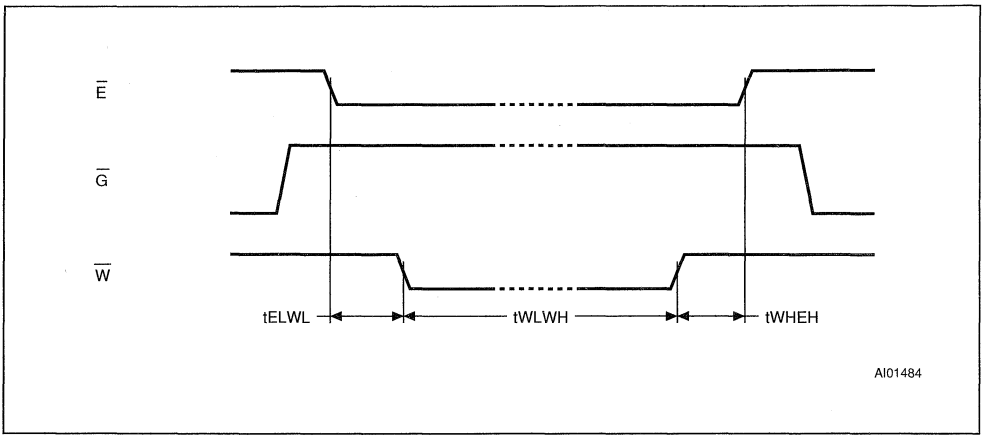


Table 9. Chip Erase AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C, V_{CC} = 2.7V to3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = 12V	5		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = 12V	5		µs
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{G}$ = 12V	10		ms

ORDERING INFORMATION SCHEME

Example: M28LV64 -200 K 1

Speed		Package		Temperature Range	
-150	150ns	P	PDIP28	1	0 to 70 °C
-200	200ns	K	PLCC32	3 *	–40 to 125 °C
-300	300ns	MS	SO28 300 mils	6	–40 to 85 °C
		N	TSOP28 8 x 13.4mm		

Note: 3 * Temperature range on special request only.

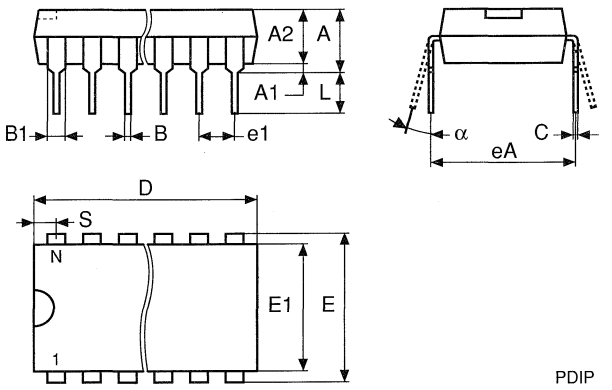
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



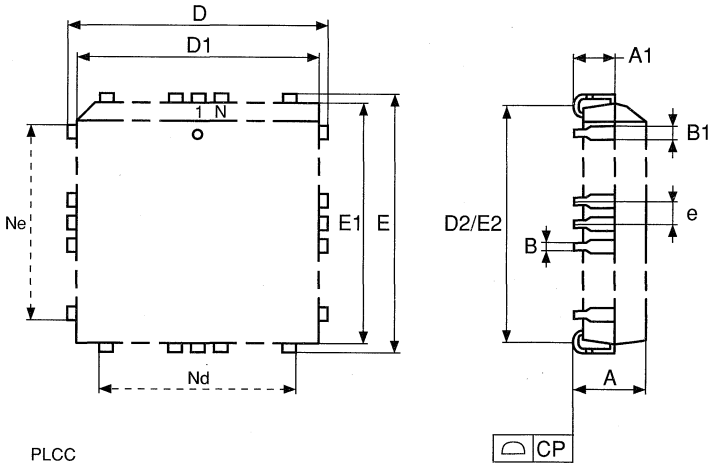
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



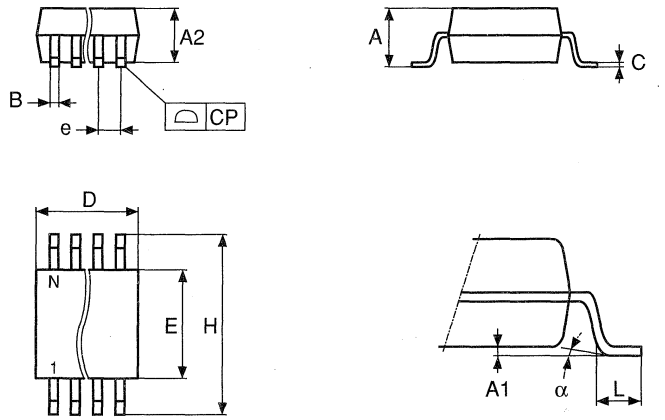
PLCC

Drawing is out of scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SO28



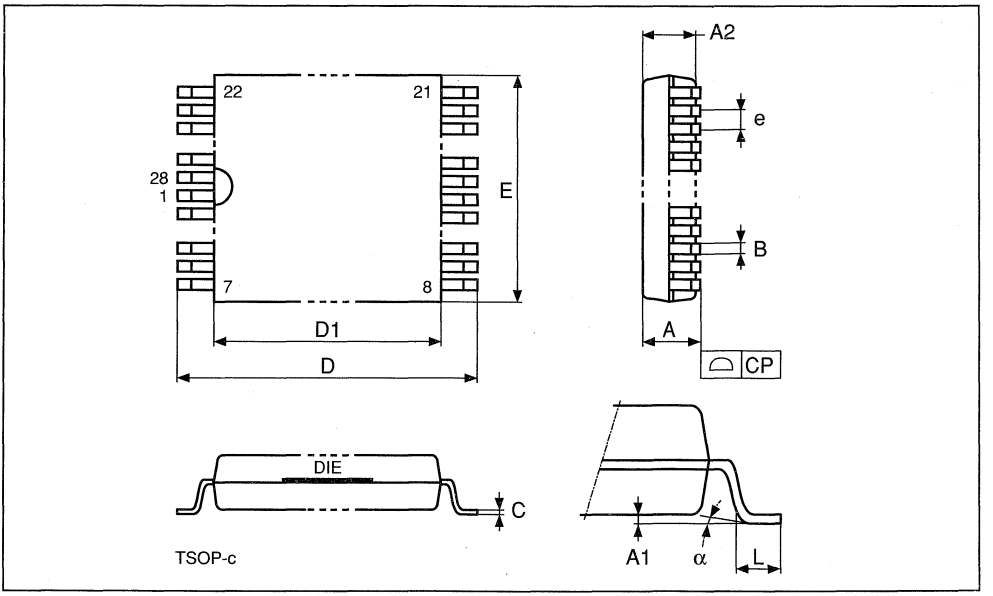
SO-b

Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		28			28	
CP			0.10			0.004

TSOP28

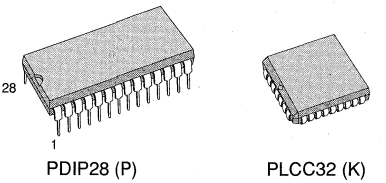


Drawing is out of scale

LOW VOLTAGE PARALLEL ACCESS 64K (8K x 8) EEPROM

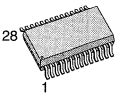
PRELIMINARY DATA

- FAST ACCESS TIME: 150ns
- SINGLE 3.3V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION
  - Active Current 15mA
  - Standby Current 50µA
- FAST WRITE CYCLE
  - 32 Bytes Page Write Operation
  - Byte or Page Write Cycle: 10ms
- ENHANCED END OF WRITE DETECTION
  - Ready/Busy Open Drain Output (for M28LV64C product only)
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABLITY SINGLE POLYSILICON, CMOS TECHNOLOGY
  - Endurance > 100,000 Erase/Write Cycles
  - Data Retention > 10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP

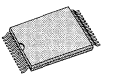


PDIP28 (P)

PLCC32 (K)

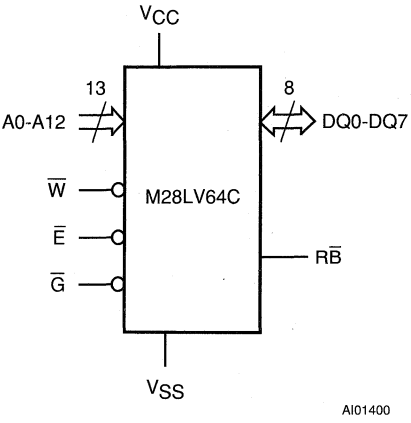


SO28 (MS)
300 mils



TSOP28 (N)
8 x13.4mm

Figure 1. Logic Diagram



DESCRIPTION

The M28LV64C is an 8K x 8 low power EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 3.3V power supply.

Table 1. Signal Names

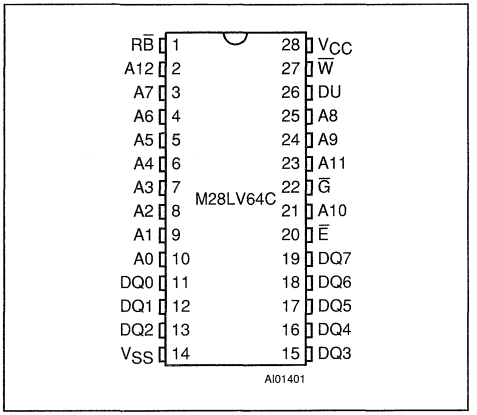
A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature:	grade 1 grade 6	0 to 70 – 40 to 85	°C
T_{STG}	Storage Temperature Range		– 65 to 150	°C
V_{CC}	Supply Voltage		– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage		– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage		– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)		2000	V

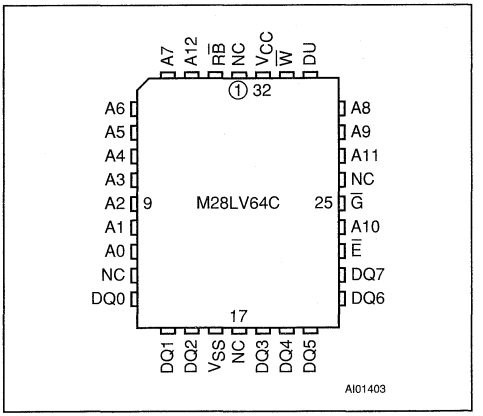
Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2A. DIP Pin Connections



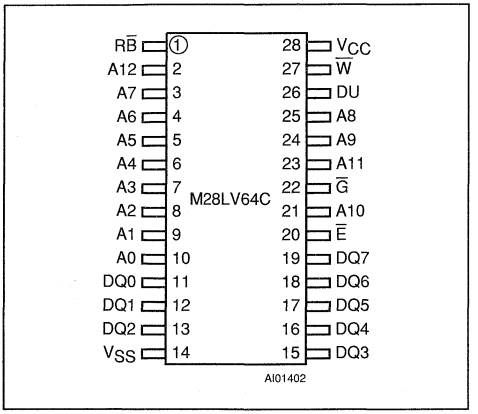
Warning: DU = Don't Use

Figure 2B. LCC Pin Connections



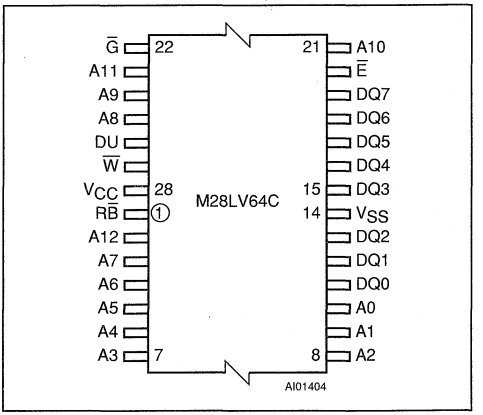
Warning: NC = No Connections, DU = Don't Use

Figure 2C. SO Pin Connections



Warning: DU = Don't Use

Figure 2D. TSOP Pin Connections



Warning: DU = Don't Use

Figure 3. Block Diagram

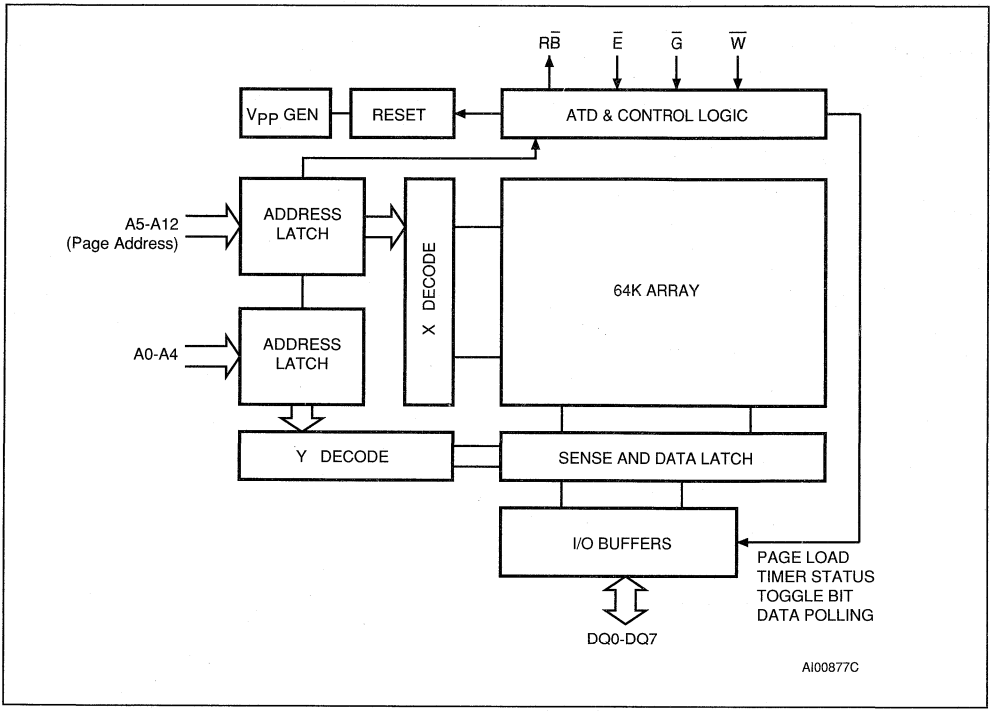


Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking mode with Ready/Busy, Data Polling and Toggle Bit. The M28LV64C supports 32 byte page write operation.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28LV64C through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28LV64C.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28LV64C is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The M28LV64C supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5-A12 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. If a transition of $\overline{E}$ or $\overline{W}$ is not detected within t_{WHWH}, the internal programming cycle will start.

Microcontroller Control Interface

The M28LV64C provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the $R\overline{B}$ signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28LV64C also offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any address in the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low. DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The $R\overline{B}$ pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0V to V_{CC} -0.3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input Output Waveforms

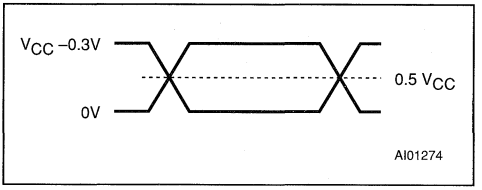


Figure 6. AC Testing Equivalent Load Circuit

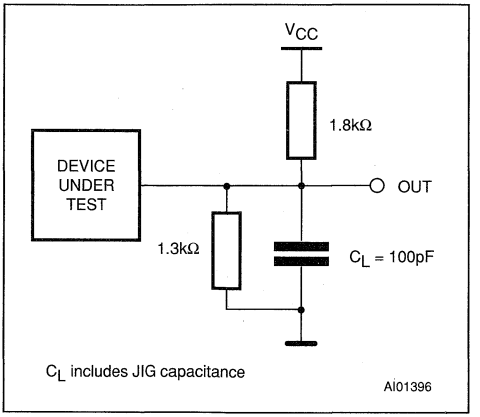


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 3V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		15	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.3	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2		V

Note: 1. All I/O's open.

Table 6. Power Up Timing (1) (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 3V to 3.6V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

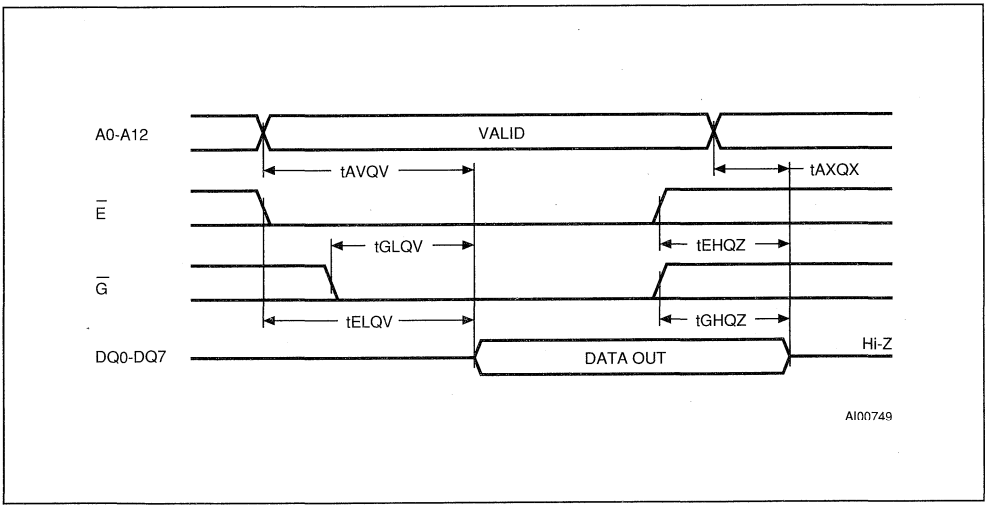
Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 3V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28LV64C						Unit
				-150		-200		-300		
				min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100		150	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. Read Mode AC Waveforms



Note: $\overline{W}$ = High

Table 8. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 3V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		150		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		150		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		150		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		150		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		10		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		10		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.35	50	µs
t_{WHRH}	t_{WC}	Write Cycle Time			10	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		100		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

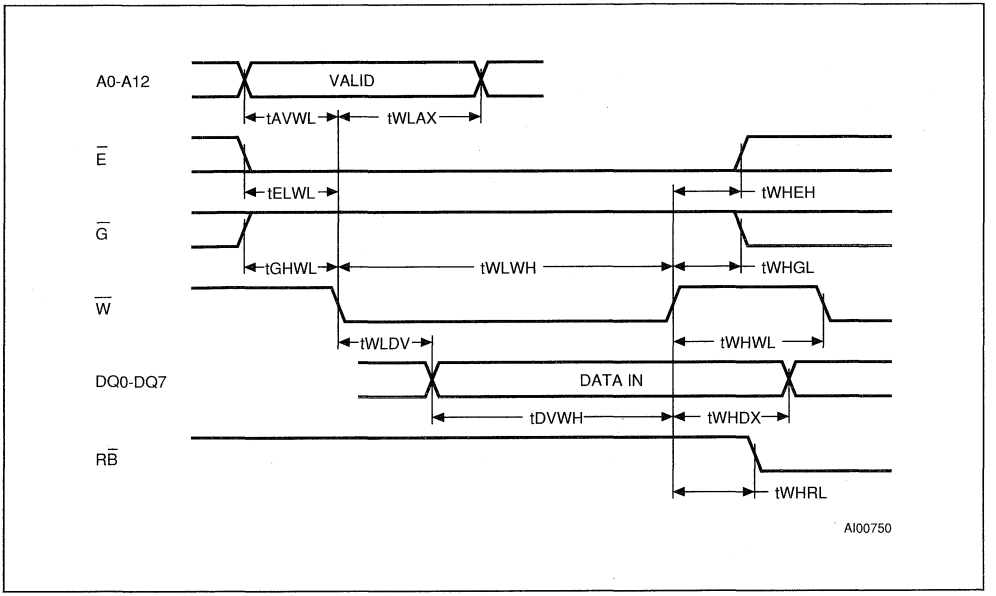


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

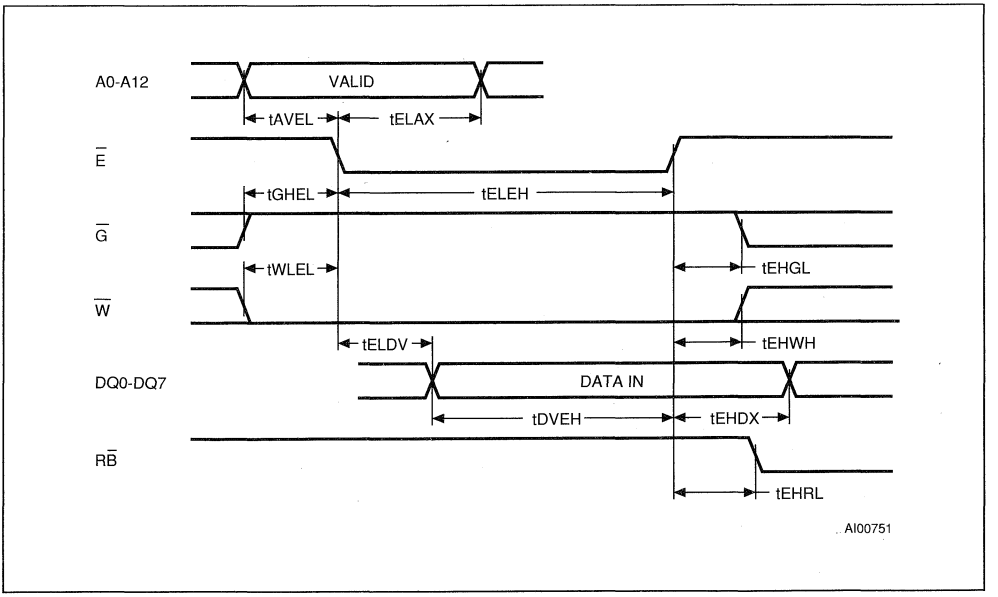


Figure 10. Page Write Mode AC Waveforms - Write Enable Controlled

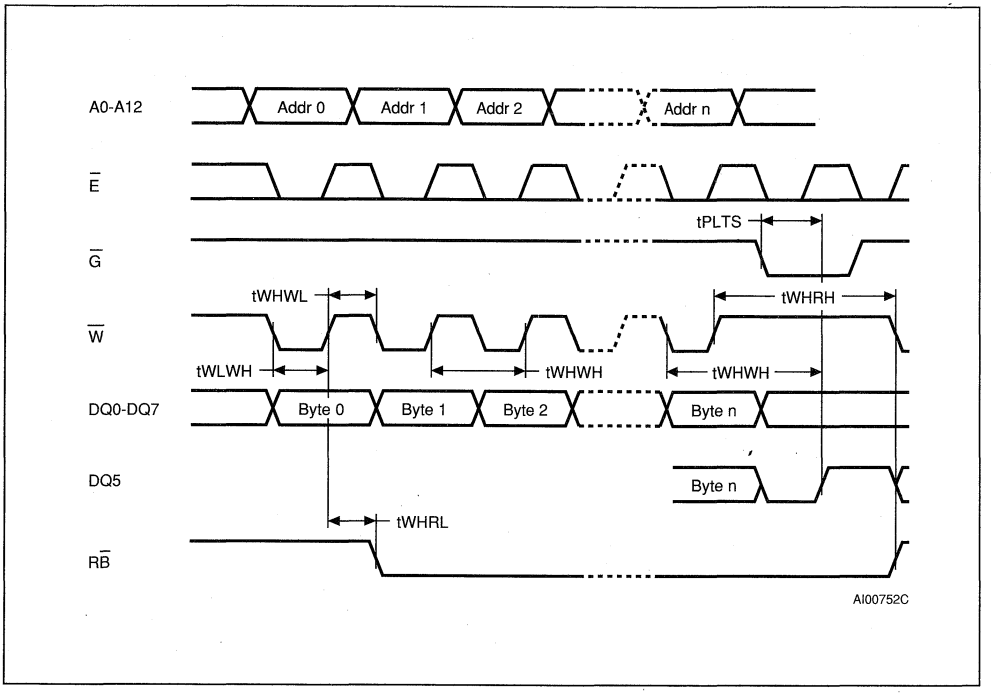


Figure 11. Data Polling Waveforms Sequence

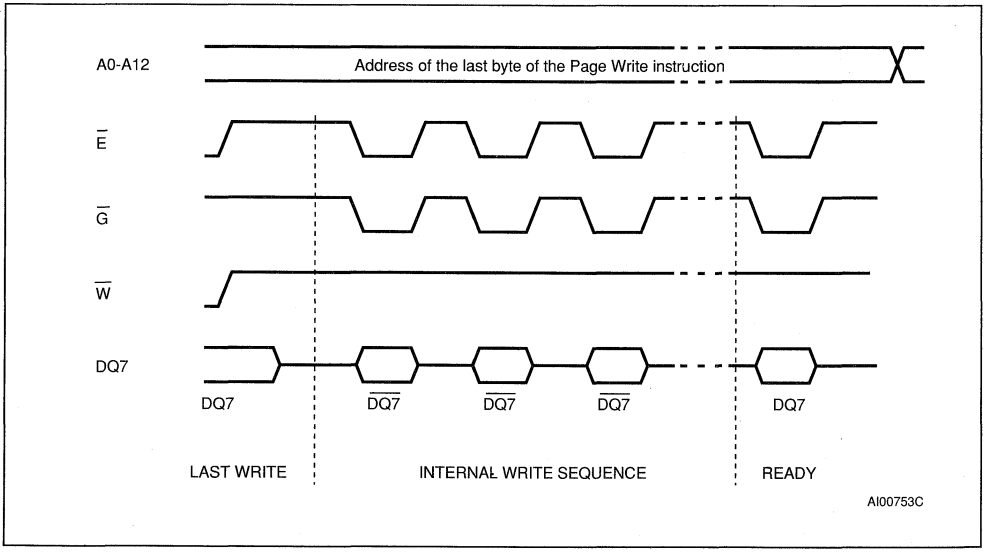
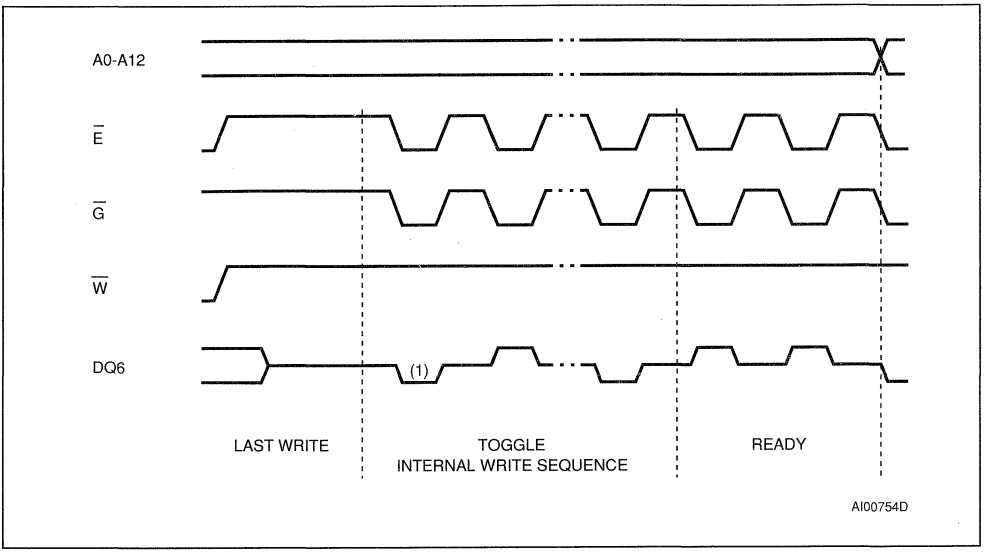


Figure 12. Toggle Bit Waveforms Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME

Example: M28LV64C -200 K 1

Version	Speed	Package	Temperature Range
C RB available	-150 150 ns	P PDIP28	1 0 to 70 °C
X RB not bonded (pin NC)	-200 200 ns	K PLCC32	6 –40 to 85 °C
	-300 300 ns	MS SO28 300 mils	
		N TSOP28 8 x 13.4mm	

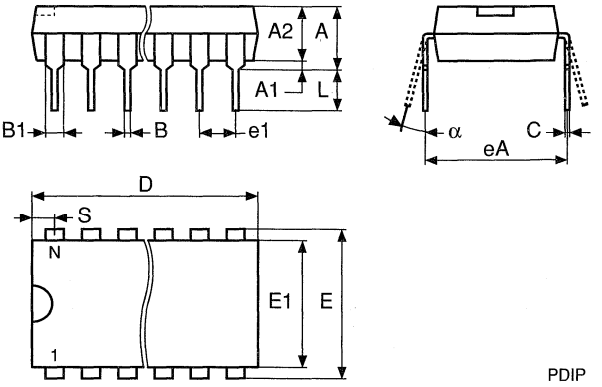
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



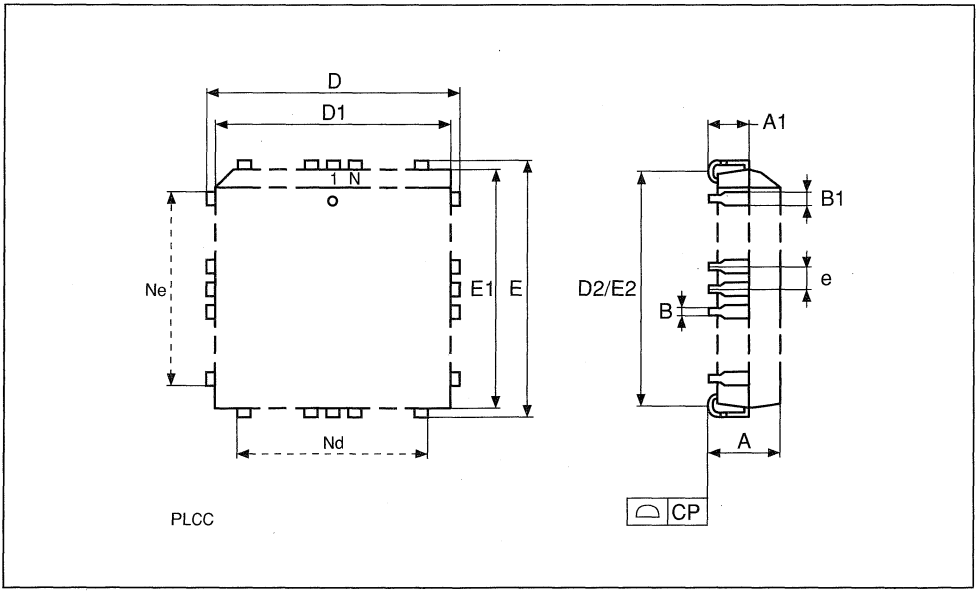
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

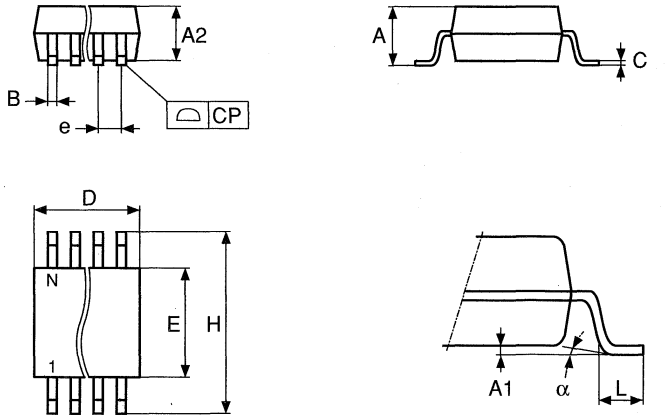


Drawing is out of scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SO28



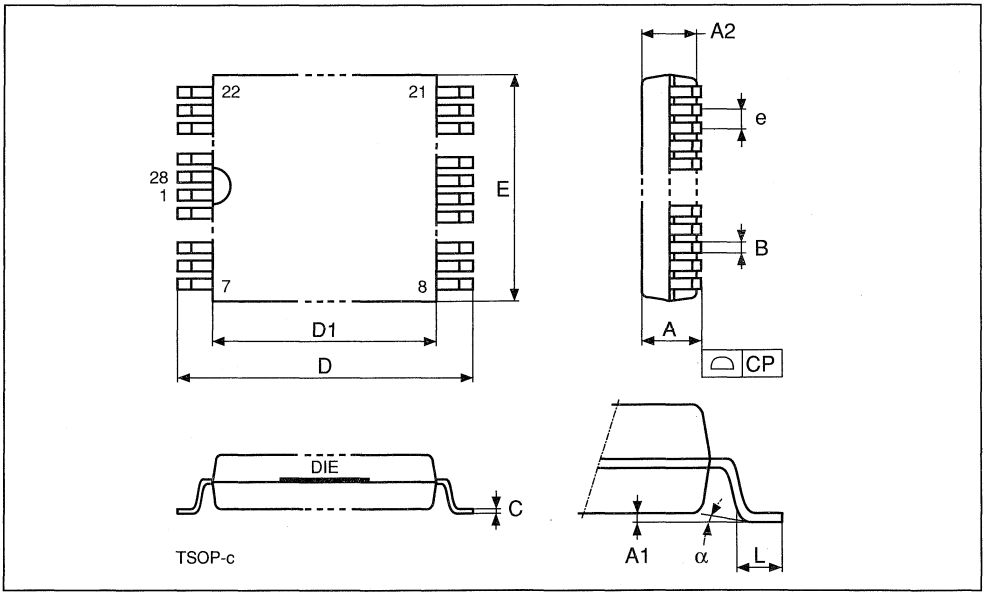
SO-b

Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0 °	5 °		0 °	5 °
N	28			28		
CP			0.10			0.004

TSOP28



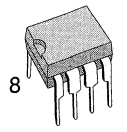
Drawing is out of scale

DEDICATED EEPROM

SERIAL ACCESS 1K (128 x 8) EEPROM

PRODUCT PREVIEW

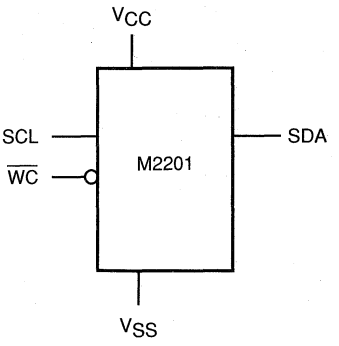
- 100.000 ERASE/WRITE CYCLES with 10 YEARS DATA RETENTION
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- HARDWARE WRITE CONTROL
- TWO WIRE SERIAL INTERFACE
- 400K BIT TRANSFER RATE
- BYTE WRITE
- PAGE WRITE (up to 4 BYTES)
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The M2201 is a 1K bit electrically erasable programmable memory (EEPROM), organized as 128 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees a data retention of over 10 years.

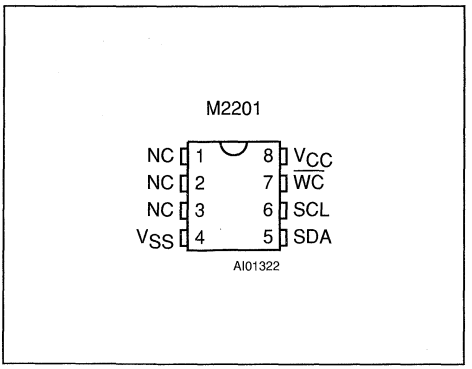
Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memory is compatible with a two wire serial interface which uses a bi-directional data bus and serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by 7 bits of address, plus one read/write bit and terminated by an acknowledge bit.

Table 1. Signal Names

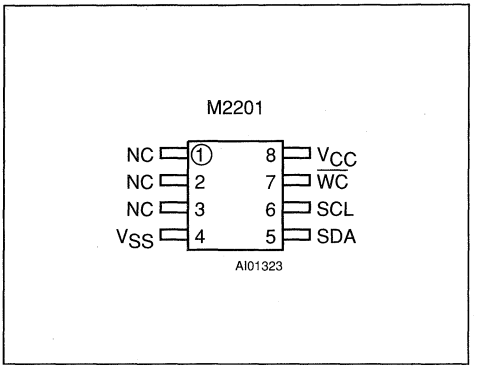
SDA	Serial Data Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1	0 to 70	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} ($\overline{WC}$ is disabled).

DEVICE OPERATION

The device that controls the data transfer is known as the master. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The M2201 is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the M2201 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the M2201 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the M2201 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

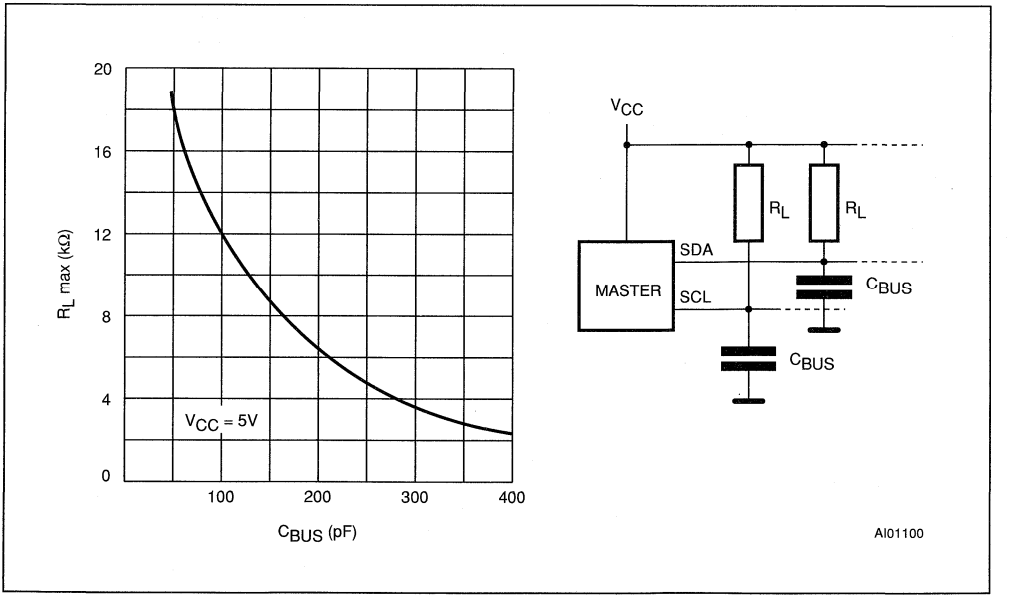


Table 3. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
I_{CC1}	Supply Current (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V

Table 5. AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

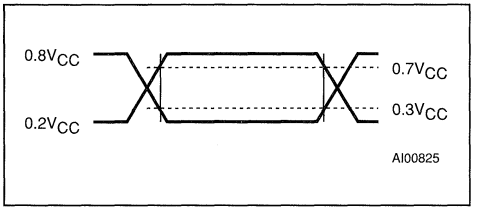
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL1} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms

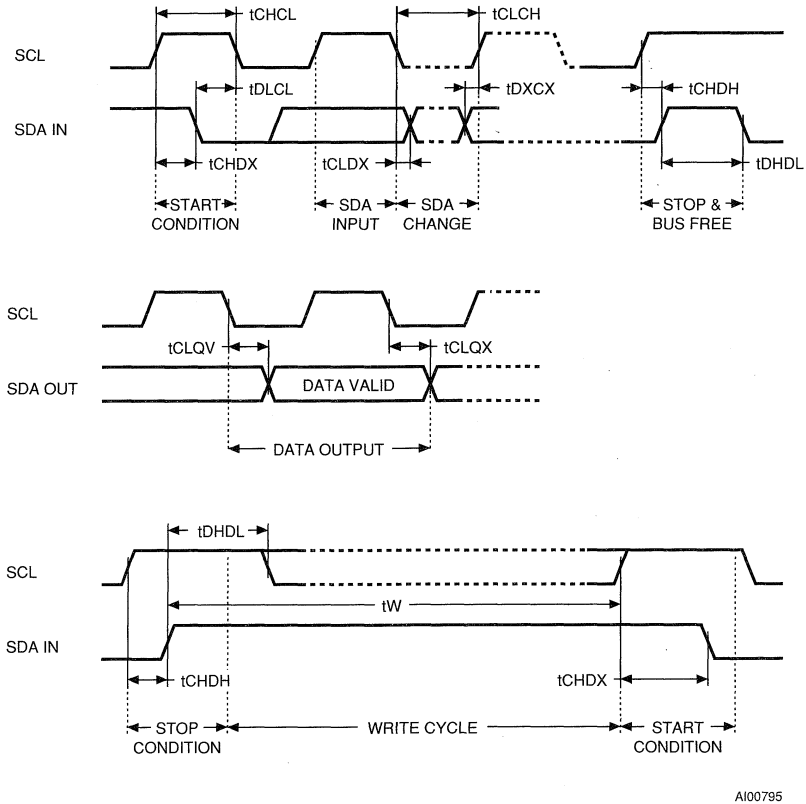


Memory Addressing. To start communication between the bus master and the slave M2201, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the 7th bit byte-address and a READ or WRITE bit. This 8th bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

Following a START condition the master sends the byte address with the RW bit reset to '0'. The memory acknowledges this and waits for a data byte. Any write command with $\overline{WC}$ = 1 (during a period of time from the START condition untill the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 8.

Figure 5. AC Waveforms



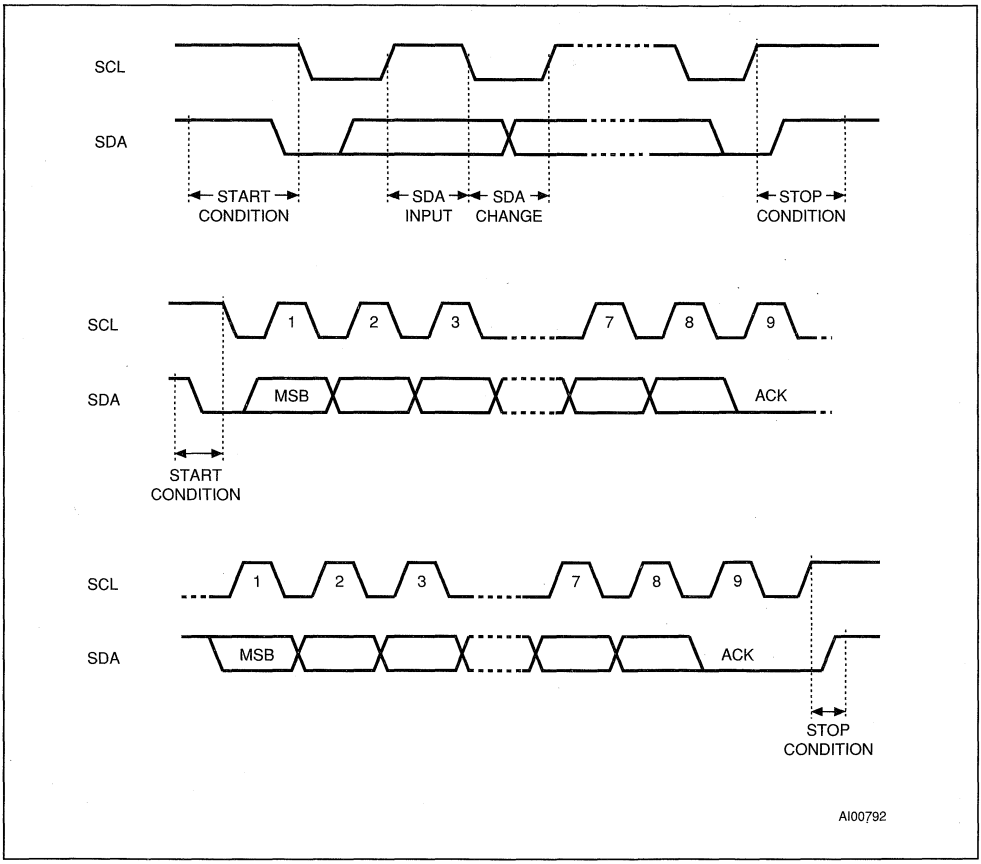
Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 4 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A6-A2) are the same. The master sends from one up to four bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (2 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

It must be noticed that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be re-

Figure 6. I^2C Bus Protocol

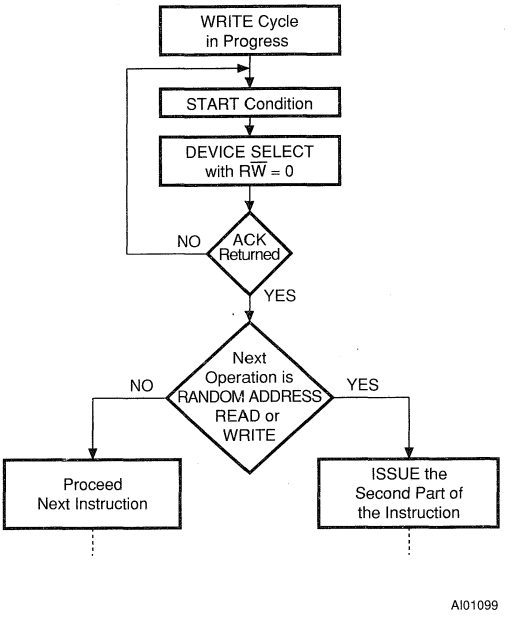


DEVICE OPERATION (cont'd)

duced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Figure 7. Write Cycle Polling using ACK



Read Operation

Byte Read. The master sends a START condition followed by seven bits of address and the R/W bit (set to '1'). The M2201 acknowledges it and outputs the corresponding data byte. The read operation is terminated by a STOP condition issued by the master (instead of the ACK bit).

Sequential Read. The master sends a START condition followed by seven bits of address and the R/W bit (set to '1'). The M2201 acknowledges it and outputs the corresponding data byte. The master does acknowledge this byte and reads the next data byte (at address + 1). The read operation is terminated by a STOP condition issued by the master (instead of the ACK bit). The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over to address '00' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the M2201 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the M2201 terminates the data transfer and switches to a standby state.

Figure 8. Write Modes Sequences with Write Control = 1

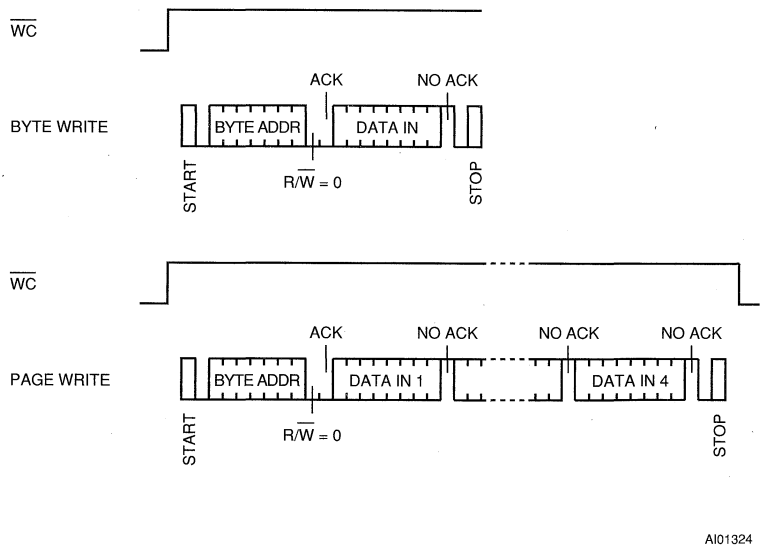
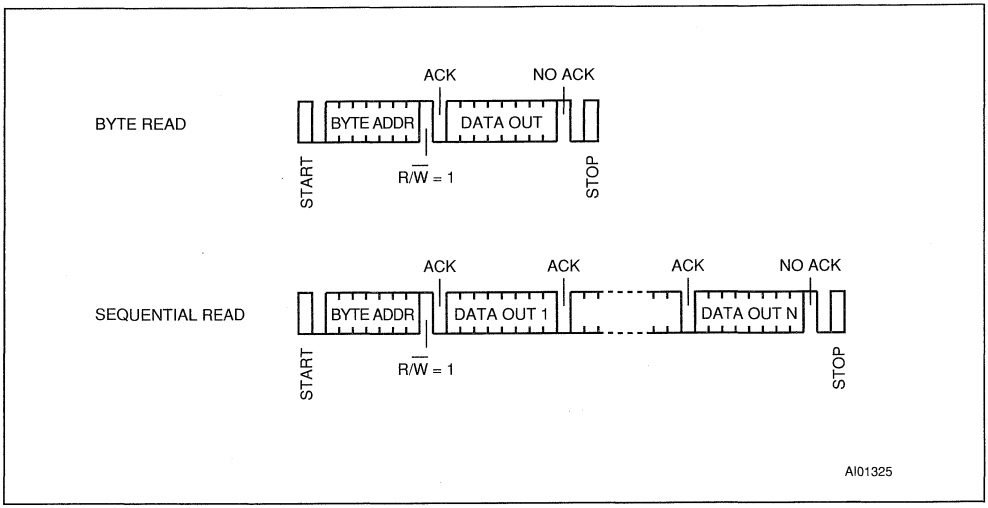
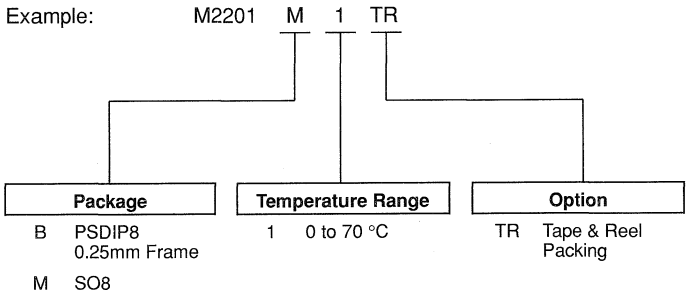


Figure 9. Read Modes Sequences



ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFh).

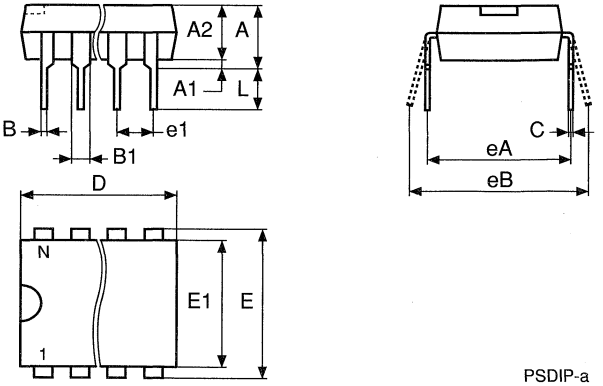
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



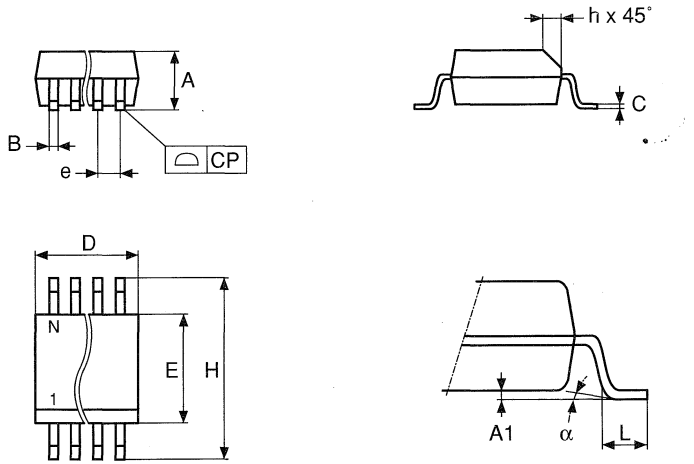
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8

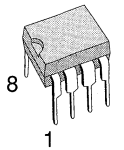


SO-a

Drawing is out of scale

SERIAL ACCESS 16K (2K x 8) EEPROM

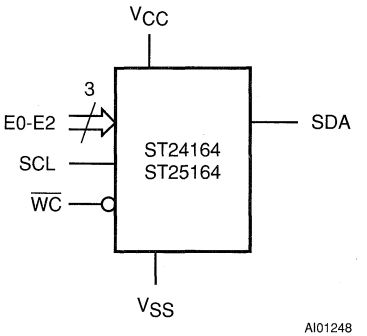
- 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24164 version
  - 2.5V to 5.5V for ST25164 version
- HARDWARE WRITE CONTROL PIN
- TWO WIRE SERIAL INTERFACE
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



DESCRIPTION

The ST24/25164 are 16K bit electrically erasable programmable memories (EEPROM), organized as 2048 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

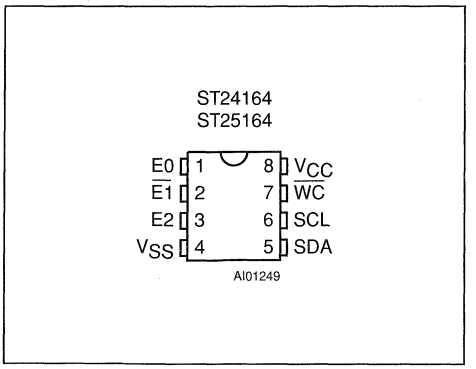


Figure 2B. SO Pin Connections

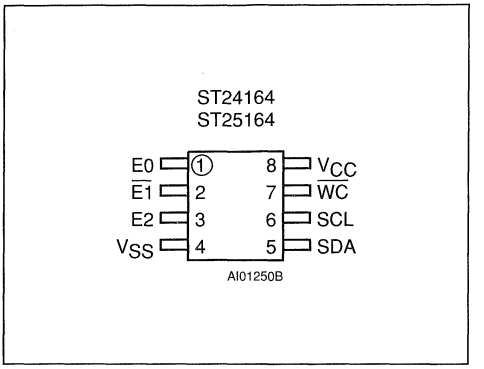


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the two wire serial interface which uses a bi-directional data bus and serial clock. The memories offer 3 chip enable inputs (E2, $\overline{E1}$, E0) so that up to 8 x 16K devices may be attached to the bus and selected individually. The memories behave as a slave device with all memory operations synchronized by the serial clock.

Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits, plus one read/write bit and terminated by an acknowledge bit (see Table 3).

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Table 3. Device Select Code

		Chip Enable			MSB Address			R/$\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	E2	E1	E0	A10	A9	A8	R/$\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	R$\overline{W}$ bit	$\overline{WC}$ pin	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R/$\overline{W}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, R/$\overline{W}$ = '0', Address,
	'1'			reSTART, Device Select, R/$\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 2048	Similar to Current or Random Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, R/$\overline{W}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, R/$\overline{W}$ = '0'

Notes: 1. X = V_{IH} or V_{IL}

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

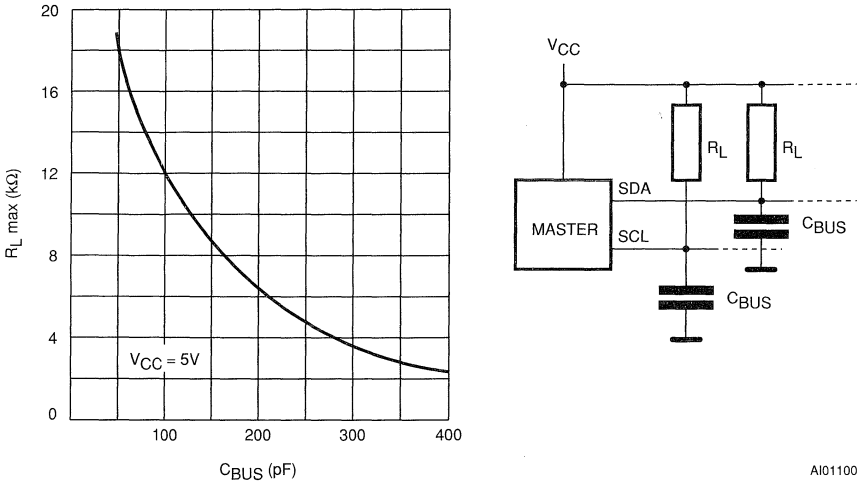
Chip Enable (E2 - E0). These chip enable inputs are used to set 3 bits (b6, b5, b4) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered on pin 7. This feature is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. $\overline{WC}$ pin can be direcly connected to V_{SS} pin, in order to run the ST24/25164 without the Write Control protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} (see Table 5).

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acnowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for a Serial Bus



DEVICE OPERATION

Bus Background

The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25164 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25164 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25164 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25164 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25164, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a Read or Write bit (R/$\overline{W}$).

Three out of the four most significant bits of the Device Select code are the Device Select bits (b6, b5, b4). They are matched to the chip enable signals applied on pins E2, $\overline{E1}$, E0. Thus up to 8 x 16K memories can be connected on the same bus

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, WC)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, WC)		V_{CC} –0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

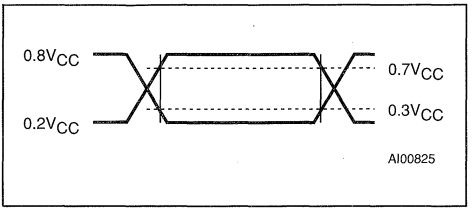
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W	t_{WR}	Write Time		10	ms

Note: 1. For a reSTART condition, or following a write cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

giving a memory capacity total of 128K bits. After a START condition any memory on the bus will identify the device code and compare the 3 bits to its chip enable inputs E2, $\overline{E1}$, E0.

The 8th bit sent is the Read or Write bit (R/$\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

The Write Operations are only possible when the Write Control pin is low ($\overline{WC}$ to ground).

Following a START condition the master sends a device select code with the R$\overline{W}$ bit reset to '0'. The memory acknowledges and waits for the lower byte address. After receipt of the byte address the device again responds with an acknowledge.

Figure 5. AC Waveforms

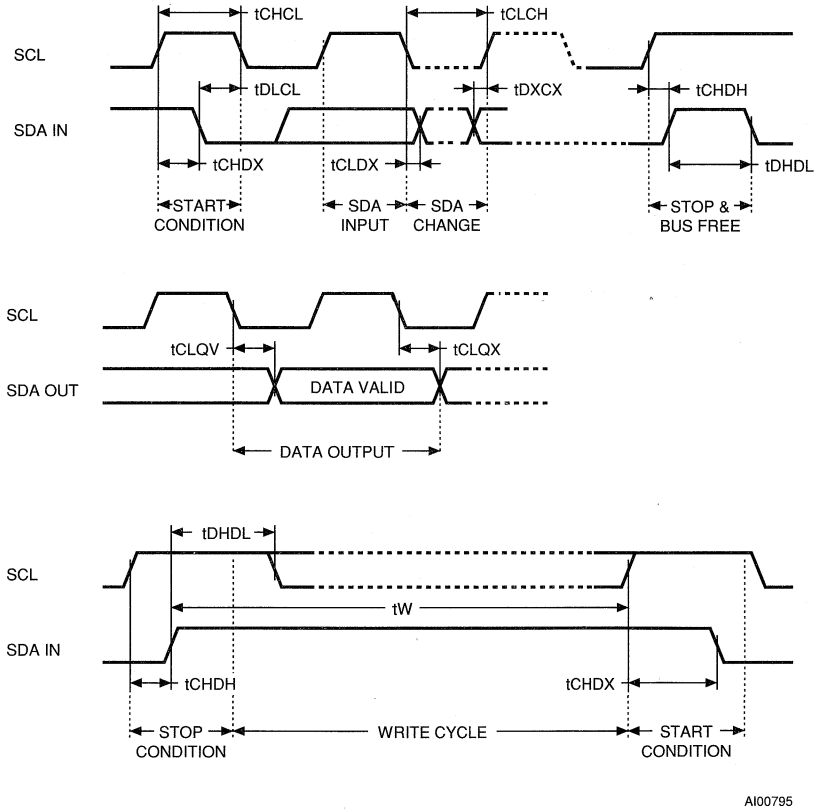
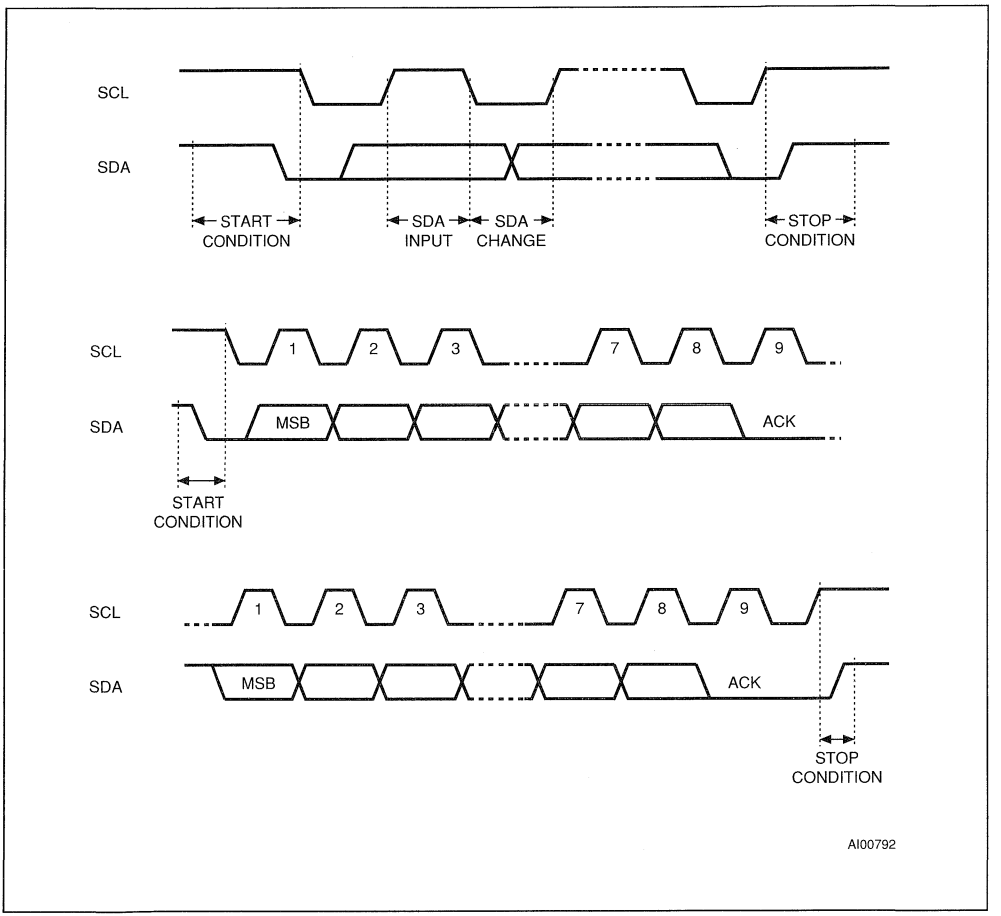


Figure 6. I²C Bus Protocol



Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant Byte Address bits (A7-A4) are the same. The master sends from one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (tw) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

Read operations are independent of the state of the $\overline{WC}$ pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Figure 7. Write Cycle Polling using ACK

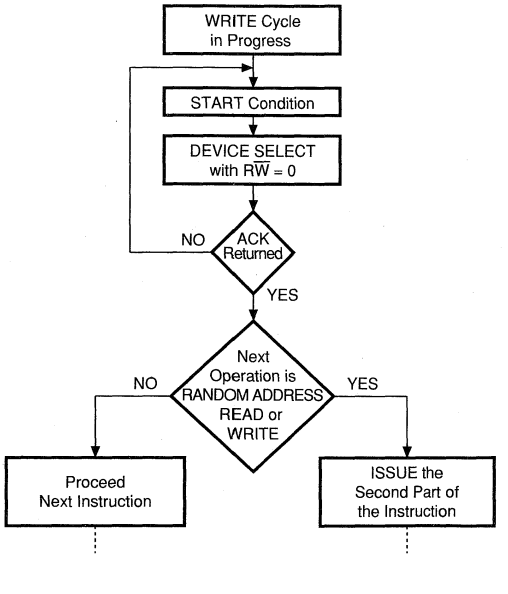
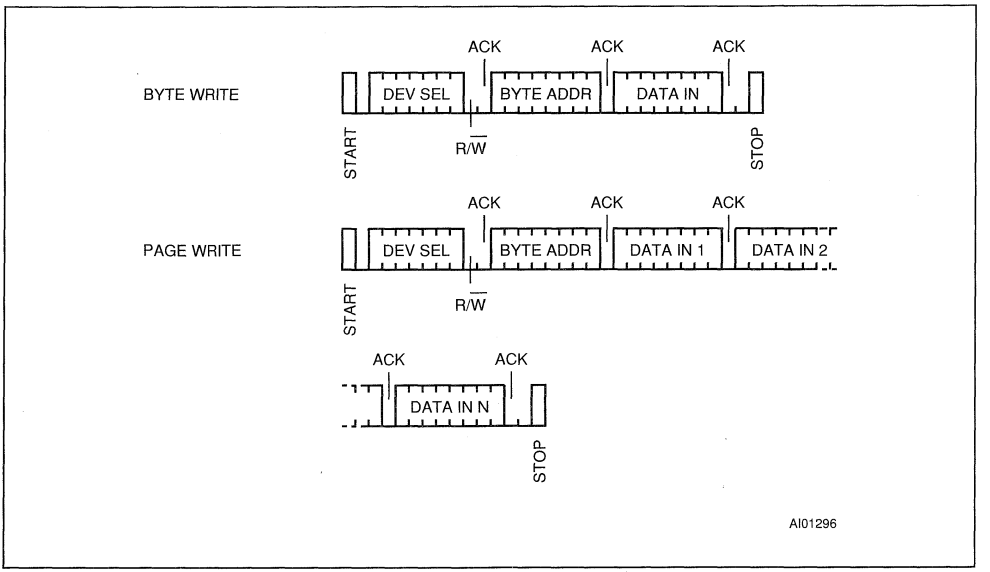


Figure 8. Write Modes Sequence



Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the R/$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25164 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25164 terminates the data transfer and switches to a standby state.

Figure 9. Write Modes Sequence with Write Control = 1

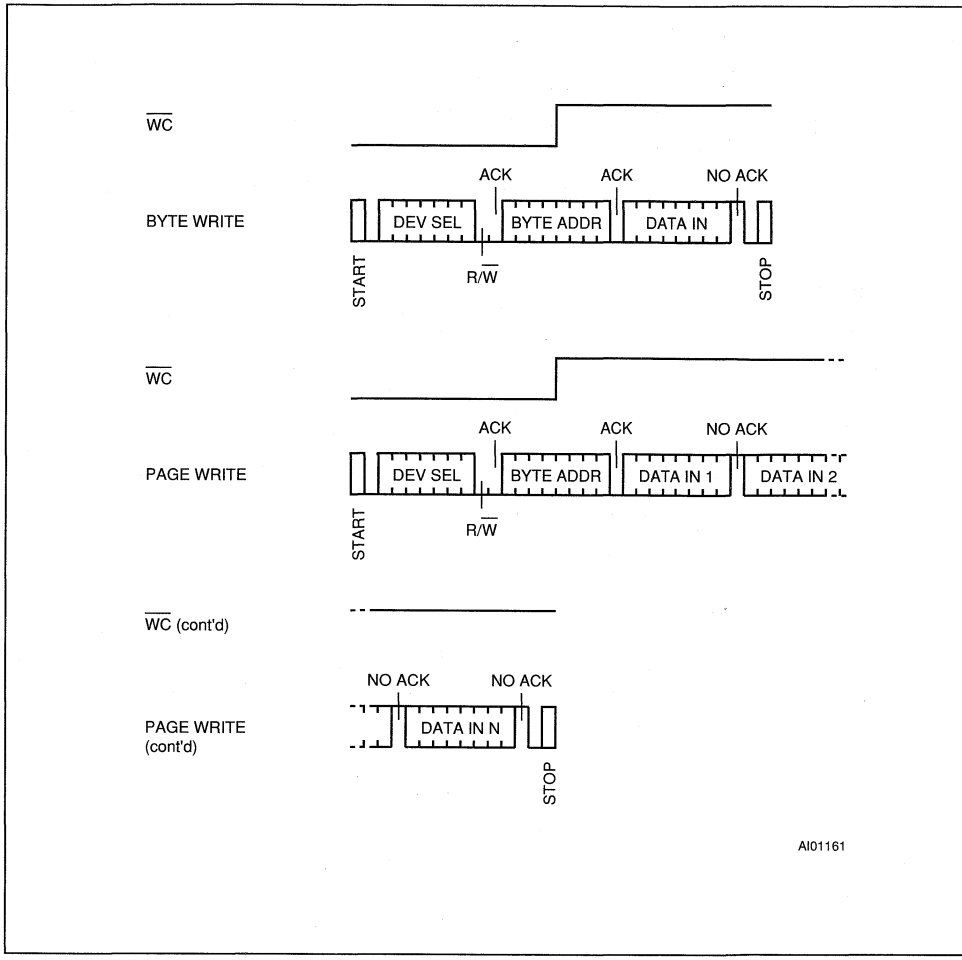
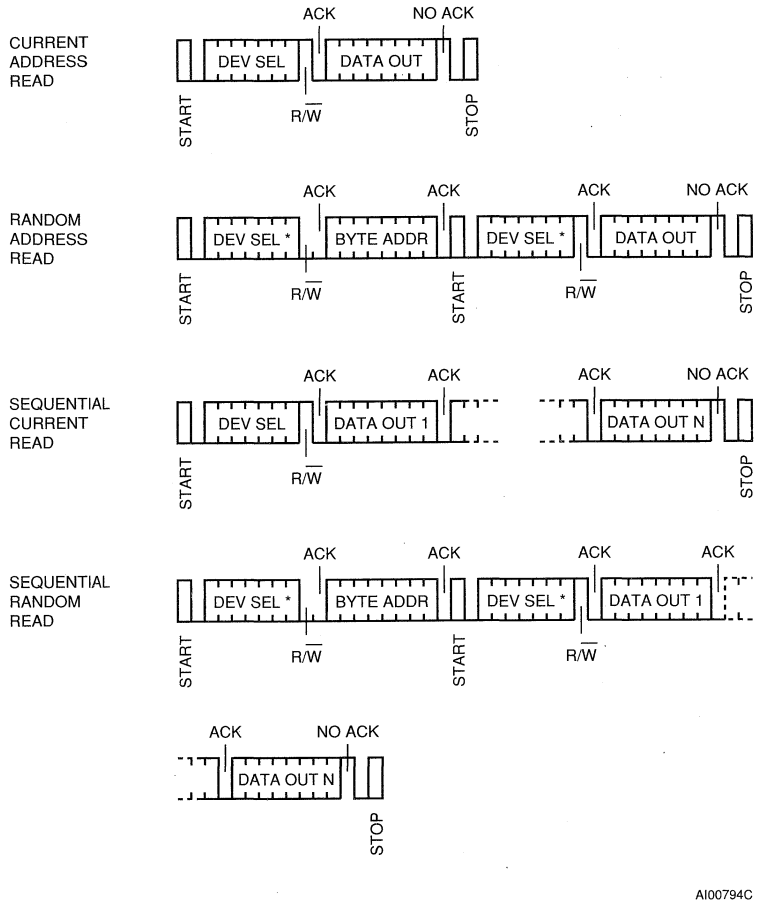
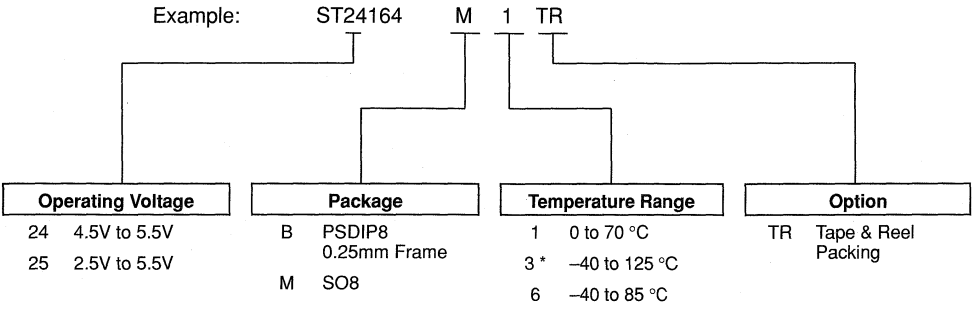


Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

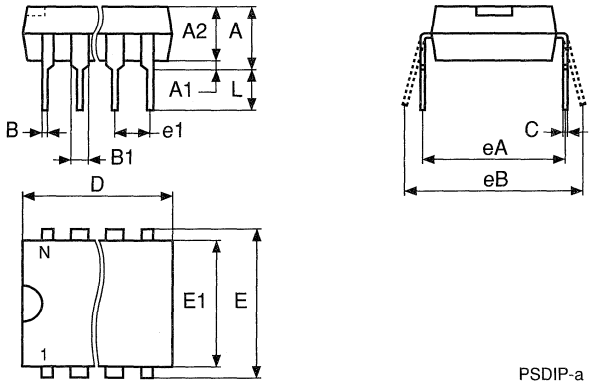
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



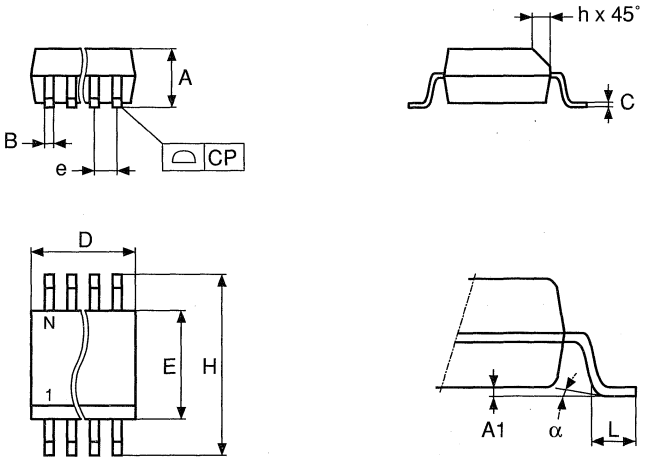
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



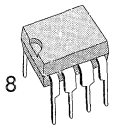
SO-a

Drawing is out of scale

DUAL MODE SERIAL ACCESS 1K (128 x 8) EEPROM

PRODUCT PREVIEW

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2.5V to 5.5V SINGLE SUPPLY VOLTAGE
- 400k Hz COMPATIBILITY OVER the FULL RANGE of SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE I^2C BUS COMPATIBLE
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits. This device can operate in two modes: Transmit Only mode and I^2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK.

The device will switch to the I^2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I^2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode

Figure 1. Logic Diagram

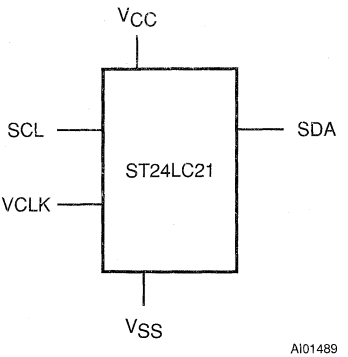
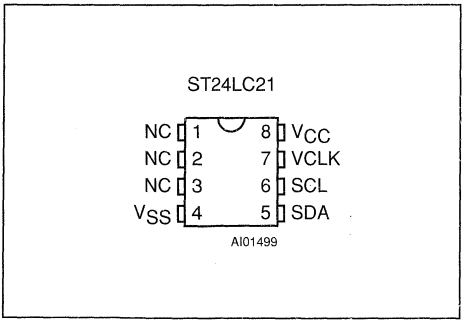
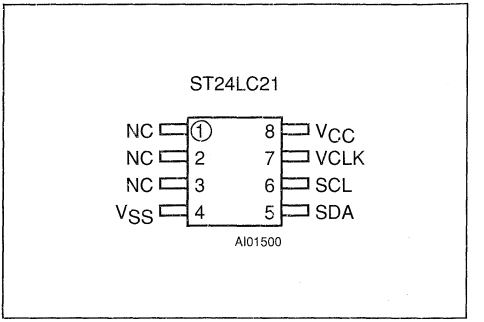


Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Table 3. Device Select Code

	Device Code				Chip Enable			$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	X	X	X	$\overline{RW}$

Note: The MSB b7 is sent first.
X = 0 or 1.

Figure 3. Transmit Only Mode Waveforms

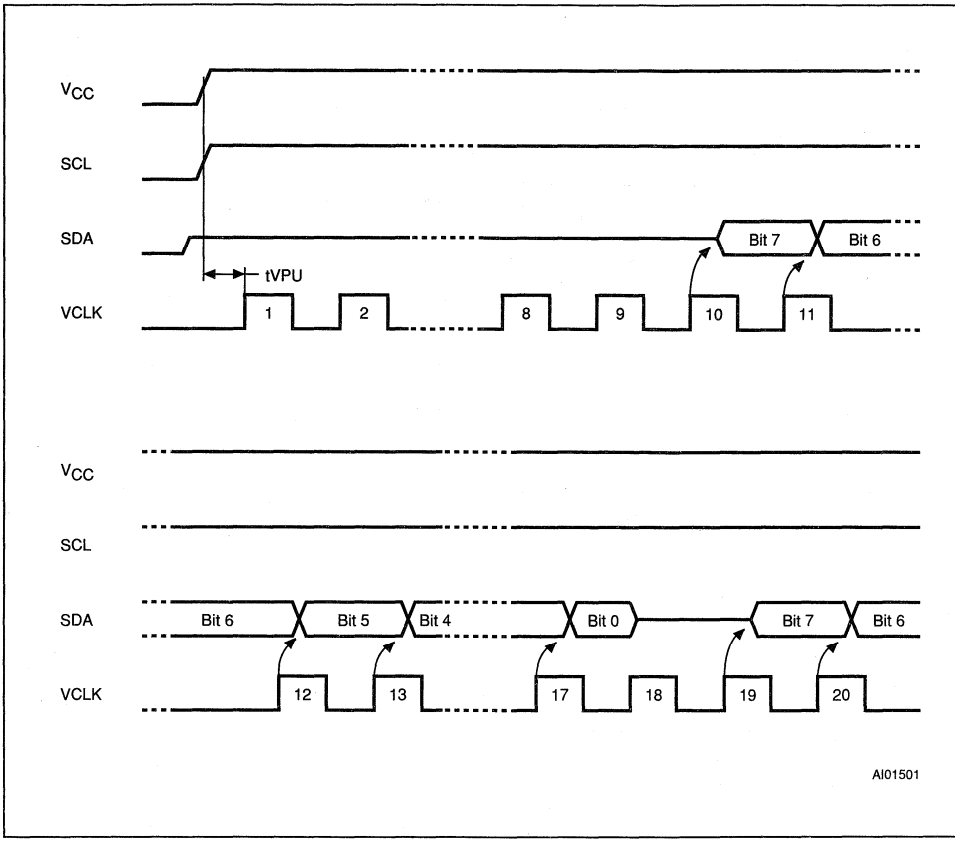
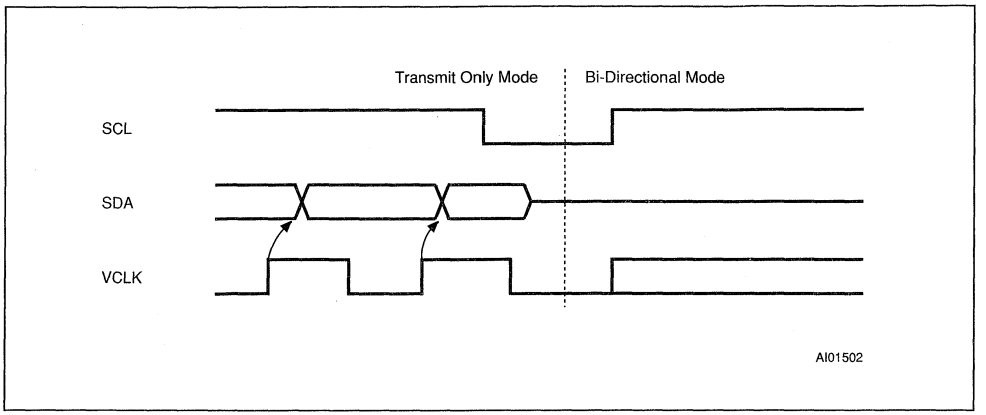


Table 4. Operating Modes

Mode	$\overline{RW}$ bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, $\overline{RW}$ = '1'
Random Address Read	'0'	1	START, Device Select, $\overline{RW}$ = '0', Address,
	'1'		reSTART, Device Select, $\overline{RW}$ = '1'
Sequential Read	'1'	1 to 128	Similar to Current or Random Mode
Byte Write	'0'	1	START, Device Select, $\overline{RW}$ = '0'
Page Write	'0'	8	START, Device Select, $\overline{RW}$ = '0'

Figure 4. Transition Mode Waveforms



Transmit Only Mode

After a Power-up, the device is in the Transmit Only mode. A proper initialization sequence must supply nine clock pulses on the VCLK pin (in order to internally synchronize the device). During this initialization sequence, the SDA pin is in high impedance. On the rising edge of the tenth pulse applied on VCLK pin, the device will output the first bit of byte located at address 00h (most significant bit first).

A byte is clocked out (on SDA pin) with nine clock pulses on VCLK: 8 clock pulses for the data byte and one extra clock pulse for a Don't Care bit.

As long as the SCL pin is held high, each byte of te memory aray is transmitted serially on SDA pin with an automatic address increment.

When the last byte is transmitted, the address counter will roll back to location 00h.

I^2C Bidirectional Mode

The device can be switched from Transmit Only mode to I^2C Bidirectional mode by applying a valid high to low transition on the SCL pin (see Figure 4).

When the device is in the I2C Bidirectional mode, the VCLK input enables (or inhibit) the execution of any write instruction: if VCLK = 1, write instructions are executed; if VCLK write instructions are not executed.

The device is compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The device carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition.

The device behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

I^2C Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 5).

Transmit Only Clock (VCLK). The VCLK input pin is used to synchronize data out when the ST24LC21 is in Transmit Only mode. The VCLK input offers also a Write Enable (active high) function when the ST24LC21 is in I^2C bidirectional mode.

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 5).

DEVICE OPERATION

I^2C Bus Background

The ST24LC21 support the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24LC21 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24LC21 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24LC21 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Figure 5. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus, fc = 400kHz

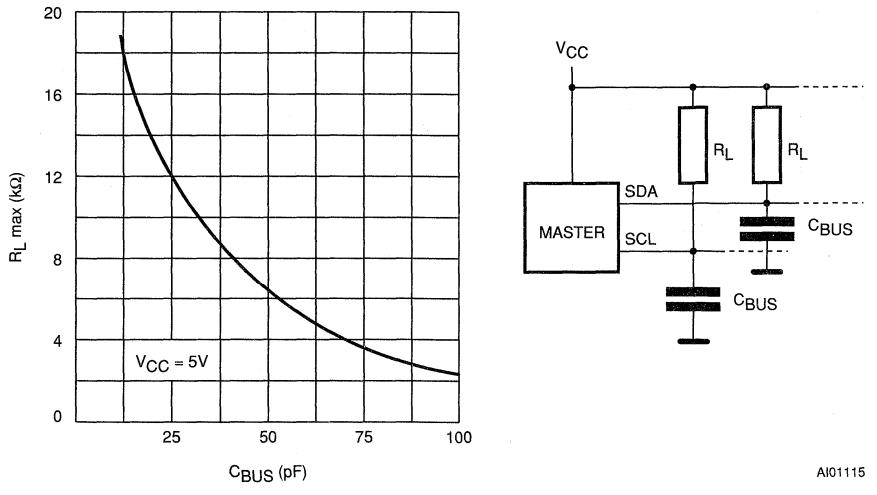


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)			300	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current	V_{CC} = 2.5V, f_C = 400kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		100	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		5	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (VCLK)	2.5V ≤ V_{CC} ≤ 3V	–0.3	0.2 V_{CC}	V
		V_{CC} > 3V	–0.3	0.8	V
V_{IH}	Input High Voltage (VCLK)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA		0.4	V

Table 7. AC Characteristics, I^2C Bidirectional Mode
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL1} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU:STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	900	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

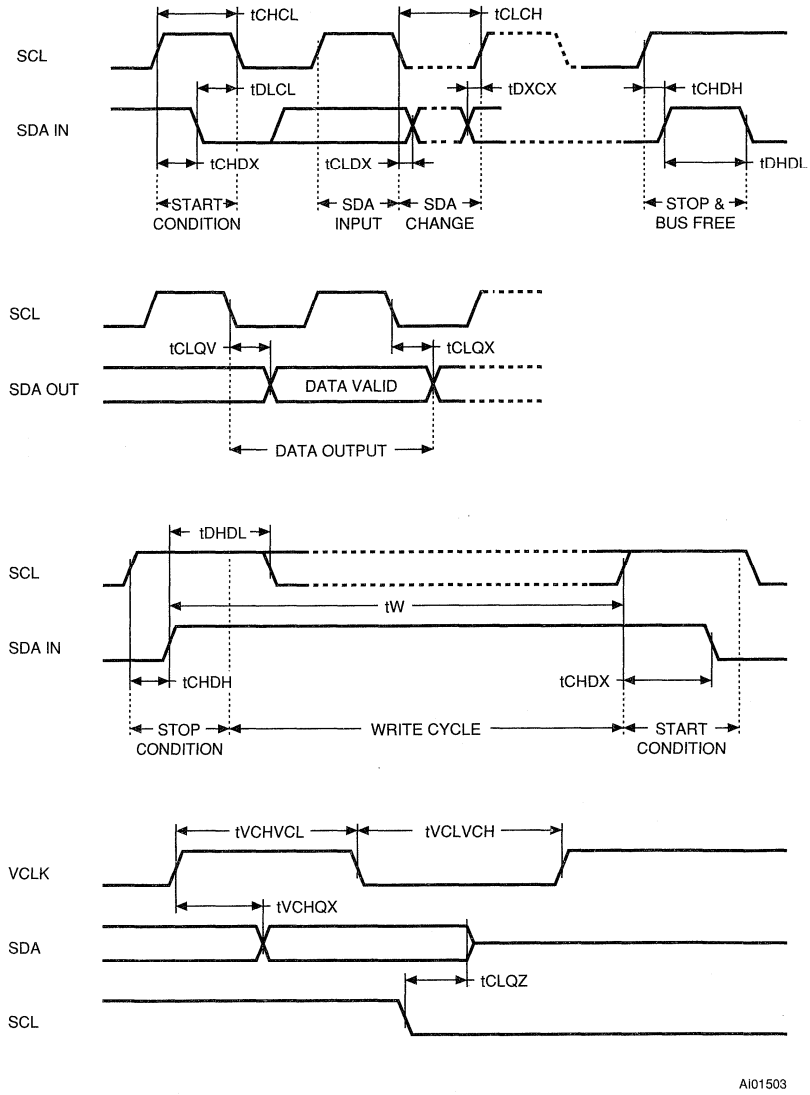
Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

Table 8. AC Characteristics, Transmit-only Mode
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 2.5V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{VCHQX}	t_{VAA}	Output Valid from VCLK		500	ns
t_{VCHVCL}	t_{VHIGH}	VCLK High Time	600		ns
t_{VCLVCH}	tVLOW	VCLK Low Time	1.3		µs
t_{CLQZ}	t_{VHZ}	Mode Tansition Time		500	ns
t_{VPU} (1)		Transmit-only Power-up Time	0		ns

Note: 1. Refer to Figure 3.

Figure 6. AC Waveforms



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages SDA, SCL	$0.2V_{CC}$ to $0.8V_{CC}$
Input Pulse Voltages V_{CLK}	0.4V to 2V
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 7. AC Testing Input Output Waveforms

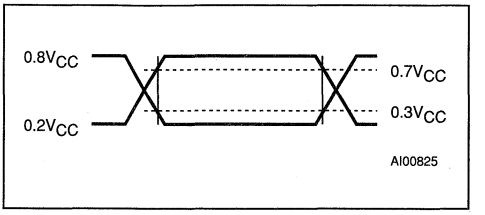


Figure 8. I²C Bus Protocol

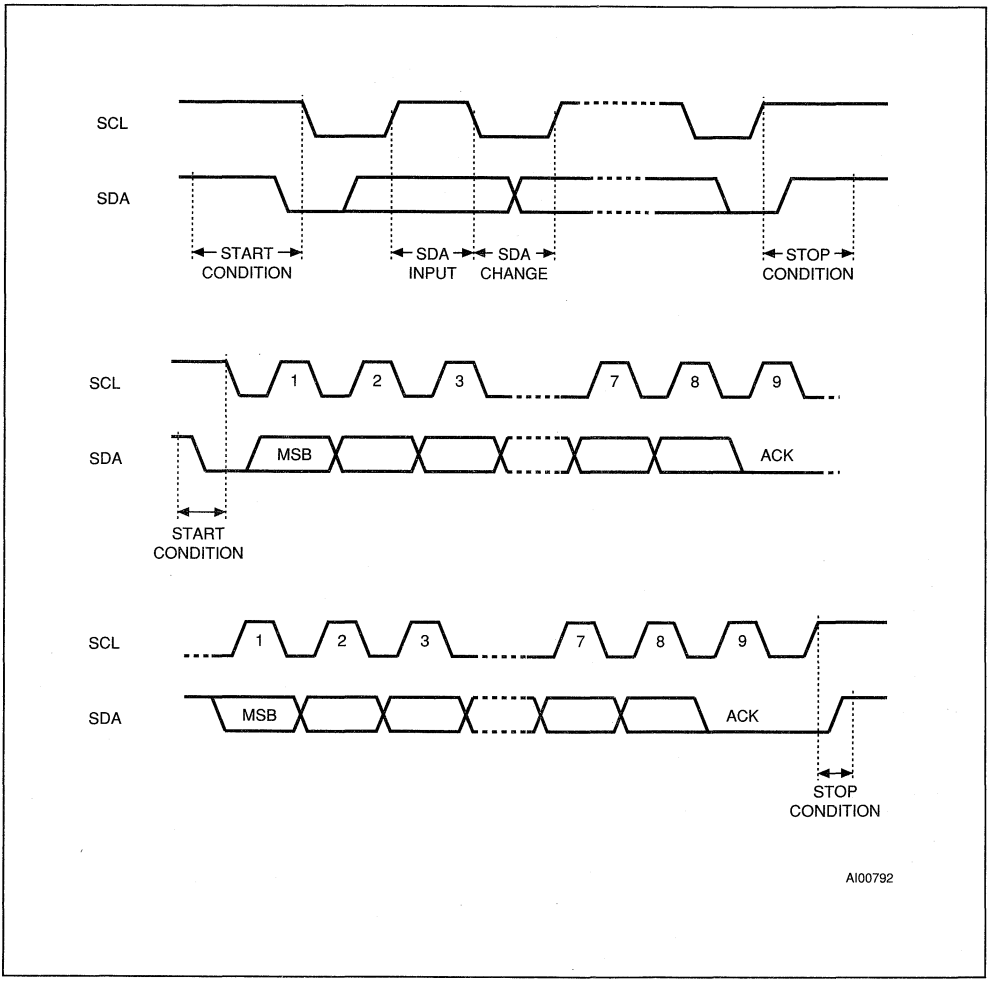
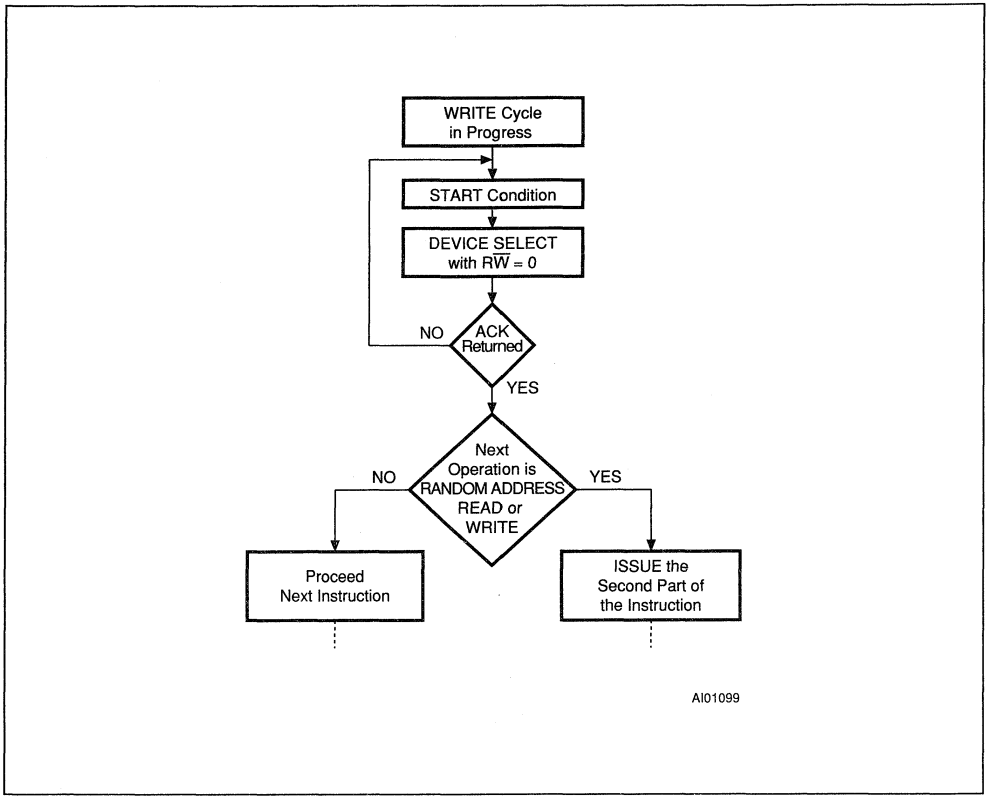


Figure 9. Write Cycle Polling using ACK



Data Input. During data input the ST24LC21 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24LC21, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit. The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits are Don't Care. The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

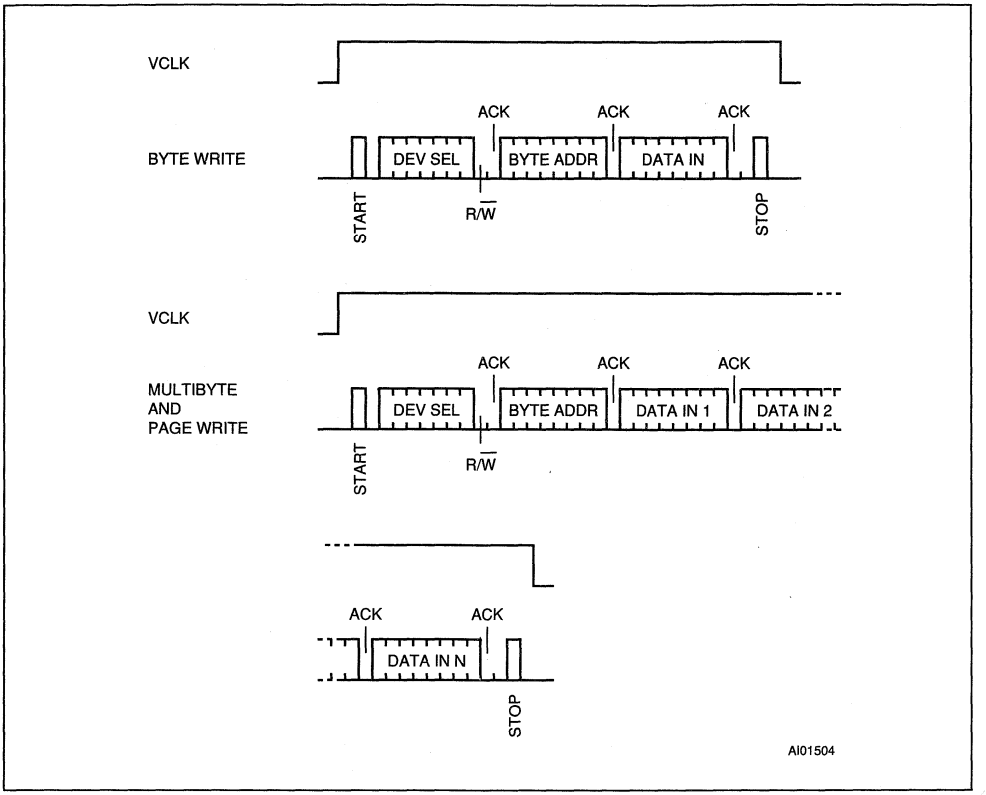
Write Operations

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. After receipt of the byte address the device again responds with an acknowledge.

In I^2C bidirectional mode, any write command with VCLK = 0 will not modify data and will be acknowledged on data bytes, as shown in Figure 11.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Figure 10. Write Modes Sequence

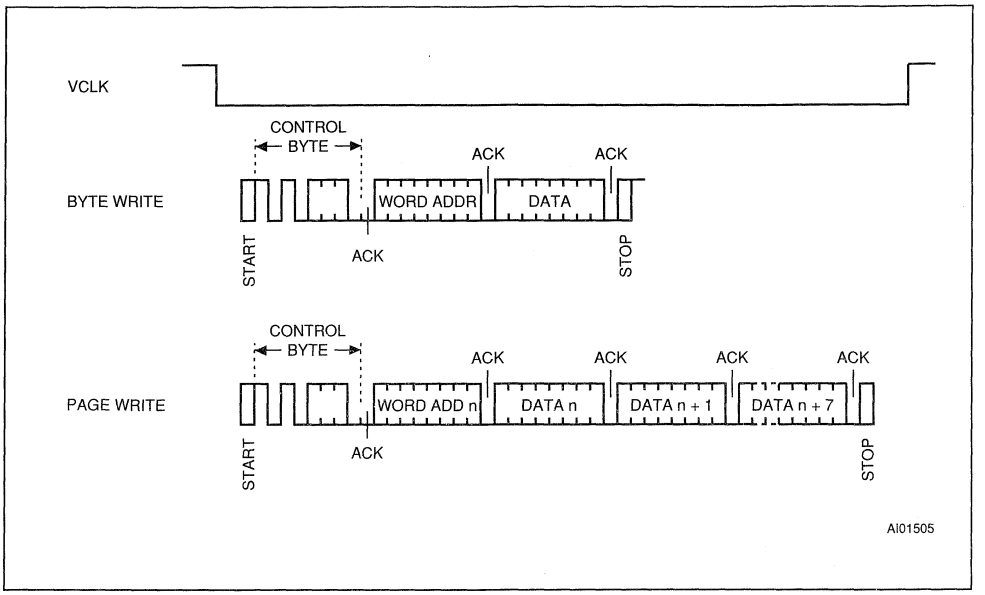


Page Write. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (tW) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 9).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Figure 11. Inhibited Write when V_{CLK} = 0



Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

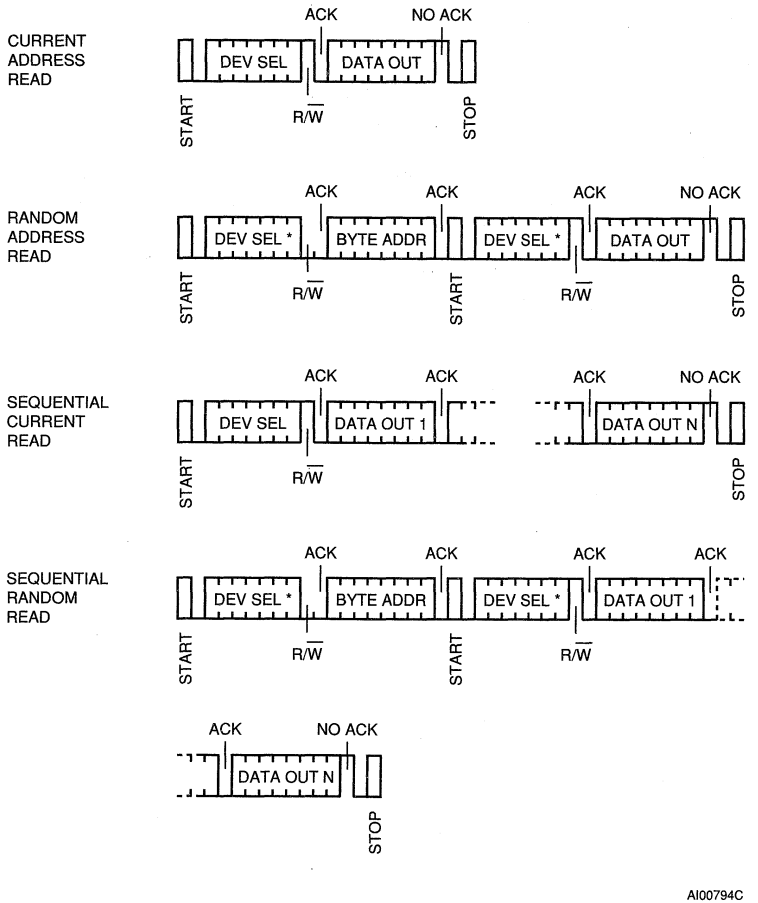
Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 12. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

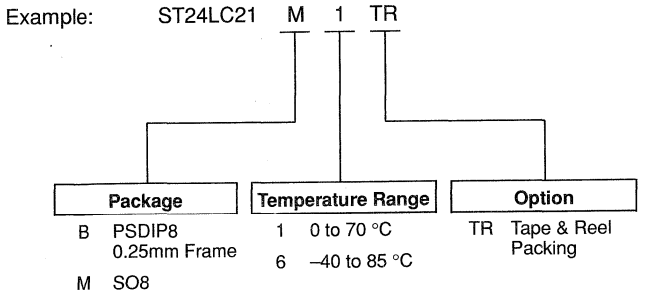
Acknowledge in Read Mode. In all read modes the ST24LC21 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the St24LC21 terminate the data transfer and switches to a standby state.

Figure 12. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFh).

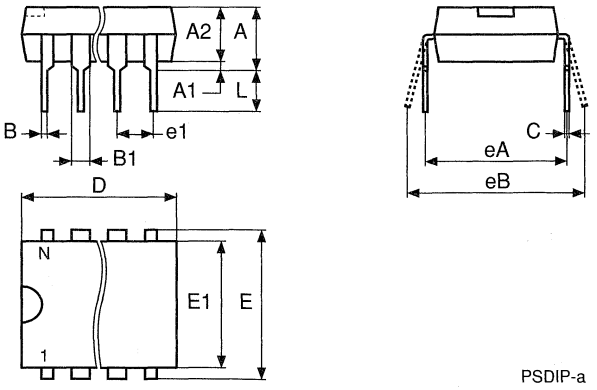
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	

PSDIP8



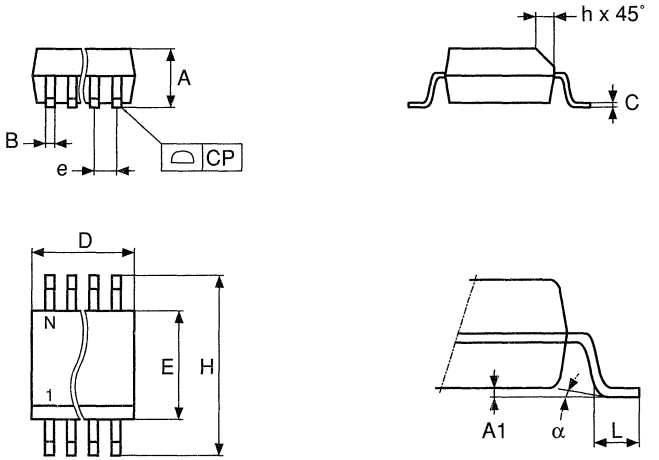
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



SO-a

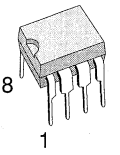
Drawing is out of scale

ST24S08, ST25S08 ST24S16, ST25S16

SECURE SERIAL ACCESS I²C BUS 8K (1K x 8) and 16K (2K x 8) EEPROM

PRODUCT PREVIEW

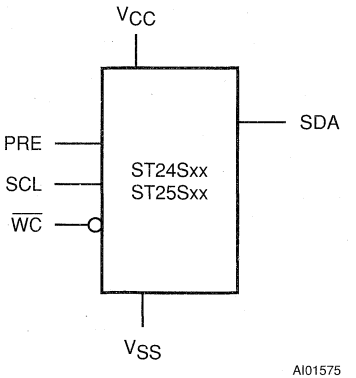
- SECRET KEYS READ and WRITE PROTECTED EEPROM
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24Sxx versions
  - 2.5V to 5.5V for ST25Sxx versions
- HARDWARE WRITE CONTROL
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I²C BUS COMPATIBLE
- PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



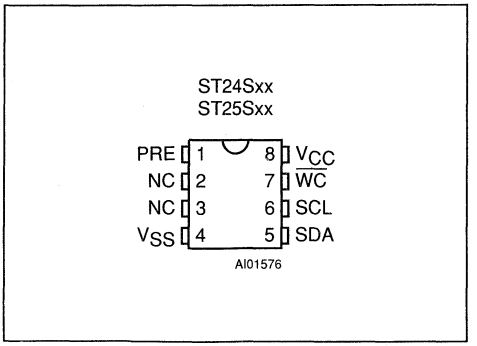
DESCRIPTION

The ST24/25S08 and ST24/25S16 are secure serial access I²C bus EEPROMs of 8K and 16K bits density. A security mechanism using two alternative secret keys (known as the Issuer and User keys) control access to the memory array. When a correct key is recognised by the device, the memory array may be read or written. Additional write protection is provided by the Software Write Protection (SWP), which can inhibit writing to a part of the memory array. In the following text, the ST24/25S08 and ST24/25S16 products are referred to as ST24/25Sxx, where "xx" is the EEPROM size (8 Kbit or 16 Kbit).

Table 1. Signal Names

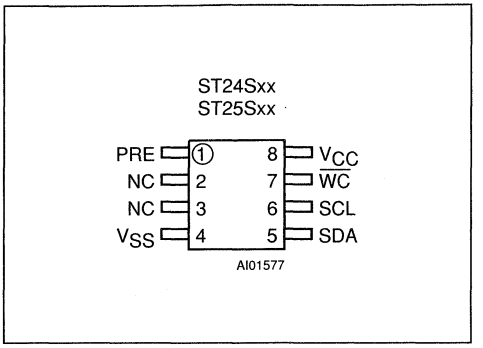
PRE	Write Protect Enable
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition.

The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Table 3. Device Select Code (1)

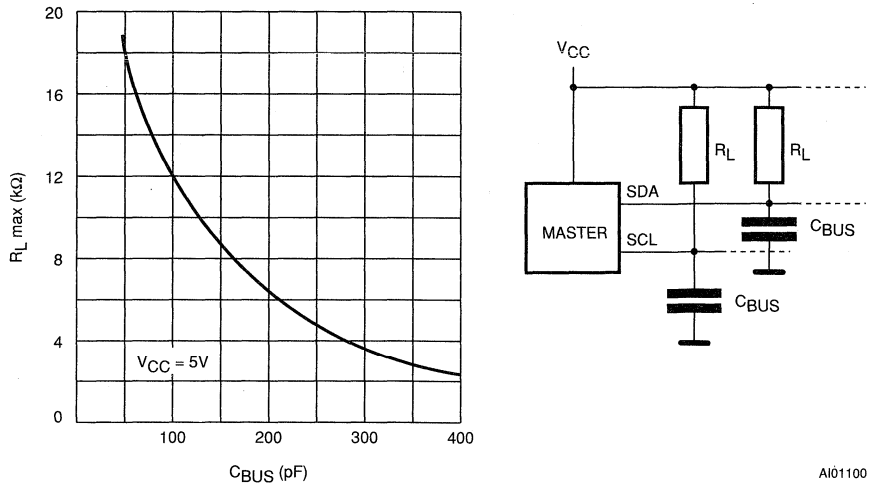
	Device Code				Address Most Significant Bits			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	A10 (2)	A9	A8	RW

Notes: 1. The MSB b7 is sent first.
2. A10 is a "don't care" bit for the ST24S08.

Table 4. Operating Modes

Mode	RW bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, RW = '1'
Random Address Read	'0'	1	START, Device Select, RW = '0', Address,
	'1'		reSTART, Device Select, RW = '1'
Sequential Read	'1'	1 to 1024	Similar to Current or Random Mode
Byte Write	'0'	1	START, Device Select, RW = '0'
Page Write	'0'	16	START, Device Select, RW = '0'

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus



SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Protect Enable (PRE). The PRE input pin, in addition to the status of the SWP page pointer, sets the SWP write protection active.

Write Control ($\overline{WC}$). An hardware Write Control ($\overline{WC}$) feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected the $\overline{WC}$ input is internally read as V_{IL}.

GLOSSARY

Master: Microcontroller or Microprocessor controlling the application.

Key: string of bytes presented by the Master to a Lock address.

Lock: string of bytes stored in the ST24/25Sxx. The Lock can never be read, it may be modified under specific conditions.

SECURITY FUNCTIONALITIES

Memory Map

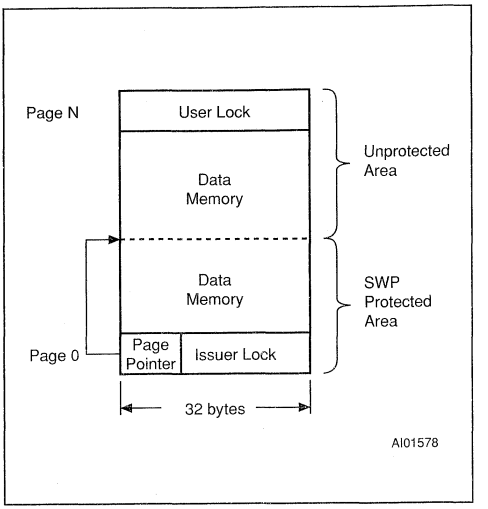
The memory array is organised by bytes (one byte=8 bits) and is divided into 3 parts.

- At the bottom of the memory is the page 0 containing a first byte (address 00h) defined as the page pointer of the Software Write Protection; and the 31 remaining bytes holding the 248 bit Issuer Lock (address 01h to 1Fh)
- The data storage area occupies the largest part of the memory array, from page 1 to page N-1
- A top page N for the User Lock of 256 bits is located at the top of the address space (N=31 for the ST24S08 and N=63 for the ST24S16). See Figure 4.

Memory Access

Access to the various parts of the memory array is controlled and depends on the setting of three parameters: the Security Flag, the SWP status and the $\overline{WC}$ pin.

Figure 4. Memory Map



Security Flag. When the Security Flag is set to '1' (default status at power up) the memory is locked. In this condition, only the Issuer Key or User Key can be presented to the memory (the Read and Write instructions cannot be executed).

When the Security Flag is '0', the memory is unlocked. In this condition, all data can be modified (assuming that $\overline{WC}$ pin is driven low and that these data are not protected by the SWP feature). The Security Flag feature is a global write protection, automatically set upon Power-up.

SWP. The Software Write Protection (SWP) is a programmable protection available for disabling/enabling the execution of the Write instructions addressing the lower part of the memory. The SWP is active when the Most Significant Bit of the page Pointer is set to 0, and the protected area is located from Page 0 up to the Page defined by the content of the Page Pointer (located in Page 0, byte 00h). See Figure 4.

Since the Page Pointer and the Issuer Lock are located in the bottom of the memory, they may be protected from writing by this mechanism.

The SWP feature is a software defined write protection set once for ever.

$\overline{WC}$ pin. THe $\overline{WC}$ (Write Control) pin inhibits ($\overline{WC}$ = 1) or enable ($\overline{WC}$ = 0) any Write instruction execution, whateever is the address. The $\overline{WC}$ feature is a global software lock.

Figure 5. Access Map

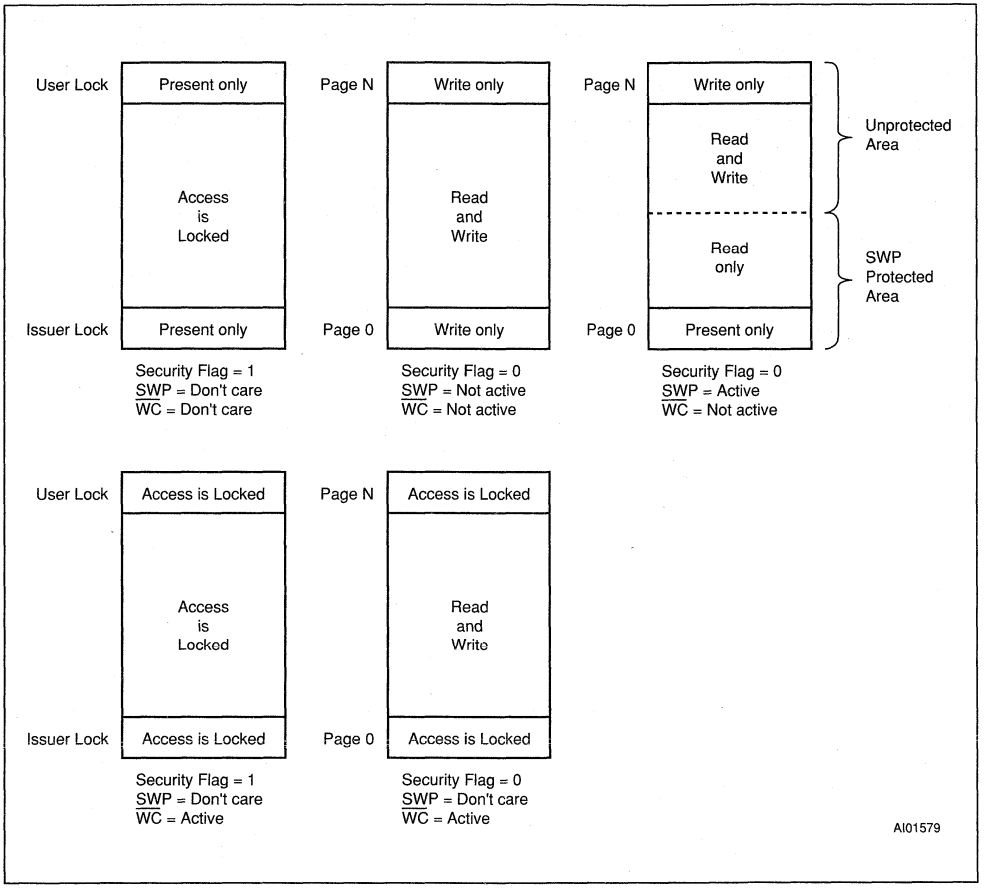


Table 5. Security Operating Instructions

Instruction	Security Flag = 1 (1) SWP Enabled or Disabled	Security Flag = 0 (2) SWP Disabled
Current Address Read	No Access (Data read = FFh)	Read all the memory except Issuer Lock and User Lock
Sequential Read	No Access (Data read = FFh)	Similar to the Current Address Read
Random Read	No Access (Data read = FFh)	Similar to the Current Address Read
Byte Write	Not Executed	Write byte to memory (3)
Page Write	Not executed except for Issuer and User Locks: Present instruction	Page Write to memory (3)

Notes: 1. Security Flag = 1: access is locked
2. Security Flag = 0: access is open
3. When $\overline{WC}$ = 0

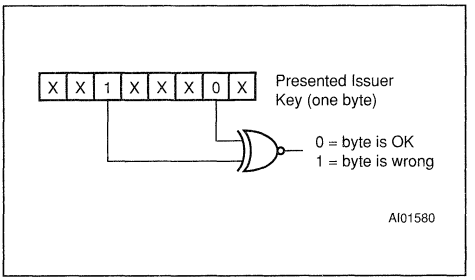
Security Operations

Present a Key. The memory always acts as a Slave on the I^2C bus. In order to unlock the ST24Sxx, the Master must send the correct key to the Issuer Lock address or the User Lock address. This operation is performed with a Page Write instruction to the address of either the Issuer Lock or User Lock. This action is called Present a key.

The memory will take the incoming code and:

- at User Lock address: compare serially bit-by-bit the received User Key with the stored User Lock. User Lock accepts only one User Key which unlocks access to the memory
- at Issuer Lock address: make an XOR of two bits for each received byte according to the value stored in the Issuer Lock. Issuer Lock accepts several Issuer Keys which unlock access to the memory

Figure 6. Presentation of the Issuer Key



If either one of the presentation is correct, then the security flag is cleared to '0' and the data area can be accessed for reading or writing. Any incorrect key presented will set back the Security Flag to '1' whatever is the status of $\overline{WC}$ and SWP; the memory will be locked.

Modify a Key. When the Security Flag is '0' (unlocked) and both SWP and $\overline{WC}$ are not active so that the memory is unprotected, the Issuer Lock or User Lock can be directly re-written.

- When the SWP is active, the Issuer Lock cannot be modified
- Since the User Lock is located at the top of the memory, the User Lock can be re-written by the user, assuming that the SWP is not protecting the whole memory, that is excluding the top page (where the User Lock is stored).

Personalisation of the ST24/25Sxx

Initial Conditions and Preliminary Remarks. When delivered, the memories have all the contents set to FFh (or '1's) and the Security Flag set to '1' (upon reset).

- One page is 32 bytes
- A WRITE instruction (according to the I^2C bus protocol) is decoded by the ST24/25Sxx either as a Present a Key or Write instruction, depending on the status of the Security Flag.
- The Lock is a string of bytes stored into one page of the memory, the Key is the string of bytes presented to the memory.

The issuer defines the Issuer Lock.

Step one: Unlock the blank ST24/25Sxx. The Master sends at User Lock address the User Key value of all '1's (Page Write FF...FFh), which corresponds to the User Lock. The Security Flag will be cleared to '0' and the memory will then be unlocked.

Step two: Write the Issuer Lock new value. The required Issuer Lock can be written provided that both SWP and $\overline{WC}$ features are disabled. The Issuer Lock is written with a Page Write instruction to the Issuer Lock address, each of the 31 bytes having exactly two bits set to '1' (and the other 6 bits cleared to '0'). The Issuer Lock bits set to '1' will define the position of the two inputs of an XOR

Table 6. Presentation or Modification of the Issuer Key

SWP	Security Flag (1)	Code Input	Instruction	Result
Not active	'1'	Issuer Key	Present a Key	Key Wrong: Security Flag set to '1' Key Right: Security Flag set to '0'
	'0'	Issuer Key	Page Write (2)	Write new Issuer Lock
Active	'1'	Issuer Key	Present a Key	Key Wrong: Security Flag set to '1'. Key Right: Security Flag set to '0'.
	'0'	Issuer Key		Option not used for any sensible purpose

Notes: 1. Security Flag = 1: ST24S/25xx is locked, Security Flag = 0: ST24/25Sxx is open.
2. Page of 31 bytes

gate capturing only two bits by byte from the presented bytes of the Issuer Key.

Note: *The V_{CC} supply must not be interrupted between these first and second steps as this would set the Security Flag once more to '1' and lock access to the memory.*

The Issuer Writes Application Data into the Memory. When the Security Flag is reset, data are writen by using a series of normal Byte Write or Page Write instructions addressing the Data Space of the ST24/25Sxx.

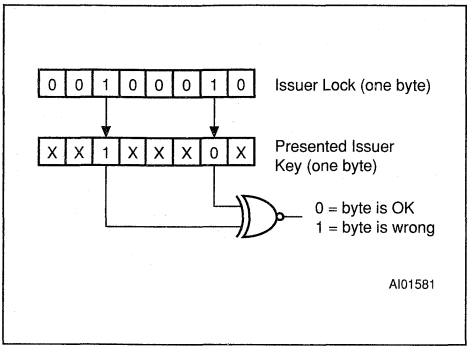
The Issuer Sets the Protection. The SWP Protection is set by programming the Page Pointer (byte 0 of page 00) to define the start address of the Software Write Protection SWP (see figure a). The SWP protection is enabled when the Most Significant Bit of the Page Pointer is set to 0.

Typical Use of ST24/25Sxx in Secured Application

The Application Presents the Issuer Key. When powered, the application should check (from time to time) the authentication of identity of the ST24/25Sxx by presenting the Issuer Key. The Master presents (at Issuer Lock address) an Issuer Key chosen in the family of active keys unlocking the ST24/25Sxx. The family of active keys is the set of bytes which have two bits set to either (0,1) or (1,0) in the correct position of the byte; other bits are Don't Care bits (as shown in figure c).

If the presented Issuer Key matches the Issuer Lock, the Master can access data stored in the ST24/25Sxx.

Figure 7. Definition of the Issuer Key



Write the User Lock. It is very convenient for the end user of a secured application to define his own value of User Key.The User Lock may be written if the SWP does not protect the top page (Top Page =User Lock) with the Security Flag cleared to '0' (which can be achieved if the Master has been previously presenting a correct Issuer Key). The User Lock is written with a Page Write instruction at the User Lock address.

If the power supply is removed, the memory will only be accessible if the correct User Key or Issuer Key is presented to the User Lock or Issuer Lock address respectively. During use, the User Lock which is outside the SWP protected area can be updated, but the Issuer Lock remains fixed.

Table 7. Presentation or Modification of the User Key

Security Flag	Code input	Instruction	Result
'1'	User Key	Present a Key	Key Wrong: Security Flag set to '1' Key Right: Security Flag set to '0'
'0'	User Lock	Page Write	Write new User Lock

Note: If SWP is active, the protection must not cover the top page (User Lock).

Table 8. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 9. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (PRE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (PRE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 10. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

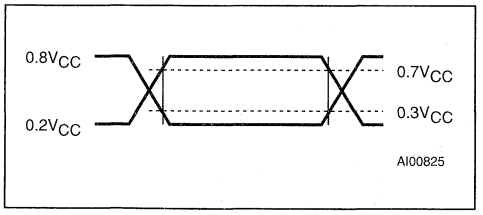
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise Suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W	t_{WR}	Write Time		10	ms

Note: 1. For a reSTART condition, or following a write cycle.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 8. AC Testing Input Output Waveforms



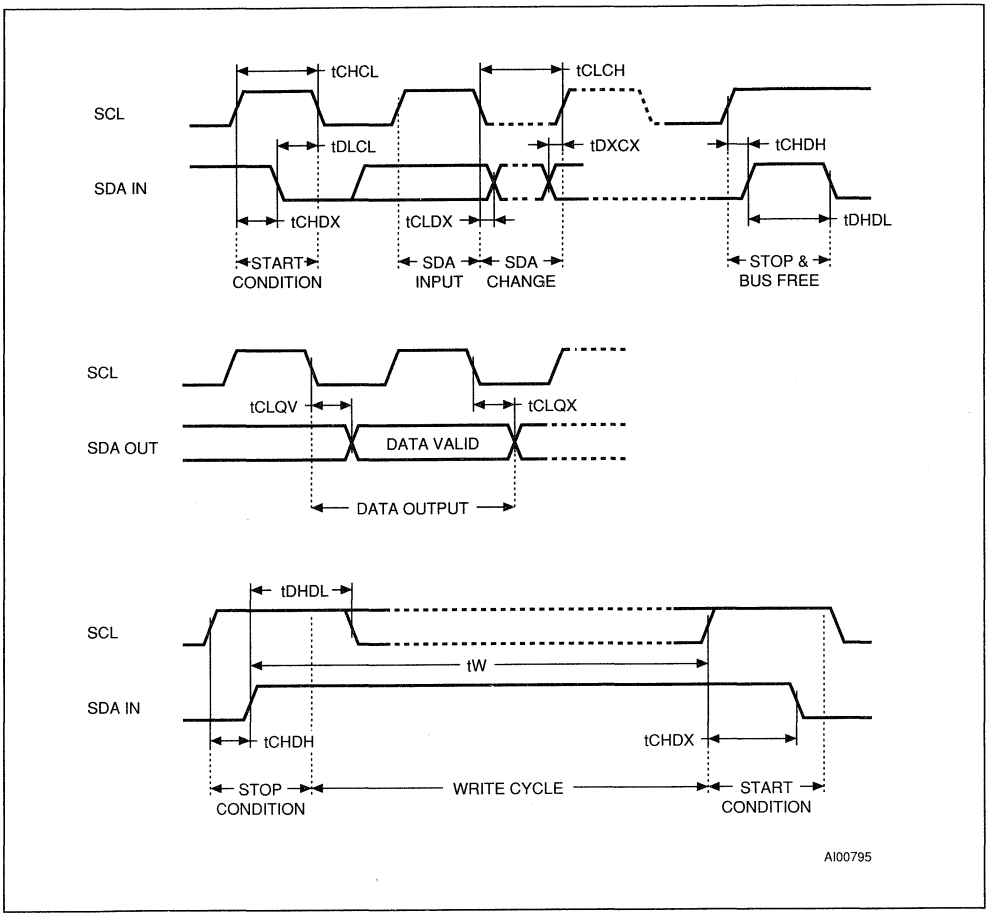
DEVICE OPERATION

I²C Bus Background

The ST24/25Sxx support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25Sxx are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25Sxx continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 9. AC Waveforms



Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25Sxx and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

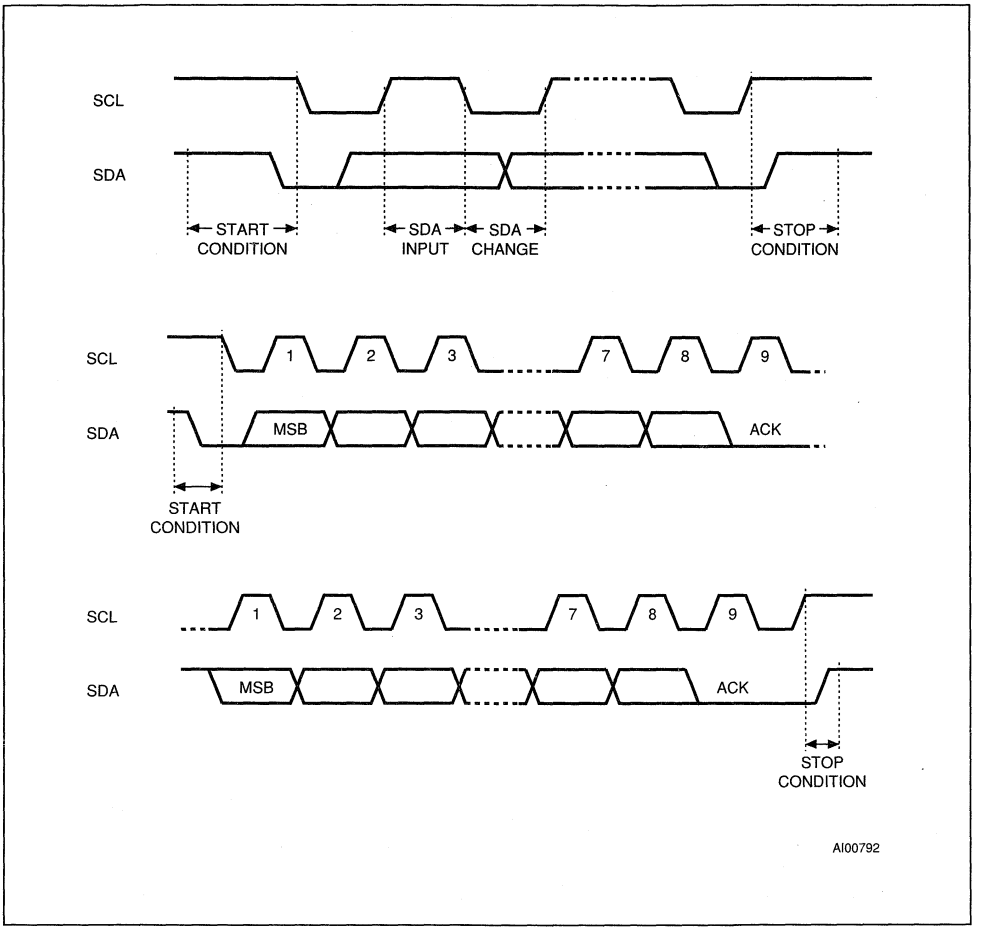
Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25Sxx sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25Sxx, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b.

Figure 10. I²C Bus Protocol



The 5th, 6th and 7th bits are the address most significants bits. The 8th bit is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

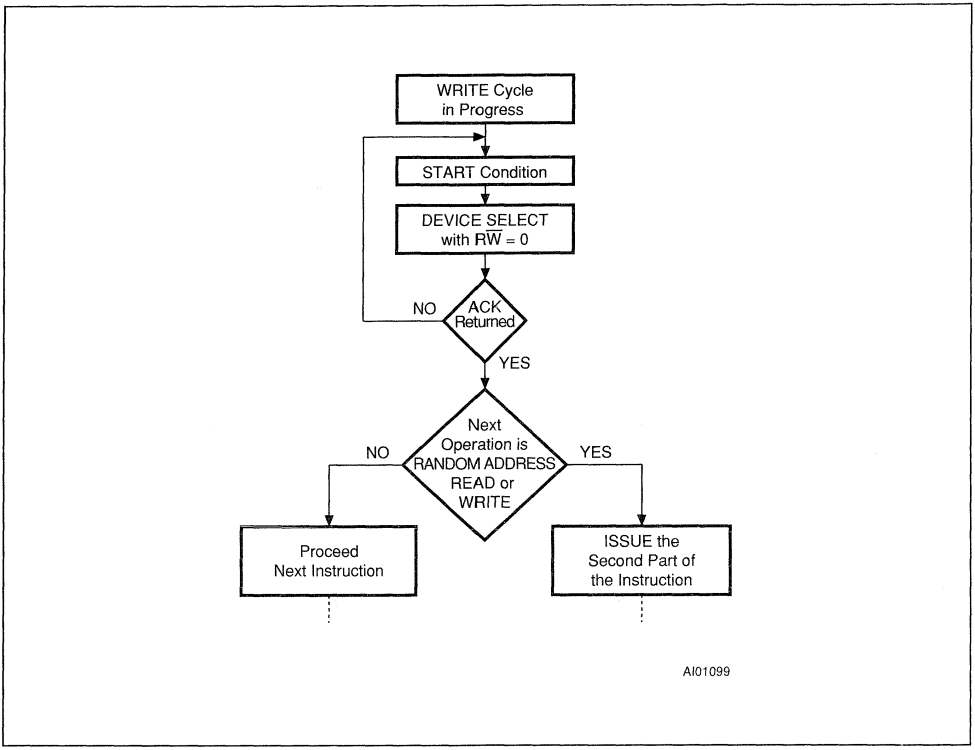
Write Operations

Following a START condition the master sends a device select code with the $R\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to one block of 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25Sxx versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the standby current.

Figure 11. Write Cycle Polling using ACK



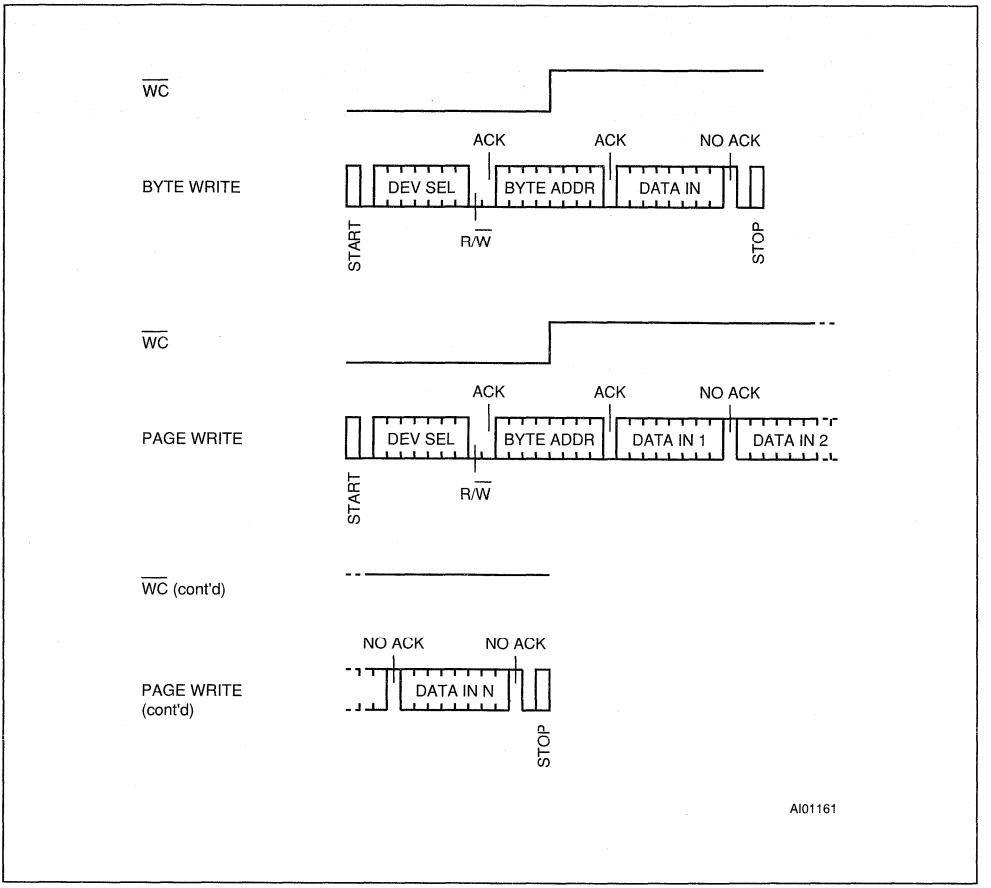
Page Write. The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same inside one block. The master sends from one up to 32 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (5 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 11).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Figure 12. Write Modes Sequence with Write Control = 1



Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

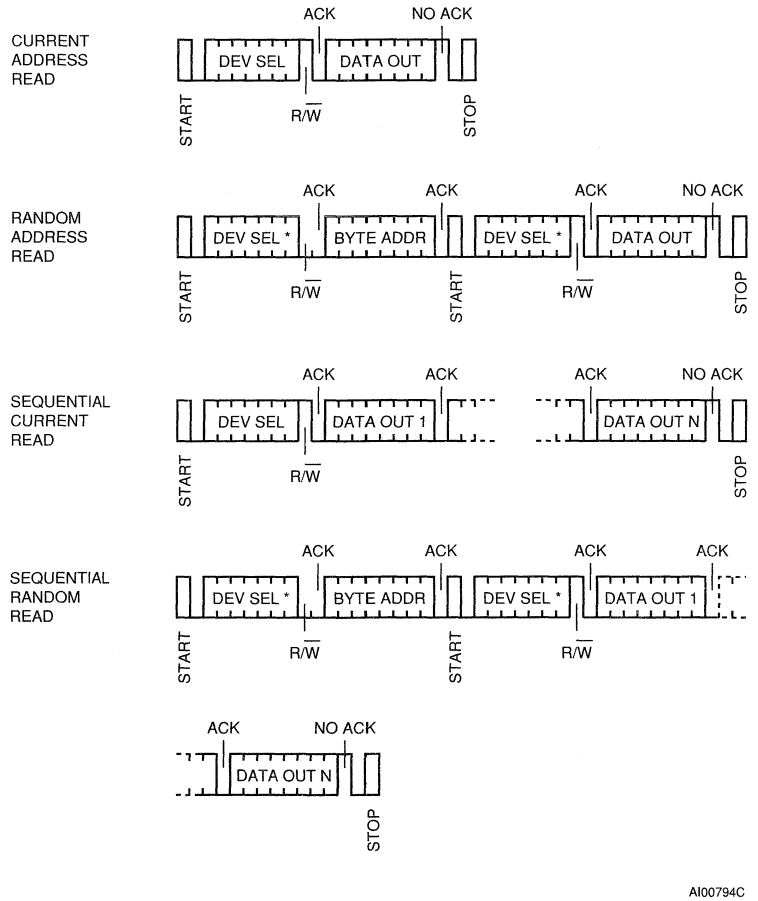
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the

DEVICE OPERATION (cont'd)

master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

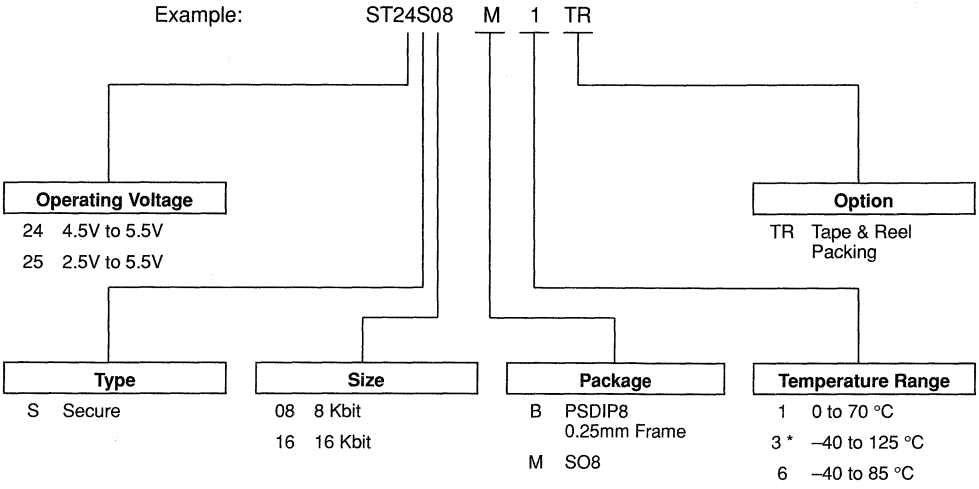
Acknowledge in Read Mode. In all read modes the ST24/25Sxx wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25Sxx terminate the data transfer and switches to a standby state.

Figure 13. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Note: 3 * Temperature range on special request only.

Parts are shipped with the memory content set at all "1's" (FFh).

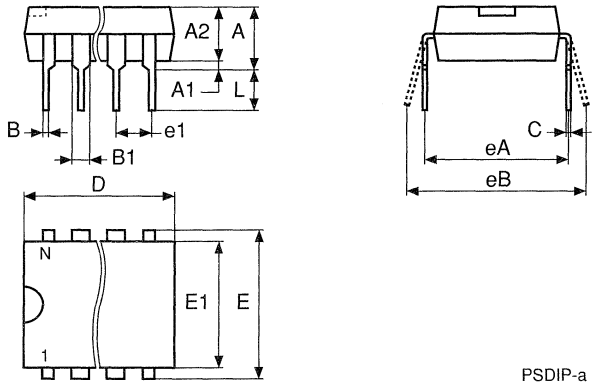
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



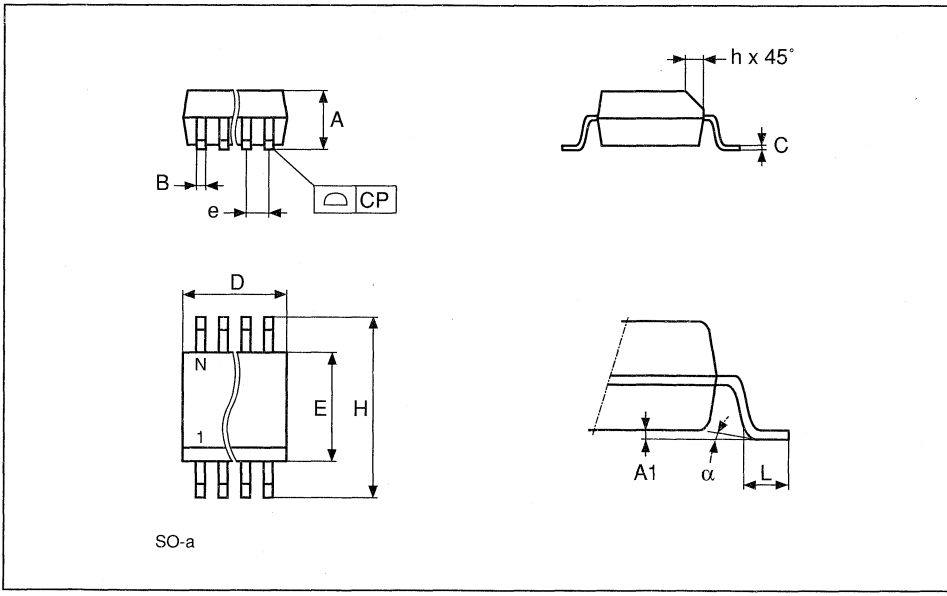
PSDIP-a

Drawing is out of scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is out of scale

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